Simultaneous Capacitor Sharing and Scaling for Reduced Power in Pipeline ADCs

Saqib Q. Malik and Randall L. Geiger
Department of Electrical and Computer Engineering
Iowa State University
Ames, IA 50011
e-mail: {sqmalik, rlgeiger}@iastate.edu

***Abstract*— A technique for reducing power dissipation in pipeline Analog-to-Digital converters (ADCs) is presented. The technique stems from the observation that the amplifier of the first stage is used to charge the input capacitors of the subsequent stage. At the end of the amplification phase, the feedback capacitor of the first stage holds the residue voltage across it and can be reused in the second stage. The feedback capacitor is designed to be a network of capacitor and switches. With appropriate clocking, the network is re-configured to form the input sampling network of the second stage. This reuse is combined with scaling down of the capacitors to result in more power savings.**

I. INTRODUCTION

With newer process technologies to fabricate integrated circuits, the number of transistors that fit on a single die has roughly followed the Moore's law. The higher number of transistors has allowed more digital circuits to be realized on a chip resulting in high processing power. On the other hand, analog circuits do not scale as well and the technology scaling benefits have not been quite so dramatic. In order to utilize the available processing power on a chip, it is essential to convert the analog signals to digital. Analog-to-Digital converters (ADCs) form the bridge between the analog and the digital worlds.

ADCs are used in a variety of applications such as mobile devices including mobile phones, personal organizers etc. Due to their dependence on batteries, much effort has been made to minimize the power consumption of these devices. Many techniques have been proposed to reduce the power consumption of the digital as well as the analog part of the systems that make up these mobile devices. The focus of this paper is to present a technique that can reduce the power consumption of the ADCs.

Many architectures for ADCs have been presented over the years. Pipeline ADCs stand out for achieving high speeds at high resolutions. The block diagram of a pipeline ADC is shown in Fig. 1. The complete pipeline is subdivided into

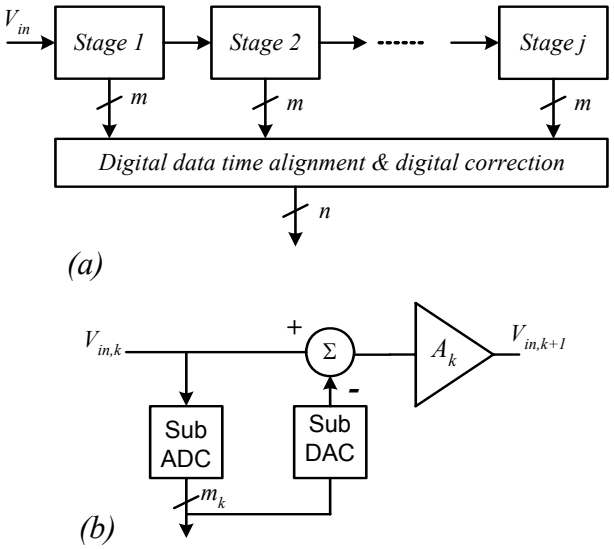

Figure 1. (a) Block diagram of an n-bit, m-bits per stage, pipeline ADC, (b) Block diagram of a single stage

stages with each stage processing the signal from its preceding stage. Each stage may be designed to generate 1 or more bits per stage. The analog signal is applied at the input of the first stage. The stage has a sub-ADC that determines the digital bits for the stage. The digital bits are then used by a sub-Digital-to-Analog Converter (DAC) to add or subtract a reference voltage from the input. An operational amplifier (opamp) then amplifies the signal and creates a "residue" voltage that is passed on to the next stage. Each stage repeats the process until the residue has been processed by the last stage. The distinguishing feature of the pipeline ADC is that it does not have to wait for a conversion to complete before starting a new one. Since each stage process the signal independently of the following or the preceding stage, the first stage starts to sample the next input after it has passed on its residue to the next stage. The output bits corresponding to a specific V_{in} do need to be aligned in time,

0-7803-9197-7/05/$20.00 © 2005 IEEE.

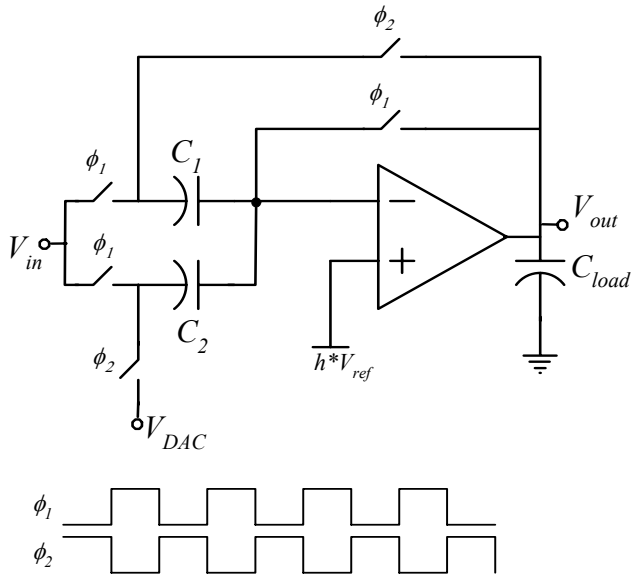

Figure 2. A typical switched-capacitor MDAC structure

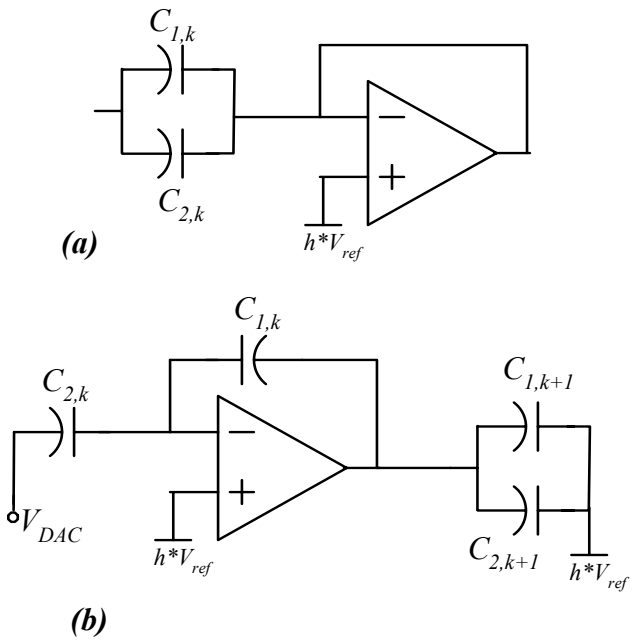

Figure 3. Operation of a typical MDAC

as shown in Fig. 1a. Furthermore, pipeline ADCs lend themselves to calibration algorithms [2]-[4] and correction techniques [5] that allow correcting of many common errors.

Traditional pipeline stages combine the function of the DAC and amplification into one block, commonly referred to as the Multiplying DAC (MDAC). By observing that there is interaction between the MDAC of stage k and the input of stage k+1, the possibility arises of sharing the capacitors between two adjacent stages in order to save power. A technique is presented in this paper that exploits the interaction of two stages to reduce the power dissipation in the MDAC of the first stage. Although the sharing can be extended throughout the pipeline, only first two stages are considered for modification due to their higher power requirements.

Operational amplifiers (opamps) are the major contributors towards the overall power dissipation in pipeline ADCs. The opamp power dissipation is proportional to the capacitive load they have to drive. In a typical MDAC based pipeline stage, the opamp must simultaneously drive its own capacitive feedback network as well as the capacitive sampling network of the following stage. A technique is proposed that uses a portion of the feedback network as the sampling network of the subsequent stage thus eliminating the need to charge a separate sampling network and reducing the capacitive drive requirement of the opamps.

The operation of a typical MDAC will be presented in Section II. Section III will describe the details of the proposed technique.

II. Operation of a Typical Pipeline Stage

A typical MDAC for a nominal 1-bit per stage pipeline ADC stage is shown in Fig. 2 [6]. The two capacitors C_1 and C_2 form the sampling network. The two non-overlapping clocks ϕ_1 and ϕ_2 are used to determine the sampling or the amplification mode of the MDAC. Ideally, $C_1=C_2$, $V_x=V_{ref}$, and $h=0.5$.

For the kth stage in the pipeline, the circuit operates as follows. When ϕ_1 goes high, the sampling capacitors sample the input voltage. At the same time, the sub-ADC compares the value of the input and generates an output bit d_k. The digital bit, d_k, is also sent to the sub-DAC of the stage. The output of the DAC, V_{DAC} is V_{ref} or zero for a d_k of 1 or 0, respectively. At the end of the sample phase, ϕ_1 goes low and ϕ_2 goes high. The resulting configuration is shown in Fig. 3b. Charge is transferred from capacitor C_2 to C_1 resulting in the residue voltage given by

$$V_{res,k} \approx \left(1+\frac{C_1}{C_2}\right) - \frac{C_1}{C_2} \cdot d_k \cdot V_{ref}$$

While stage k is in the amplification phase, the stage k+1 is in sampling phase, as shown in Fig. 3b by the capacitors $C_{1,k+1}$ and $C_{2,k+1}$. By the end of ϕ_2, the opamp output has settled to the residue voltage and the sampling capacitors of stage k+1 have now acquired the residue voltage. A key observation is that at this moment, $C_{1,k}$ also holds the final residue voltage across its terminals.

III. Proposed Technique

A. Operation

The proposed technique exploits the fact that the feedback capacitor, $C_{1,k}$, of the MDAC holds the residue

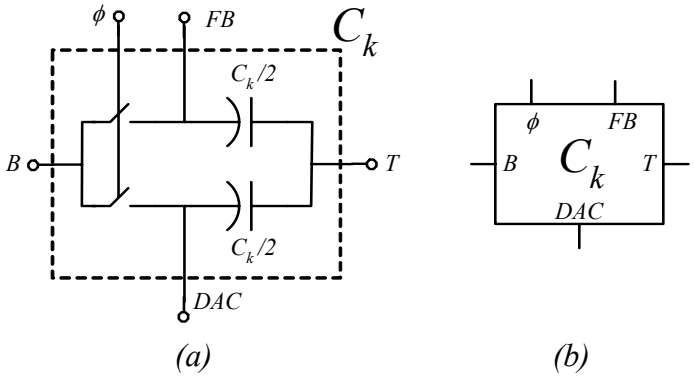

Figure 4. Compund Capacitor Network (CCN) and its symbol

signal at the end of the amplify phase. We propose re-using the charge stored on the feedback capacitor instead of re-sampling the residue on the capacitors of the next stage. To achieve this, $C_{1,k}$ is implemented as a compound capacitor network (CCN) of capacitors and switches, as shown in Fig. 4. Each CCN is made up of two capacitors and two switches. For the case where it is desired to have C_1=C_2, each sub-capacitor is made to be equal to $C_{1,k}/2$. To use the CCN as a single capacitor, the control clock ϕ is set to high placing the two capacitors in parallel. The equivalent capacitance seen between the top terminal, T, and the bottom terminal, B, of the resulting network is given by $C_{1,k}$. When the control clock signal ϕ goes low, the sub-capacitors become independently accessible through the terminals FB and DAC. The terminals FB and DAC connect to the next stage's opamp's feedback node and the VDAC, respectively.

In the proposed scheme, two CCNs are required for two consecutive stages. Two clocks, *chA* and *chB*, in conjunction with other control signals (not shown for simplicity), are used to choose appropriate capacitors C_A or C_B between two adjacent stages. The circuit uses clocks similar to those used in the traditional case and are shown in Fig. 5d.

At the beginning of a conversion, the first stage is configured to use the CCN C_A, as shown in Fig. 5a. With *chA* and ϕ_1 high, C_A appears to be a single capacitor and samples the input voltage with C_2. With *chA* staying high, ϕ_1 goes low and ϕ_2 goes high placing the first stage in amplification mode. Notice from the configuration of the circuit in this mode, shown in Fig. 5b, that the next stage is not connected to the output of the first stage's opamp at all. This is possible since the input capacitive network of the second stage has been eliminated. As a result, the capacitive load of the opamp is reduced by the total capacitance of the second stage's sampling network.

By the time ϕ_2 becomes low, the appropriate residue voltage has been formed across C_A. At the end of ϕ_2, *chA* goes low and *chB* goes high. Simultaneously, ϕ_1 goes high placing the first stage in sample mode but using C_B instead. This switching of C_A into the second stage results in

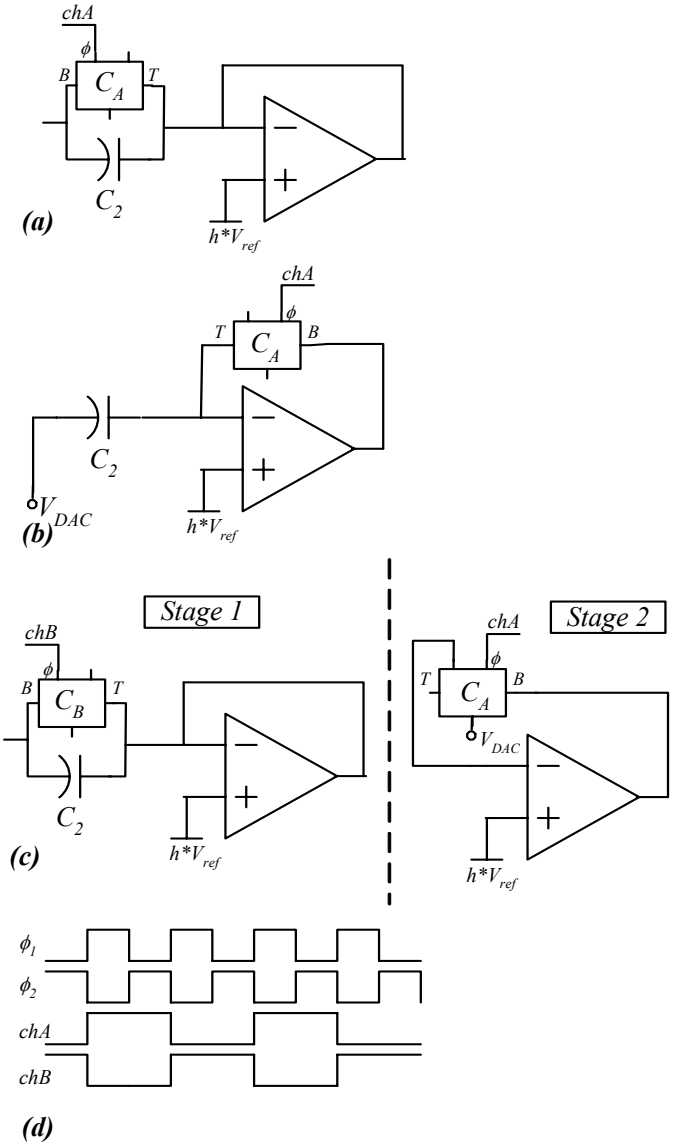

Figure 5. Structure of the pipeline with CCNs in different stages of operation

"unfolding" of the CCN. Consequently, when the clock ϕ_2 for the second stage goes high, C_A is connected to the second stage's opamp such that it is identical to the topology of the stage in its traditional amplification mode. At the end of ϕ_2, *chA* goes high again placing C_A into the first stage. Similarly, C_B is now moved to the second stage and the process is repeated.

B. Advantages

The proposed scheme has many benefits as compared to the traditional pipelined ADC. First, since the total capacitance that needs to be driven by the opamp is cut down, the power dissipation in the opamp is reduced. Since the opamp needs to drive smaller loads than before, the design requirements are relaxed.

It is well known that the capacitor sizes in a pipelined ADC can be scaled down for reducing power dissipation [1]. Although this reduction increases the stage's noise contribution to the overall noise, the power savings may be more important in many applications. When the C_A from stage k is switched into stage k+1, the capacitors that now form the capacitor network of stage k+1 are automatically scaled by a factor of 2 as compared to stage k. This tapering of capacitor sizes results in lower power dissipation for the combined ADC. Additionally, since the $k+1^{th}$ stage does not need to have its opamp present to sample the residue from stage n, it opens up the possibility of further power saving by sharing opamp between stages k and k+1. Finally, since the load seen by the opamp of stage k is reduced, the time required for the output to settle within a desired window is reduced too, allowing faster speeds of operation.

IV. Simulation results

To validate the proposed technique, a simple setup was selected. The first two stages were implemented using the CCNs followed by two stages of conventional architecture. Each stage's capacitor sizes were designed for a gain of 2. Behavioral descriptions of circuit elements using Verilog-A were used for the opamps and comparators. The simulation results showing the 4 output bits for a ramp input are shown in Fig. 6. As can be seen, the circuit worked according to design demonstrating that the residues were formed and passed through the pipeline as desired.

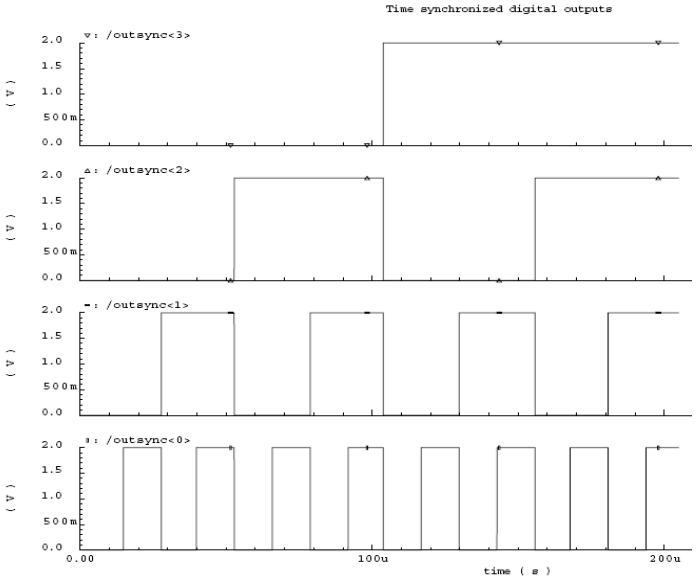

Figure 6. Simulation results showing the correct synchronized digital outputs for a ramp input

V. Conclusions

A new technique to reduce the power dissipation in pipeline ADC was presented. The technique proposed replacing the feedback capacitor in the first stage with a network of capacitors that can be configured as the sampling network of the second stage. This capacitor sharing reduces the load on the opamp, reuses the charge stored on the feedback capacitor, and allows scaling of the capacitor sizes in the second stage for more power savings. Simulation results were used to prove the soundness of the proposed technique. The technique has also been adapted to work in cyclic ADCs [7].

Acknowldgments

This work was supported in part by Semiconductor Research Corporation (SRC).

References

[1] D. W. Cline, and P. R. Gray, "A power optimized 13-b 5 Msamples/s pipelined analog-to-digital converter in 1.2 μm CMOS", IEEE Journal of Solid-State Circuits, vol. 31, pp. 294-303, March 1996.

[2] A. Karanicolas and H. Lee, "Digitally Self-Calibrating Pipeline Analog-to-Digital Converter", US Patent No. 5499027, Mar. 1996.

[3] E. Soenen and R. Geiger, "Accuracy Bootstrapping", US Patent No. 5327129, July 1994.

[4] J. Ingino and B. Wooley, "A Continuously Calibrated 12-b, 10-MS/s, 3.3-V A/D Converter", *IEEE J. Solid-State Circuits*, Vol. SC-33, pp. 1920-1931, Dec.1998.

[5] S. H. Lewis and P. R. Gray, "A pipelines 5Msamples/s 9-bit analog-to-digital converter," IEEE J. Solid-State Circuits, vol. 22, pp. 954-961, Dec. 1987.

[6] R. J. Baker, CMOS: Mixed-Signal Circuit Design vol. II, IEEE press , 2002.

[7] B. Soufi, S. Q. Malik, and R. L. Geiger, "A capacitor sharing technique for RSD cyclic ADC", in Proc. of IEEE Midwest Symp. Circ. Systems, August 2005.