Statistical modeling of over-range protection requirement for a switched capacitor inter-stage gain amplifier

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***Abstract*— Over-range protection requirements for switched capacitor inter-stage amplifiers in pipelined analog to digital converters are investigated. Two popular inter-stage amplifier architectures, charge-redistribution and flip-around, are considered. Closed form expressions for the three sigma variation of the output trip point voltage levels of the amplifier transfer curve are given for both architectures. These expressions can be used for to determine the level of over-range protection required and to assist in allocation of error budgets to different pipeline blocks.**

I. Introduction

The design of high speed high accuracy Analog-to-Digital converters (ADCs) is of growing interest to the semiconductor industry. The common choice for such ADCs is a pipeline structure. Process variations and limitations introduce gain errors, sub-DAC errors, and offset errors in the residue transfer characteristics of the amplifier and these errors can cause the actual output range of the amplifier to become unacceptably large [1] - [4]. This creates what is generally termed an over-range problem and over-range protection circuits are invariably used to ensure that these errors do not unacceptably degrade the performance of the pipelined ADC. Errors introduced by the finite operational amplifier gain can be reduced by using a positive feedback amplifier [5] or by using correlated double sampling [6] and hence will be ignored in following analysis. Calibration techniques in the sub-DAC can minimize its error contribution in the overall pipeline [7].

The sub-DAC and the interstage amplifier in a pipelined ADC are often combined into a single switched-capacitor gain block that functions as a Multiplying Digital to Analog Converter (MDAC). Two commonly used MDAC architectures, one that we term a charge-redistribution (CR) structure and one that is often termed a flip-around (FA) structures are quite popular. [2], [3], [8] In this paper, over-range protection for these two MDAC structures is discussed. In particular, closed form expressions for the 3σ variation of the output over-range protection voltage at the discontinuities in the residue amplifier transfer characteristics (often termed trip points) are given as a function of several critical random variables; the closed loop gain, amplifier and comparator offsets, and sub-DAC output voltages.

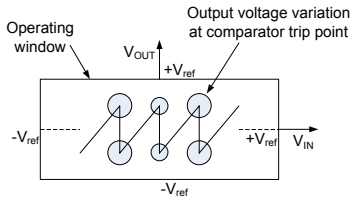

Fig. 1. Pipeline ADC single stage residue transfer

It will be shown that for the FA structure, the over-range protection requirements change from one trip point to another. This is due to the dependence of the output trip point voltage level variation on the input voltage level. In contrast, the over-range protection requirements for the CR architecture are independent of the input voltage level.

From the point of view of total power consumption and input referred noise, the FA is favored over the CR architecture [8]. Regardless of which architecture is ultimately use, the closed form expressions will facilitate error budget allocation for both architectures.

II. Output voltage variation

For a pipeline ADC with input and output range of $2V_{ref}$, the residue transfer characteristics of a single stage is shown in Fig. 1. The circles around the comparator trip point depict the possible variation of the output voltage from its nominal value due to the process variations. The circles are representations of the movement of the output voltage at the discontinuities of the transfer characteristics in the neighborhood of its nominal value but these regions are not necessarily circular in nature. For proper operation of the pipeline, the total output voltage deviation from its nominal value should be less, in a statistical sense, than the available over-range protection otherwise it will cause non recoverable errors to occur.

A. Charge-Redistribution Switched Capacitor Amplifier (CR-SC Amp)

For the switched capacitor (SC) amplifier shown in Fig. 2, where Φ_1 and Φ_2 are the complimentary non-overlapping

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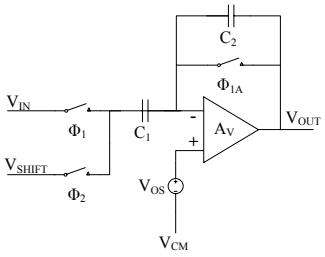

Fig. 2. Charge-redistribution switched capacitor amplifier (MDAC)

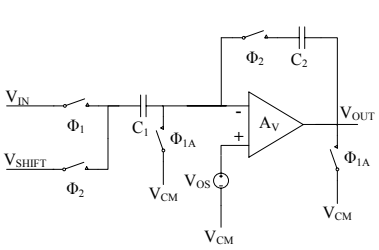

Fig. 3. Modified charge-redistribution switched capacitor amplifier (MDAC)

clocks and Φ_{1A} is the advanced version of Φ_1, the output voltage at the end of phase Φ_2 is

$$V_{OUT} = m[V_{IN} - V_{SHIFT}] + V_{CM} + V_{OS} \tag{1}$$

where V_{IN} is the input of the SC amplifier, V_{CM} is the amplifier common mode output voltage, V_{OS} is the amplifier offset which is modeled as a Gaussian random process with zero mean and $\sigma_{Amp_{OS}}$ as standard deviation, V_{SHIFT} is the output of a sub-DAC and m is the gain of the SC amplifier give by

$$m = \frac{C_1}{C_2} \tag{2}$$

Due to process variations m, V_{IN} and V_{SHIFT} can be written as

$$\begin{aligned} m = m_n + m_r, \;\; V_{IN} &= V_{IN,n} + V_{IN,r} \\ V_{SHIFT} &= V_{SHIFT,n} + V_{SHIFT,r} \end{aligned} \tag{3}$$

where the 'n' terms in (3) represent nominal values and the 'r' terms are the random components of the respective parameter. The random components are modeled as Gaussian random processes with zero mean, i.e. $m_r \sim N(0, \sigma_m^2)$, $V_{IN,r} \sim N(0, \sigma_{V_{IN}}^2)$ and $V_{SHIFT,r} \sim N(0, \sigma_{V_{SHIFT}}^2)$, where the σs' are the standard deviations of the respective random processes. From (1) and (3) and neglecting the product of two random terms

$$V_{OUT} = V_{OUT,n} + V_{OUT,r} \tag{4}$$

where

$$\begin{aligned} V_{OUT,n} &= m_n[V_{IN,n} - V_{SHIFT,n}] + V_{CM} \\ V_{OUT,r} &\simeq m_n[V_{IN,r} - V_{SHIFT,r}] + V_{OS} \\ &\quad + m_r[V_{IN,n} - V_{SHIFT,n}] \end{aligned} \tag{5}$$

Here V_{OUT} is modeled as linear combination of the Gaussian random processes of V_{IN}, V_{SHIFT}, m and V_{OS} resulting in a Gaussian random process with mean $V_{OUT,n}$ and the variance given by

$$\begin{aligned} \sigma_{V_{OUT}}^2 &= m_n^2(\sigma_{V_{IN}}^2 + \sigma_{V_{SHIFT}}^2) + \sigma_{Amp_{OS}}^2 \\ &\quad + \sigma_m^2(V_{IN,n} - V_{SHIFT,n})^2 \end{aligned} \tag{6}$$

Correspondingly, the capacitors can be modeled as a combination of a nominal component and a random component, i.e.

$$C_i = C_{i,n} + C_{i,r} \qquad \forall\ i = 1, 2 \tag{7}$$

It thus follow from (2) and (3) that

$$m_n = \frac{C_{1,n}}{C_{2,n}} \qquad \& \qquad m_r \simeq \frac{C_{1,n}}{C_{2,n}}\left[\frac{C_{1,r}}{C_{1,n}} - \frac{C_{2,r}}{C_{2,n}}\right] \tag{8}$$

Hence, the variance of the slope is given by

$$\sigma_m^2 = m_n^2\left[\sigma^2_{\frac{C_{1,r}}{C_{1,n}}} + \sigma^2_{\frac{C_{2,r}}{C_{2,n}}}\right] = 2m_n^2\sigma_C^2 \tag{9}$$

where σ_C is the normalized capacitor's standard deviation. From (5), (6) and (9)

$$\begin{aligned} \sigma_{V_{OUT}}^2 &= m_n^2(\sigma_{V_{IN}}^2 + \sigma_{V_{SHIFT}}^2) + \sigma_{Amp_{OS}}^2 \\ &\quad + 2(V_{OUT,n} - V_{CM})^2\sigma_C^2 \end{aligned} \tag{10}$$

The errors present in V_{SHIFT} can be minimized by using calibration techniques in the sub-DAC [7]. If this is done, (10) reduces to

$$\sigma_{V_{OUT}}^2 = m_n^2\sigma_{V_{IN}}^2 + \sigma_{Amp_{OS}}^2 + 2(V_{OUT,n} - V_{CM})^2\sigma_C^2 \tag{11}$$

The maximum deviation of the output voltage from its nominal value will occur at the comparator trip point (TP), therefore, the errors present in V_{IN} will be caused mainly by the comparator offset. The variance of the output voltage at TP can be written as

$$\begin{aligned} \sigma_{V_{OUT,TP}}^2 &= m_n^2\sigma_{Comp_{OS}}^2 + \sigma_{Amp_{OS}}^2 \\ &\quad + 2(V_{OUT,TP,n} - V_{CM})^2\sigma_C^2 \end{aligned} \tag{12}$$

where $\sigma_{Comp_{OS}}$ is the comparator offset's standard deviation and $V_{OUT,TP,n}$ is the nominal output voltage at the comparator trip point.

For faster amplifier settling, Fig. 2 can be modified as shown in Fig. 3. For this structure, the variance of V_{OUT} at the TP is given by

$$\begin{aligned} \sigma_{V_{OUT,TP}}^2 &= m_n^2[\sigma_{Comp_{OS}}^2 + \sigma_{V_{SHIFT}}^2] \\ &\quad + 2(V_{OUT,TP,n} - V_{CM})^2\sigma_C^2 \\ &\quad + (1 + m_n)^2\sigma_{Amp_{OS}}^2 \end{aligned} \tag{13}$$

B. Flip-Around Switched Capacitor Amplifier (FA-SC Amp)

For a flip around SC amplifier as shown in Fig. 4, the output voltage at the end of phase Φ_2 is given by

$$V_{OUT} = (1 + m)V_{IN} - mV_{SHIFT} \tag{14}$$

where m is defined as in (2) and $(1+m)$ is the gain of the SC amplifier. Again considering m, V_{IN} and V_{SHIFT} as Gaussian random processes, (14) can be written as

$$V_{OUT} = V_{OUT,n} + V_{OUT,r} \tag{15}$$

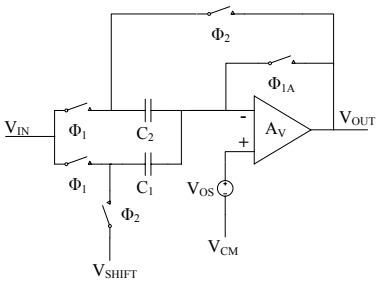

Fig. 4. Flip-around switched capacitor amplifier (MDAC)

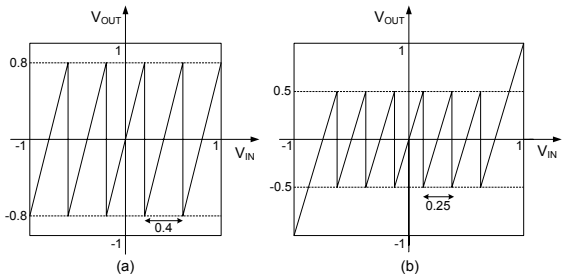

Fig. 5. Single stage pipeline ADC transfer curve (a) 4 comparators/stage (b) 6 comparators/stage

where

$$\begin{aligned} V_{OUT,n} &= (1+m_n)V_{IN,n} - m_n V_{SHIFT,n} \\ V_{OUT,r} &= (1+m_n)V_{IN,r} - m_n V_{SHIFT,r} \\ &\quad + m_r(V_{IN,n} - V_{SHIFT,n}) \end{aligned} \tag{16}$$

and the variance of the output voltage is

$$\begin{aligned} \sigma^2_{V_{OUT}} &= (1+m_n)^2\sigma^2_{V_{IN}} + m_n^2\sigma^2_{V_{SHIFT}} \\ &\quad + (V_{IN,n} - V_{SHIFT,n})^2\sigma^2_m \end{aligned} \tag{17}$$

From (8), (9), (16) and using calibration in sub-DAC, the variance of the maximum output voltage deviation at the TP can be rewritten as

$$\begin{aligned} \sigma^2_{V_{OUT,TP}} &= (1+m_n)^2\sigma^2_{Comp_{OS}} \\ &\quad + 2(V_{OUT,TP,n} - V_{Comp,TP,n})^2\sigma^2_C \end{aligned} \tag{18}$$

where $V_{Comp,TP,n}$ is the nominal comparator TP voltage level. From (18), the output voltage at the trip point is a function of the comparator TP, whereas, in the previous case of CR-SC amp it is independent of the comparator TP.

For faster amplifier settling, a similar modification as that of the previous section on modified CR-SC amp, Fig. 3, can be made, and the variance of the output voltage at the comparator TP is given by

$$\begin{aligned} \sigma^2_{V_{OUT,TP}} &= (1+m_n)^2[\sigma^2_{Comp_{OS}} + \sigma^2_{Amp_{OS}}] \\ &\quad + 2(V_{OUT,TP,n} - V_{Comp,TP,n})^2\sigma^2_C \end{aligned} \tag{19}$$

III. Results

Two scenarios are considered for evaluating the effects of process variation on the output voltage at the comparator TP. In the first case the effect of comparator offset has been ignored, whereas, in the second case its contribution is taken into account. Both cases are studied for SC amp with a closed loop gain of 4 and 4 or 6 comparators per stage in a pipeline data converter. Typical transfer curves with 4 and 6 comparator per stage are shown in Fig. 5 for a reference voltage of ±1V. For a 4 comparators per stage structure, $V_{OUT,TP,n} = \pm 0.8V$, $V_{Comp,TP,n} = \{\pm 0.2V, \pm 0.6V\}$ and the available over-range is assumed to be 0.2V, whereas, for a 6 comparators per stage structure, $V_{OUT,TP,n} = \pm 0.5V$, $V_{Comp,TP,n} = \{\pm 0.125V, \pm 0.375V, \pm 0.625V\}$ and the available over-range is assumed to be 0.5V. In both cases the $V_{CM} = 0$V.

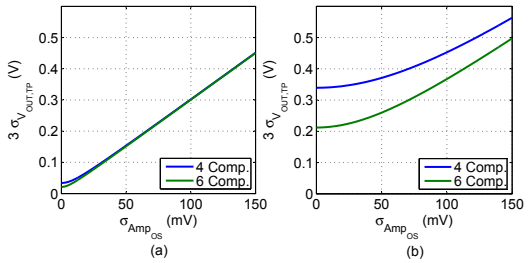

Fig. 6. $3\sigma_{V_{OUT,TP}}$ vs. $\sigma_{Amp_{OS}}$ for a CR-SC amp (a) $\sigma_C = 0.01$ (b) $\sigma_C = 0.1$

For the CR-SC amp of Fig. 2, the standard deviation of the output voltage at all transition points is the same. Neglecting the comparator offset contribution term in (12), a plot of the 3σ value of the output voltage at the 4 or 6 transition points (i.e. 99.87% of output voltages lies with in the 3σ range around its nominal value) vs. amplifier offset standard deviation at the comparator trip point is plotted in Fig. 6 for two different values of σ_C. A corresponding plot of the 3σ values of the output voltage at the transition points vs. comparator offset standard deviation for (12) is plotted in Fig. 7 for a fixed 10 mV of amplifier offset standard deviation. In both cases, with or without comparator offset, the 6 comparators per stage pipeline structure has a sufficiently lower output voltage variation compared to that of the 4 comparators per stage pipeline even though for practical applications with $\sigma_C = 0.01$, there is not much difference between the 4 and 6 comparators per stage structures. If offset cancellation techniques are not used, the comparator offset contribution will dominate the overall

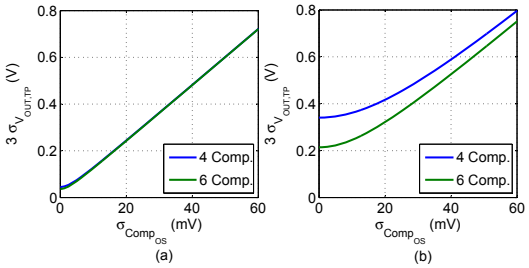

Fig. 7. $3\sigma_{V_{OUT,TP}}$ vs. $\sigma_{Comp_{OS}}$ for a CR-SC amp with $\sigma_{Amp_{OS}} = 10$ mV (a) $\sigma_C = 0.01$ (b) $\sigma_C = 0.1$

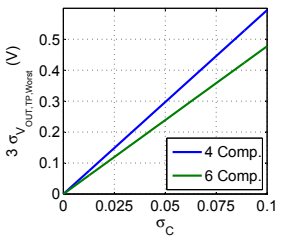

Fig. 8. $3\sigma_{V_{OUT,TP,Worst}}$ vs. σ_C for a FA-SC amp

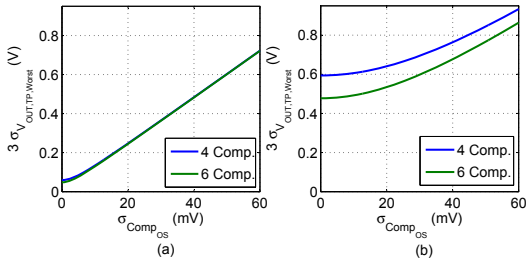

Fig. 9. $3\sigma_{V_{OUT,TP,Worst}}$ vs. $\sigma_{Comp_{OS}}$ for a FA-SC amp (a) $\sigma_C = 0.01$ (b) $\sigma_C = 0.1$

3σ variation of the output voltage at the transition points.

Similar results have been obtained for the FA-SC amp of Fig. 4. If the comparator offset error term is neglected in (18), then the 3σ output voltage at the transition points will be directly proportional to σ_C as well as a function of comparator TP value, hence a worst case output voltage plot of $3\sigma_{V_{OUT,TP}}$ vs. σ_C is shown in Fig. 8 which occurs at the upper transition point of the first comparator and at the bottom transition point of the last comparator. A plot of worst case 3σ output voltage vs. comparator offset standard deviation is shown in Fig. 9 for (18). Again, if offset cancellation techniques are not used, the comparator offset term dominates the overall output voltage deviation for the FA-SC amp.

Table I summarizes the comparison between the CR-SC and FA-SC structures for $\sigma_C = 0.01$ and $\sigma_{Amp_{OS}} = 10$ mV without offset cancellation techniques. The $\sigma_{Comp_{OS}}|_{max}$ is the worst case comparator offset standard deviation for the maximum allowable over-range protection. Table I confirms the well known concepts that over-range protection of the 6 comparator per stage structure is substantially larger than that of the 4 comparator structure and that the offset contribution dominates the over-range protection requirements for a typical process. The small differences in the variance suggest that there is little substantial difference in over-range performance between the CR-SC and the FA-SC structures.

However, if offset cancellation techniques are used for both the amplifier and the comparators, substantially different conclusions can be drawn. With $\sigma_C = 0.01$, the worst case 3σ over-range voltage variations for the CR-SC amp are 34mV and 21mV for the 4 and 6 comparators per stage structures respectively, whereas for the FA-SC amp, the corresponding values are 59mV and 48mV. The worst case 3σ over-range voltage variation values suggest that the CR-SC amp is substantially better than the FA-SC amp and there is little justification to go beyond a 4 comparators per stage structure. For high resolution levels, the $\frac{KT}{C}$ noise and power benefits of FA-SC structure may over shadow the over-range protection advantages of the CR-SC structure [8].

TABLE I
COMPARISON BETWEEN CR-SC AND FA-SC STRUCTURES WITHOUT OFFSET CANCELLATION TECHNIQUES

Case	$Maximum\ allowable$	$\sigma_{Comp_{OS}}\|_{max}$(mV)	
	$over-range\ protection$	CR	FA
4 comp./stage	0.2 V	16.23	15.91
6 comp./stage	0.5 V	41.55	41.47

IV. CONCLUSION

For the inter-stage amplifiers in pipeline ADCs, closed form expressions of the three sigma variation in the over-range voltage levels have been derived. If no offset cancellation techiques are used, offsets dominate the over-range protection requirements and the 6 comparator per stage structure may be required to provide adequate over-range protection. Without offset cancellation techniques, little substantial difference was found between the CR-SC and the FA-SC structures. However, if offset cancellation techniques are used, the CR-SC amp was substantially better and there is little justification to going beyond 4 comparator per stage structure. For higher resolution levels, capacitance noise and power issue favor the FA-SC amp over the CR-SC amp even if offset cancellation techinques are used.

V. ACKNOWLEDGEMENT

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