New Over-range Protection Scheme in Pipelined Data Converters

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***Abstract*—Existing approaches for the design of interstage switched-capacitor amplifiers used in pipelined data converters have evolved following the notion that there are firm limits on input range and output range of the amplifier. In this work, it is recognized that the limits on signal swing are not dictated by binary and somewhat arbitrary boundaries but rather by increasing levels of distortion with signal swing. The concept of defining a series of signal swing windows based on the degree of distortion present in the gain stage amplifier is formalized. A set of "critical points" on the transfer characteristics are identified that are useful for determining robustness of any given over-range protection circuit. In contrast to existing approaches where the amplifier may be under-designed or over-designed in an attempt to meet a fixed signal swing window requirement, the designer can select signal swing windows to provide acceptable levels of distortion. Following this approach, a new over-range protection scheme is developed which ensures that all residues of a given stage are mapped back into an acceptable distortion window of the following stage**

I. INTRODUCTION

The presence of uncompensated nonlinearities in the signal path can significantly degrade the performance of a pipeline analog to digital converter (ADC). Few of these nonlinearities contribute to recoverable errors whereas other results in non-recoverable errors. Recoverable errors may cause an error in the overall interpretation of the digital output code, but sufficient information still exists in the digital output for correct interpretation. In contrast, non-recoverable errors cause a loss of information and sufficient information does not exist for the recovery. Both non-recovered recoverable errors and non-recoverable errors limit the performance of most pipeline data converters. Excessive growth in the residue path caused by nonlinearities will cause such recoverable or non-recoverable errors. In particular, the concern is that the residue can cause the output of one or more amplifier stages to saturate. These excessive signals are often termed over-range signals. Modifications of the basic amplifier structure are included in some pipeline ADCs [1-4] to limit the over-range signals. The circuits that provide this over-range protection are generally termed an over-range protection circuits.

Common practice for over-range protection circuits is to use the same signal conversion range for all the stages. Moreover, no distinction is made between the signal conversion range and signal saturation range [1-4]. This results in excessive design requirements of a pipeline ADC. To overcome this problem, a series of signal swing windows based on the degree of distortion present in the gain stage amplifier is formalized. A set of "critical points" on the transfer characteristics are identified that are useful for determining robustness of any given over-range protection circuit. A new over-range protection scheme based on these signal swing windows and critical points will be investigated to achieve a relaxed pipeline ADC design.

II. LINEARITY AND OVER-RANGING

A. Operating Windows

Consider the signal path from the input to the output of a stage of pipeline ADC as depicted in Fig. 1. The two-dimensional input/output plane in Fig. 2 shows the normal input and output operating range of the amplifiers for an arbitrary amplifier stage relative to the reference range of the ADC. In Fig. 2, V_{DD} and V_{SS} represent the upper and lower supply voltages. It is generally assumed that it is necessary to keep the input and output in a rectangular window positioned on $V_{in}=V_{out}$ line. This window is defined as Data Converter Reference Window (DCRW) and it is the inner most rectangle shown in Fig.2. For convenience, it will be assumed that the position of the DCRW is the same for all stages. The specified input range of the ADC corresponds to the projection of the DCRW onto the V_{in} axis. Another important window can be defined as Residue Amplifier Saturation Window (RASW). This window is determined by few devices internal to the op-amp leaving the desired region of operation and causing amplifier to saturate. If the signal is out of the RASW range, serious non-recoverable distortion or clipping will result in the amplifier. Besides, there exists another window in between DCRW and RASW, Residue Amplifier Distortion Window (RADW). Outside this RADW

This work is supported in part by the National Science Foundation and Semiconductor Research Corporation.

0-7803-9197-7/05/$20.00 © 2005 IEEE.

window, distortion or nonlinearities becomes larger than the tolerable limit for the overall feedback amplifier (not just the operational amplifier) for a given pipeline stage. Within the RADW and RASW, the distortion can actually be reduced by calibration. The RADW is depicted as a rectangle in Fig. 2, but in actuality, this may be arbitrarily-shaped. This distortion bound has not been sufficiently studied and has not been considered for the design issues.

In most reported designs, no distinction is made between the DCRW and the RASW [1-4]. For an n-stage pipeline ADC, it is generally further assumed that it is necessary to keep the input and output signals inside the DCRW for all stages. This type of overage-protection scheme is far from necessary. In what follows, we propose linearity and over range protection method to relax the requirement based on the discussion of the concept of windows.

Fig. 3 shows the combined effects of several error sources in one of the first (n-2) stages of a pipeline ADC. Since the last stage of a pipeline ADC comprised of only a comparator, the $(n-1)^{th}$ stage output should be bounded by DCRW otherwise the last stage error can not be corrected. This is equivalent to having over-range protection on the $(n-1)^{th}$ stage. Whereas, for the first (n-2) stages, the input and output are only required to lie within the RADW window. In case (a), the amplifier is driven to the RADW. In case (b), modest distortion will occur as the output leaves the RADW window. This will cause degradation in the performance of the pipeline. Actually, this type of error may be correctable with the appropriate nonlinear error correction algorithm but very little is available in the literature on these corrections. The third situation, case (c), corresponds to impinging on the RASW. This will cause serious distortion and non-recoverable errors in the pipeline.

To correctly convert the input voltage, a less stringent but still sufficient condition would be to have linearity protection circuitry on the amplifiers of the first (n-2) stages and over-range protection on the $(n-1)^{th}$ stage, i.e.:

1. The input and output signals for the first (n-2) stages must lie within the RADW
2. The output range for the $(n-1)^{th}$ stage must lie within the DCRW

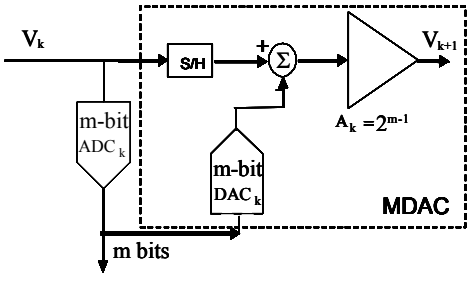


Fig. 1 Block diagram of k^{th} stage of pipeline ADC

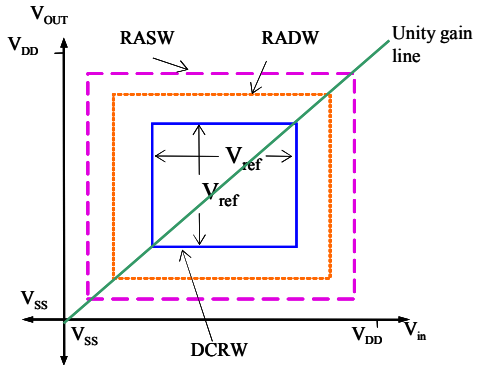


Fig. 2 Input/Output range of amplifier stage in pipelined ADC

These conditions must be maintained for all specified input signals and throughout all process and temperature variations. It should be noted that the issue of over range plays no role on any stage except the output of the $(n-1)^{th}$ stage provided that the previous stages amplifier remain linear. Of course, many designers use over-ranging to maintain linearity on intermediate stages as well. One of the major reasons that many existing data converters fail to meet static linearity constraints is associated with improper sizing of the DCRW and the RADW. This may be a challenge because creating a large RADW, specifically large enough to contain the DCRW, can be difficult.

B. Critical Points

Some points on the transfer characteristics of a residue amplifier that are particularly indicative of non-idealities in the pipeline stage can be defined as Critical Points (CP). These points must be constrained to prevent the amplifier from saturating to avoid non-recoverable errors. The vulnerability of the amplifier is due to the fact that the non-idealities in the amplifier cause these points to move. The movement of these points from their ideal locations can be an indicator of degradation in performance of the pipeline. For a 1-bit per stage pipeline, the critical points are shown by the circles in Fig. 4. The radius of the circles will be used to identify the worst-case deviation of these critical points from their desired values due to non-idealities in the circuit. These CPs can be further classified as Internal Critical Points (ICP) or Boundary Critical Points (BCP). The ICPs are the points where discontinuities of the ideal transfer characteristic occur, which are close to or beyond the DCRW, e.g. points B in Fig. 4. The BCPs are the points corresponding to the minimum and maximum input of a stage which are close to or beyond a horizontal DCRW boundary, e.g. points D in Fig. 4. The points with the worst case deviation that remain within the DCRW will not be termed as CPs.

BCPs that are near a vertical edge of DCRW are problematic for two reasons. First, if the output of the previous stage, i.e. the input of the present stage, extends beyond the DCRW boundary, the output of this stage may go beyond the RADW. Second, the movement of these

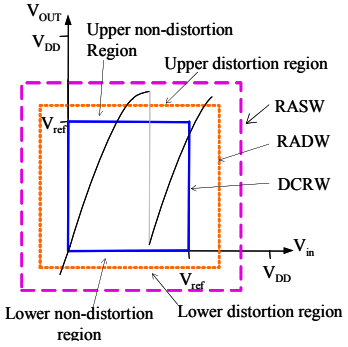
points can also affect both the output range of the present stage and the input of the next stage. The ICPs affect the output range of the stage and may also affect the distortion.

In the next section we will identify a new window based on CPs and propose an over-range protection scheme where the CPs will not cause problems.

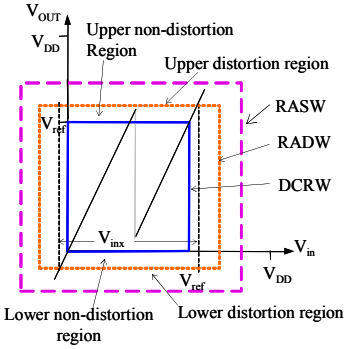
III. Strategies for Providing Over-Range Protection

In this discussion we will focus on the operation of a pipeline stage in the range of the DCRW. Fig. 5 shows the transfer characteristics of an ideal 1-bit/stage architecture including the unity gain line. It can be observed that the unity gain line crosses the transfer characteristics of the amplifier at the two corners of the DCRW and there are two ICPs and BCPs. This does not necessarily suggest that this architecture should be avoided, but rather indicates that the accurate control of the variation will be essential for good yield. Good yield will be increasingly difficult to achieve as the resolution of the ADC increases.

The previous examples provided insight into the properties that are needed to develop a new linearity and over range protection scheme, which is termed as new over-range protection scheme.



(a)



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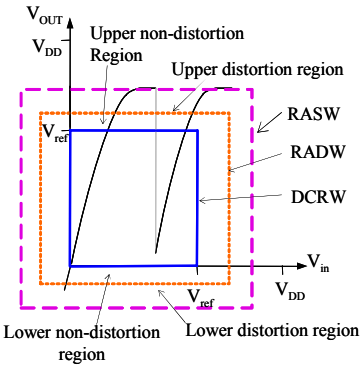

(c)

Fig. 3 Effects of driving residue amplifier beyond the DCRW

A. Critical Window

The concept of critical window (CW) based on the DCRW, RADW and the transfer characteristic is defined below.

Fig.6 shows CW for 3 different cases. The 1st vertical CW edge is defined by the intersection of 1st transfer curve segment with that of the lower horizontal line of the DCRW, whereas, for 2nd vertical CW edge is defined by last transfer curve segment with that of the upper horizontal line of the DCRW. The horizontal lines of the CW are same as those of the DCRW. For instance, if we have 2 BCPs, e.g., case (b), the CW will be a subset of DCRW. For case I and case II, the RADW is outside of CW. For case III, part of RADW is inside of CW, and a new critical window (NCW) is defined by the innermost closure of these two windows.

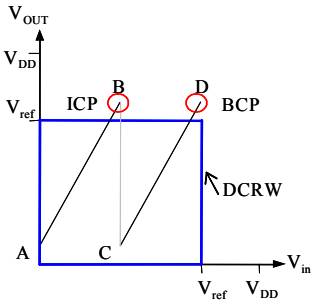

Fig. 4 Critical points for one-bit per stage amplifier

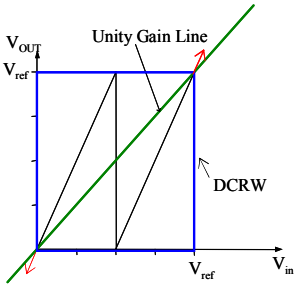

Fig. 5 Single bit/stage structure showing over-range sensitive region

For simplicity, we will assume that the DCRW is the same for all the stages, but the RADW can be different from stage to stage. It is also assumed that CW can be inside of the DCRW or outside of the DCRW. The detailed design strategy for new over-range protection scheme based on the signal swing windows and CPs is shown in Fig.7, along with the linearity and over-range protection scheme discussed in II-A.

The main idea of this strategy is to insure the residue of each stage is mapped back into an acceptable distortion window of the following stage. For example, if stage k is of case I or II and stage (k+1) is of case II, and if there is any CP present in stage k, it would result in the output of stage k to exceed the CW_k. This will cause signal to become larger than the input range of the stage (k+1) and cause non recoverable errors.

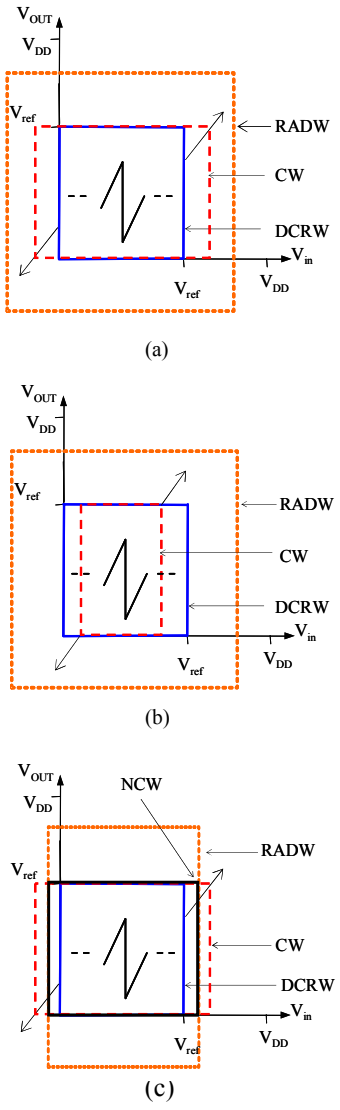

Fig. 6 (a) case I (b) case II (c) case III for CW

IV. CONLUSIONS

A new scheme for over-range protection for a pipeline ADC was proposed. Concepts of a series of signal swing windows, i.e., Data Converter Reference Window (DCRW), Residue Amplifier Saturation Window (RASW) and Residue Amplifier Distortion Window (RADW) were formalized. A set of critical points (Cps), i.e. Boundary Critical Points (BCP) and Internal Critical Points (ICP) were identified based on the signal swing windows. In contrast to existing approaches which attempt to meet a fixed signal swing window, this new scheme provides flexibility for designers to choose different signal swing windows. A Critical Window (CW) and New Critical Window (NCW) based on different combinations of the above mentioned windows and CPs were identified. A design strategy for the new over-range protection scheme was developed and shown in the flow chart.

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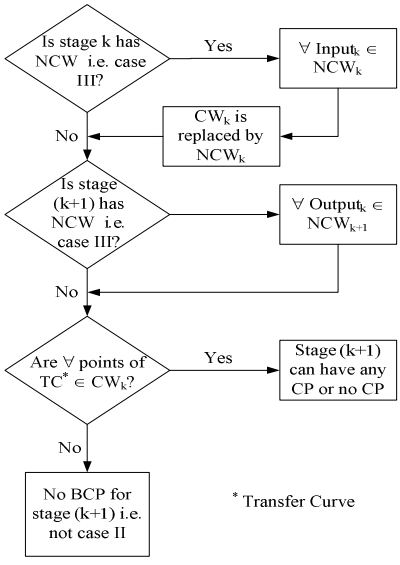

Fig. 7 Flow chart for new over-range protection scheme