High-Performance ADC Linearity Test Using Low-Precision Signals in Non-Stationary Environments

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Abstract

This work describes a linearity test strategy for ADCs that uses stimuli with precision much lower than the ADC resolution and tolerates environment nonstationarity. This approach can be applied to testing ADCs of very high performance, such as 16-bit or higher resolutions and more than 1 MSPS sampling rates, to which there is hardly a well-established solution for full-code test. Simulation and experimental results show that a 16-bit ADC can be tested to 1-LSB accuracy by using input signals of 7-bit linearity in an environment with more than 100 ppm per minute nonstationarity. The proposed method can also help control the cost of ADC production test, extend the test coverage and enable built-in self-test and test-based self-calibration.

1. Introduction

The analog-to-digital converter (ADC) is one of the world's largest volume analog and mixed-signal (AMS) integrated circuit products and is viewed as one of the system drivers for AMS chip design [1]. Linearity test of high-performance ADCs is a well-known important and challenging problem, and the testing cost has essential meaning to the manufacturers because of the high volume. The ADC testing capability is mainly determined by three enabling technologies: fast data capture, precision clock timing and linear stimulus generation [2]. The bottle neck in testing of next generation high-performance ADCs is the linear signal generation, as the present state-of-the-art technologies on clock timing and data capture can handle the up coming ADCs. The quasi-static linearity of ADCs is conventionally tested with the histogram approach by using a ramp or sine wave input signal, with linearity at least one decade better than the specification of the ADC under test [3-5]. The input linearity requirement makes the test of high-resolution ADCs an increasingly challenging problem, since the resolution of ADCs is continuously going up along with the emerging demand for high-performance applications in communications, imaging, and industrial controls [6, 7].

A full-code histogram test for a high-resolution ADC requires a large number of samples, which implies long and expensive test time [8]. In some linearity test practices, only a reduced set of codes are tested for to control the test cost. Due to long testing time, the nonstationarity of the test environment will cause errors in linearity testing as well and becomes a problem when the resolution of ADCs under test increases. A highly-linear signal source does not necessarily have good stationarity and vice versa [12]. However, there is not much discussion about the stationarity issue in existing literatures, although the industry always spends efforts on designing and maintaining a stationary test environment. Because of the above facts, there is a lack of widely-adopted cost-effective approaches for testing high-performance ADCs that are pushing the edge of current technologies. However, a precision linearity test can help validate the design of a high-performance ADC, reduce the number of wasted parts, and enable the calibration, so it is necessary to develop methods for accurately characterizing linearity of high-resolution high-speed ADCs.

In addition to the production test approach for ADC linearity by using analog and mixed-signal automated test equipments (ATEs), other test approaches have been developed for measurement of ADC linearity. Max proposed a ramp test method with a relaxed requirement on input resolution [9]. A built-in self-test (BIST) method was introduced in [10]. An on-chip ramp generator was designed and achieved 11-bit linearity [11]. However, for testing ADCs with 16-bit or higher resolutions by using the conventional histogram method, more than 20-bit linear signals are needed. To the best of the authors knowledge, none of the existing on-chip signal generators can fulfill this requirement. This is why there is little industrial adoption of BIST techniques.

In a previous work, the authors introduced an ADC test algorithm using nonlinear signals with stimulus error identification and removal (SEIR) at ITC 2003 [12]. In this paper, the authors will describe a test strategy that can

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eliminate the effect of environment nonstationarity on the test results for the purpose of precision ADC testing. The combination of the above two methods will provide a solution to production test of high-performance ADCs, utilizing low-linearity stimuli in a non-stationary environment. Simulation and experimental results show that the proposed technique can accurately test 16-bit ADCs using 7-bit linear signals in an environment with more than 100 ppm per minute nonstationarity. Since the combined strategy allows using nonlinear but fast signals in test, it is applicable to ADCs with a 16-bit or higher resolution and a sampling rate of more than 1 MSPS, which do not have a practical full-code test solution because of the prohibitively long test time required for conventional methods. It can also work in a test environment with stability worse than that of the application environment, but still provide accurate test results. Additionally, this approach can help reduce the test cost if combined with current solutions and enable testing of a wider range of specifications at a manageable cost.

2. Precision ADC Test with SEIR

This section will briefly review the SEIR algorithm. More details can be found in [12]. An n-bit ADC has $N=2^n$ distinct output codes. The static input-output characteristic of the ADC can be modeled as

$$D(x)=\begin{cases}0, & x\le T_0,\\ k, & T_{k-1}<x\le T_k,\\ N-1, & T_{N-2}<x,\end{cases} \tag{1}$$

where D is the output code, x is the input voltage, and T_k is the k-th transition level. One of the most widely used ADC linearity metrics is the integral non-linearity (*INL*). For code k, INL_k is defined as

$$INL_k=\frac{T_k-T_0}{T_{N-2}-T_0}(N-2)-k. \tag{2}$$

The *INL* is the maximum magnitude of INL_k's,

$$INL=\max_k\{|\,INL_k\,|\}. \tag{3}$$

A larger *INL* indicates an ADC is less linear.

A real ramp signal can be modeled as

$$x(t)=x_{os}+\eta t+F(t), \tag{4}$$

where x_{os} is a DC offset, ηt is a linear component, and $F(t)$ is a nonlinear component. Without affecting the linearity test results, (4) can be normalized and written as

$$x(t)=t+F(t). \tag{5}$$

Transition time t_k is defined to be the time instance at which the ramp signal is equal to the k^{th} transition level,

$$T_k=x(t_k). \tag{6}$$

If $F(t)$ is known and t_k's are measured, T_k, INL_k and ADC linearity can be calculated by using equations above. However, the input nonlinearity $F(t)$ is usually unknown. To identify this nonlinearity, it is expanded over a set of M basis function $F_j(t)$'s with unknown coefficient a_j's as

$$F(t)=\sum_{j=1}^{M}a_jF_j(t). \tag{7}$$

The SEIR algorithm uses two ramp signals with a constant offset α to test an ADC,

$$x_1(t)=t+F(t) \tag{8}$$

and $$x_2(t)=x_1(t)-\alpha. \tag{9}$$

By feeding the two ramps into an ADC under test, we can collect two sets of histogram data $H_{k,1}$'s and $H_{k,2}$'s and get two estimates for a transition level T_k,

$$\hat{T}_{k,1}=\hat{t}_{k,1}+\sum_{j=1}^{M}a_jF_j(\hat{t}_{k,1})=T_k+e_{k,1} \tag{10}$$

and $$\hat{T}_{k,2}=\hat{t}_{k,2}+\sum_{j=1}^{M}a_jF_j(\hat{t}_{k,2})-\alpha=T_k+e_{k,2}, \tag{11}$$

where $e_{k,1}$ and $e_{k,2}$ are estimation errors and transition times are estimated from the histogram data $H_{k,1}$'s and $H_{k,2}$'s as

$$\hat{t}_{k,1}=\sum_{i=0}^{k}H_{i,1}\Big/\sum_{i=0}^{N-1}H_{i,1} \tag{12}$$

and $$\hat{t}_{k,2}=\sum_{i=0}^{k}H_{i,2}\Big/\sum_{i=0}^{N-1}H_{i,2}. \tag{13}$$

Although the estimates in (10) and (11) are undetermined since a_j's are unknown, they are supposed to be the same for one transition level. It can be observed that there are totally N-1 such pairs for k taking different values in (10) and (11), but there are only M+1 unknown variables (M a_j's and α), while N is usually much larger than M. For example, N is equal to 16384 for a 14-bit ADC and M equal to 30 is usually more than enough for an accurate representation of $F(t)$. Another observation is that (10) and (11) are linear in a_j's and α. Therefore, we can robustly estimate the unknowns by using the standard least squares (LS) method to minimize the error energy as

$$\{\hat{a}_j's,\hat{\alpha}\}=\arg\min\left\{\sum_{k=0}^{N-2}\left[\hat{t}_{k,1}-\hat{t}_{k,2}+\sum_{j=1}^{M}a_j\left(F_j(\hat{t}_{k,1})-F_j(\hat{t}_{k,2})\right)+\alpha\right]^2\right\}. \tag{14}$$

With the knowledge of ramp nonlinearity a_j's, we can remove their effects on histogram data and accurately identify the transition level as

$$\hat{T}_k = \hat{t}_{k,1} + \sum_{j=1}^{M} \hat{a}_j F_j(\hat{t}_{k,1}). \quad (15)$$

Thus ADC's linearity performance can be estimated by applying (2) and (3).

The SEIR algorithm can be summarized into the following steps.

- Generate a ramp and use it to excite the ADC;
- Collect N histogram counts, $H_{k,1}$, for the ramp;
- Generate the same ramp, shift it by a constant offset, and use the shifted ramp to excite the ADC;
- Collect another set of N histogram counts, $H_{k,2}$, for the second ramp;
- Generate two estimates for each of the transition levels, T_k, using M parameters, a_j, that characterizes input nonlinearity;
- Use the LS method to identify the M parameters by minimizing the difference between the estimates associated with the same transition level;
- Estimate T_k using the identified input nonlinearity;
- Identify ADC's linearity performance based on the transition level estimation.

Figure 1 gives an example where a 14-bit ADC is under test by using 16 parameters for input nonlinearity identification.

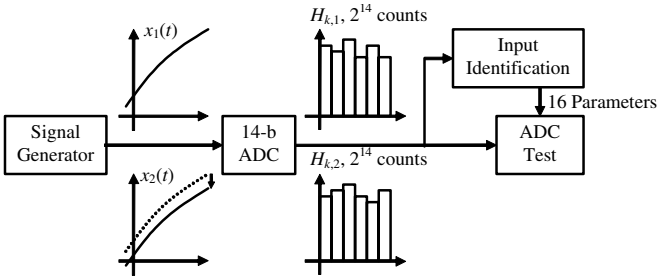


Figure 1 Test of a 14-bit ADC using SEIR algorithm.

The SEIR algorithm can use nonlinear signals for testing ADCs, with accuracy comparable to that of conventional methods using highly linear signals. Therefore it is promising for cost-effective production test and built-in self-test of precision ADCs.

3. Test in Non-Stationary Environment

Although the ramp signals can be highly nonlinear in the SEIR algorithm, it is important that the two signals have the same nonlinearity and the offset between the two signals be constant. For high precision-ADC testing, the test environment can cause the offset to change by a significant amount over the test duration due to many non-stationary mechanisms. One example is the reference voltage drifting. Although noise effects in the offset can be averaged out by the LS method, if the offset is changing as a function of time, it will introduce errors into input identification and consequently generate inaccurate ADC test results. This section will first discuss the effect of a non-constant offset on SEIR test results and then introduce a test approach that can effectively reduce the environment-related errors in the offset, which makes the SEIR algorithm robust to the test environment nonstationarity.

3.1. Effects of non-constant offset

Let the offset between nonlinear ramp signals be time dependent as

$$x_1(t) - x_2(t) = \alpha + N(t), \quad (16)$$

where α is a nominal constant shift and $N(t)$ is the offset error introduced by the test environment nonstationarity. Equation (10) and (11) should be rewritten as

$$\hat{T}_{k,1} = \hat{t}_{k,1} + \sum_{j=1}^{M} a_j F_j(\hat{t}_{k,1}) = T_k + e_{k,1} \quad (17)$$

and $$\hat{T}_{k,2} = \hat{t}_{k,2} + \sum_{j=1}^{M} a_j F_j(\hat{t}_{k,2}) - \alpha - N(\hat{t}_{k,2}) = T_k + e_{k,2}, \quad (18)$$

where transition times are estimated from the histogram data $H_{k,1}$'s and $H_{k,2}$'s as before, and a_j, α, and $N(t)$ are unknown. In this case, if we still assume the offset be constant and apply the LS method as in (14), we get another estimate of coefficients of basis functions,

$$\{\hat{a}_j^*\text{'s}, \hat{\alpha}^*\} = \arg\min\{\sum_{k=0}^{N-2} [\hat{t}_{k,1} - \hat{t}_{k,2} + \sum_{j=1}^{M} a_j\left(F_j(\hat{t}_{k,1}) - F_j(\hat{t}_{k,2})\right) + \alpha]^2\} \quad (19)$$

However, the estimates with "*" in (19) are not equal to their true values because $N(t)$ introduces errors in input identification, which can be seen from the following,

$$\sum_{j=1}^{M} \hat{a}_j^*\left(F_j(\hat{t}_{k,1}) - F_j(\hat{t}_{k,2})\right) + \hat{\alpha}^* \approx \hat{t}_{k,2} - \hat{t}_{k,1} \approx \sum_{j=1}^{M} a_j\left(F_j(\hat{t}_{k,1}) - F_j(\hat{t}_{k,2})\right) + \alpha + N(\hat{t}_{k,2}), \quad (20)$$

where estimation error $e_{k,1}$ and $e_{k,2}$ are neglected as they are very small with an appropriate number of samples. The estimated coefficients can be broked down into two terms, the true value a_j and the error δ_j contributed by $N(t)$, as

$$\hat{a}_j^* = a_j + \delta_j. \quad (21)$$

Substituting (21) back into (20) and canceling identical terms on both sides of the equation, we get

$$\sum_{j=1}^{M} \delta_j [F_j(\hat{t}_{k,1}) - F_j(\hat{t}_{k,2})] \approx N(\hat{t}_{k,2}). \quad (22)$$

Applying series expansion to basis functions, we can simplify (22) into the following form,

$$\sum_{j=1}^{M} \delta_j [F_j(\hat{t}_{k,1}) - F_j(\hat{t}_{k,2})] \approx \sum_{j=1}^{M} \delta_j (\hat{t}_{k,1} - \hat{t}_{k,2}) \frac{d}{dt} F_j(\hat{t}_{k,2}) \quad (23)$$
$$\approx -\sum_{j=1}^{M} \delta_j \alpha \frac{d}{dt} F_j(\hat{t}_{k,2}) \approx N(\hat{t}_{k,2}).$$

Equation (23) is accurate when the offset α is much smaller than the input range of the ADC. Integrating (23) gives the input identification error as

$$F_\delta(t) = \sum_{j=1}^{M} \delta_j F_j(t) \approx \frac{-1}{\alpha} \int N(t). \quad (24)$$

This error will finally become the transition level error. If the estimates in (19) are used in (15) to calculate transition levels, we get

$$\hat{T}_k = \hat{t}_{k,1} + \sum_{j=1}^{M} \hat{a}_j^* F_j(\hat{t}_{k,1}) = \hat{t}_{k,1} + F(\hat{t}_{k,1}) + F_\delta(\hat{t}_{k,1}) \quad (25)$$
$$= T_k + F_\delta(\hat{t}_{k,1}).$$

For instance, if the environment nonstationarity introduces a linear drift error in the offset, the test error will be

$$F_\delta(t) = -\frac{1}{\alpha} \int \Delta t dt = -\frac{\Delta}{2\alpha} t^2, \quad (26)$$

where Δ is the slope of the error in offset. It gives a "bell" shape INL_k test error with a maxim absolute error equal to $\Delta/(8\alpha)$ occurring at the middle of the ADC input range. We can see that the input identification error, as well as the ADC transition level estimation error, is proportional to the relative error in the offset. Therefore, even if the absolute error in the offset is very small as compared to the whole input signal range, it can still seriously hurt the final linearity test accuracy. Another observation we can make is that when designing an SEIR test, appropriately increasing the nominal value of α can reduce the effect of the offset error.

3.2. Signal modeling and environment nonstationarity

As a widely adopted practice, the ramp-based histogram test for ADC linearity is usually implemented by using a periodic triangular wave as the input. One of the major reasons for taking this approach is that it is easier to guarantee the linearity of each individual short and fast ramp, which could have different slopes from one to another but give an overall accurate test result, as compared to a long slow ramp. In the SEIR algorithm, this convention is kept. Both of the two test signals are generated as triangular waves. We will show how the arrangement of the triangular waves from the two signals, without and with offset, respectively, will affect the error in the offset introduced by the nonstationarity in a test system.

Assume a single period of triangular wave takes the following form,

$$x_T(t) = \begin{cases} 2t + F_T(t), & 0 \le t < 0.5; \\ 2 - 2t + F_T(t), & 0.5 \le t < 1; \\ 0, & o.w. \end{cases} \quad (27)$$

where $F_T(t)$ is a general nonlinear component in the triangular wave. This signal vanishes outside [0, 1]. If a test signal contains N_s periods or triangular waves, it can be expressed as

$$x(t) = \sum_{j=0}^{N_s - 1} x_T(t - j). \quad (28)$$

For histogram tests, only the distribution of the input signal affects the test result, so there is always an equivalent ramp signal assuming the form in (5) that can give the same ADC linearity test result as the signal in (28). The SEIR test method uses two signals with one shifted from the other by a constant offset. The two signals can not be generated and quantized by an ADC simultaneously. Generally speaking, the two desired input signals have to be interleaved with each other in the time domain and can be represented as

$$s_d(t) = \sum_{j=0}^{2N_s - 1} [x_T(t - j) - \alpha \cdot I_\Lambda(j)], \quad (29)$$

where $I_\Lambda(j)$ is a characteristic function on an index set Λ. $I_\Lambda(j)$ takes a value of 1 if j is an element of Λ, otherwise 0. The index set Λ specifies the time windows corresponding to the second signal, during which the offset will be added. When the ADC under test is converting the signal $s(t)$, output codes generated during the time windows associated with j's outside Λ will be counted into $H_{k,1}$, and codes associated with j's in Λ will be counted into $H_{k,2}$. Based on the above discussion, the two desired input signals are

$$x_{1d}(t) = \sum_{j \notin \Lambda}^{2N_s - 1} x_T(t - j), \quad (30)$$

and $$x_{2d}(t) = \sum_{j \in \Lambda}^{2N_s - 1} x_T(t - j) - \alpha, \quad (31)$$

which are equivalent to (8) and (9) and have a constant offset in between.

Test environment nonstationarity will inevitably introduce errors in the offset between two signals. A constantly shifted signal as assumed in (9) is practically impossible to achieve. To study the effects of environment nonstationarity on the offset and the method to suppress these effects, we need to quantify them first. Various types

of non-stationary effects exist, including deterministic and stochastic time dependent drifting, as well as random noises. The random noises usually do not degrade the final test performance in an unrecoverable way, since they are uncorrelated from time to time and their effects can be averaged out by a reasonable number of measurements. We will focus our discussion on the non-stationary effects that have a strong correlation during a test window of about tens of seconds to several minutes. These error terms can be modeled as deterministic slowly-changing functions of time in a specific test window. In the SEIR test setup, the "common mode" nonstationarity that affects both the testing circuitries and the ADC does not introduce errors in linearity test results. Only the relative, "differential", non-stationary effects among the signal generator, the offset generator, the adder and the ADC will change the offset value and cause errors. Typical examples of these effects in a test system include power coupling noises through V_{DD} and V_{SS} supplies, thermal disturbances via contacts with the external environment, temperature difference between different functional blocks generated by local power consumptions, and errors introduced by internal voltage distribution networks.

In this work, a drifting reference voltage is multiplied to the desired signals for modeling the "differential" non-stationary effects, while the reference of the ADC under test is assumed to be constant. Any nonstationarity that is common to the ADC and the signal generator will cancel each other's effect and is not modeled. The reference voltage is one of the circuit parameters that are most sensitive to the environmental change and has a dominant effect on the circuit behaviors, such as the output voltage of a signal generator, so a drifting reference voltage can effectively model the test system non-stationary effects in general. The reference voltage is modeled by the following equation,

$$V_{ref}(t) = 1 + e_d(t), \tag{32}$$

where $e_d(t)$ is the drifting error. We are focusing on linearity testing and do not care about the absolute value of the input voltage, so the nominal reference voltage is scaled to 1. The drifting error can usually be viewed as a combination of low order polynomial terms as a function of time plus additive noises for one test,

$$e_d(t) = \sum_{i=1}^{L} b_i t^i + n_{ref}(t), \tag{33}$$

where b_j's are coefficients of polynomials and $n_{ref}(t)$ is the noise. We truncate the polynomial at the L-th order. A second or third order polynomial is usually sufficient for describing the reference drift, which is dominantly a slowly changing function of time, in an overall time window of several minutes or shorter for testing ADC linearity.

By multiplying the reference voltage to the desired signals, we get the true input signals to the ADC as

$$x_1(t) = \sum_{j \notin \Lambda}^{2N_s-1} x_T(t-j)[1 + e_d(t)], \tag{34}$$

and $$x_2(t) = \sum_{j \in \Lambda}^{2N_s-1} [x_T(t-j) - \alpha][1 + e_d(t)]. \tag{35}$$

Respectively taking the average of different triangular wave periods for the first and second signals, the difference between the averaged signals can represent the time-dependent offset between the two signals,

$$\begin{aligned} d(t) &= \frac{x_T(t)}{N_s} \sum_{j \notin \Lambda}^{2N_s-1} [1 + e_d(t+j)] - \frac{x_T(t) - \alpha}{N_s} \sum_{j \in \Lambda}^{2N_s-1} [1 + e_d(t+j)] \\ &= \alpha + \frac{\alpha}{N_s} \sum_{j \in \Lambda}^{2N_s-1} e_d(t+j) + \frac{x_T(t)}{N_s} [\sum_{j \notin \Lambda}^{2N_s-1} e_d(t+j) - \sum_{j \in \Lambda}^{2N_s-1} e_d(t+j)]. \end{aligned} \tag{36}$$

The first term is the desired constant offset. The others are unwanted errors. Their total effect is represented by $N(t)$ in (16) and introduces input identification and ADC test errors as in (24) and (25). To have a constant offset, we would like to make the second and third terms in (36) be constant or equal to zero.

3.3. SEIR test in non-stationary environment

Based on the modeling and discussion in the previous subsection, it will be shown that a good choice of the index set Λ for the second signal's time windows can help significantly reduce the offset error introduced by non-stationary effects of the test environment.

Let us first look at the second term in (36). The reference drifting in a short period of time is not predictable, so $e_d(t)$ is unknown and it is difficult to make this term constant. However, the drifting effect of the reference voltage is attenuated by the multiple-triangle implementation of a ramp signal, since each triangle only experiences a small portion, approximately $1/(2N_s)$ in our two input testing case, of the total drift error. Furthermore, this term is proportional to nominal offset α, so its effect on the overall offset is not significant. Assuming each signal consists of N_s = 32 triangles and the signal source has 1000 ppm dominantly-linear drifting error in its reference voltage during a test, it will introduce a relative error of about 16 ppm in the offset through the second term in (36). Based on (26) and the discussion thereafter, this will introduce about 2 ppm error in ADC linearity test, which is much smaller than 1 LSB at the 16-bit resolution level (16 ppm). In reality, most of the existing tester circuitries can maintain better than 1000 ppm stability during a test time of several minutes or shorter, so the second term in (36) will not introduce large test errors for testing ADCs with 16-bit, or even higher, resolutions.

The third term in (36) is proportional to the input signal, which can be much larger than offset α. It will introduce large relative errors in the offset and give inaccurate ADC test results if not well handled. From (33), we get

$$\begin{aligned}&\sum_{j\notin\Lambda}^{2N_s-1} e_d(t+j)-\sum_{j\in\Lambda}^{2N_s-1} e_d(t+j)\\&=\sum_{i=1}^{L} b_i[\sum_{j\notin\Lambda}^{2N_s-1}(t+j)^i-\sum_{j\in\Lambda}^{2N_s-1}(t+j)^i]\\&=\sum_{i=1}^{L} b_i\sum_{l=0}^{i}\binom{i}{l}t^{i-l}(\sum_{j\notin\Lambda}^{2N_s-1} j^l-\sum_{j\in\Lambda}^{2N_s-1} j^l),\end{aligned} \tag{37}$$

where the choice numbers of i choose l are used and noise terms are neglected, since noise effects will be effectively averaged out in an LS-based algorithm. It can be observed that if we make the l-th moment of j's in Λ equal to that of j's outside Λ, for all l less than or equal to L, (37) is equal to zero. This gives us the criteria of what is a good Λ set. One remark is that the choice of Λ is independent of the drifting characteristics of the reference voltage.

One procedure of determining Λ is shown as follows. It starts from a sequence of one single element, [0], which will be extended to generate the elements of Λ. Extension of the sequence takes following steps:

- Start from the beginning of the current level of sequence.
- If meet a '0' in the current level of sequence, append '01' to the next level of sequence.
- If meet a '1' in the current level of sequence, append '10' to the next level of sequence.
- Finish until the end of the current level of sequence.
- Repeat above steps with the next level of sequence until the length of the sequence is equal to $2N_s$.

The first 7 levels of sequences are listed in Figure 2 (a). The final generating sequence has a length of $2N_s$, because $2N_s$ periods of triangular waves are used in an SEIR test for two signals. Index the generating sequence from 0 to $2N_s - 1$. The set Λ is choose to be the indices of "1" elements in the generating sequence. It can be verified that l-th respective moments of j's inside and outside Λ are equal to each other, for l up to $L = \log_2 N_s$. For instance, if $N_s = 32$, it can be calculated from Figure 2 (a) that $\Lambda = \{1, 2, 4, 7, 8, 11, 13, 14, 16, 19, 21, 22, 25, 26, 28, 31, 32, 35, 37, 38, 41, 42, 44, 47, 49, 50, 52, 55, 56, 59, 61, 62\}$, and the first to fifth moments of j's in Λ are the same as those of j's outside Λ. The signal generated by using the fifth sequence is plotted in Figure 2 (b), where a negative offset is added at j in $\Lambda = \{1, 2, 4, 7, 8, 11, 13, 14\}$.

Usually the dominant component in reference voltage drifting are controlled to change slowly as a function of time by a well design, so it is assumed that high-order polynomial terms in (33) be small. By using the above Λ set to pick the triangles for the first signal (no offset) and second signal (with offset) in (34) and (35), the signal-level dependent error in the offset can be significantly reduced because the dominant low-order components in drifting are eliminated. Therefore the offset between the two signals can be sufficiently constant for using the SEIR algorithm to test high-resolution ADCs, even in a non-stationary environment.

[0]

[01]

[0110]

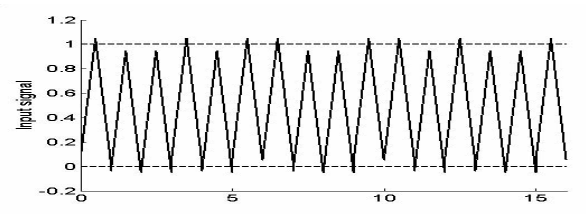
[01101001]

[0110100110010110]

[01101001100101101001011001101001]

[0110100110010110100101100110100110010110011010010110100110010110]

(a)



(b)

Figure 2 (a) First 7 levels of Λ generating sequences. (b) Signal generated using the fifth sequence.

4. Simulation Results

Simulations were run to validate the conclusions in Section 3. The ADC under test was modeled by a 16-bit flash structure with resistance mismatch in the simulation. The SEIR test algorithm is not sensitive to the ADC architecture. We choose the flash structure because it has a large number of independent error sources so that it can validate the performance of SEIR method under the challenging situations. To save simulation time, the number of average samples per code was set to 8, while it could take more than 50 samples per code in real production test applications for high-precision ADCs. In simulation, the additive noise at the ADC input had a standard deviation of 0.5 LSB. If a larger noise exists in the real test environment, its effects can be averaged out by increasing the number of measurements. The input signals were composed of triangular waves with less than 7-bit linearity. 16 sinusoidal basis functions were used in the SEIR algorithm to identify the input nonlinearity.

First we checked correctness of (24). We chose $N_s = 8$. The reference voltage had 100ppm linear drifting during the whole test time to model a non-stationary test environment. To have a visible effect of the non-constant offset, the triangular waves of the first and second signals were not carefully arranged. The second signal was generated after the first signal is completed. That means

$\Lambda = \{8, 9, 10, \ldots, 15\}$. The INL_k estimation results using the SEIR method for a same ADC are plotted in Figure 3 and 4, for offset values as 0.5% and 1% of the total ADC input range, respectively.

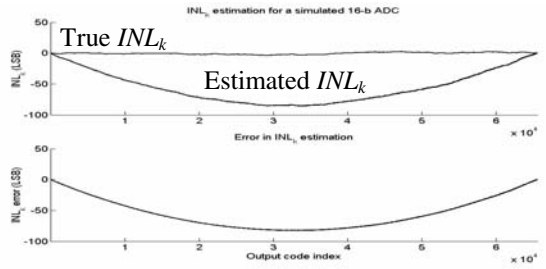


Figure 3 INL_k estimation, α = 0.5%, 100 ppm drifting.

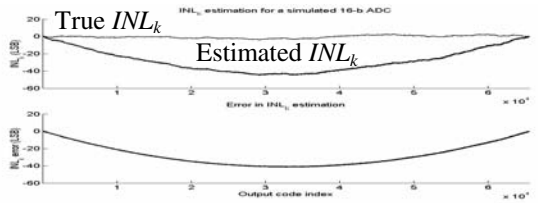


Figure 4 INL_k estimation, α = 1%, 100 ppm drifting.

From Figure 3 and Figure 4, we can see that the INL_k estimation error has a "bell" shape and the maximum error happens at the middle of the ADC input range. The maximum is inversely proportional to offset α, reduced by half when α is doubled. Further calculation based on (24) show that the equivalent error in the offset is approximately a linear drift with a 50 ppm slope, which is in agreement with the simulation setup.

Then we checked the effectiveness of the Λ generation method introduced in Section 3.3. N_s was again chosen to be 8. The reference voltage had the same 100 ppm linear drifting. The offset between two signals was 0.5% of the overall ADC input range. The Λ was determined by using the fifth sequence in Figure 2 (a) and the overall input signal had the same pattern as in Figure 2(b). The INL_k estimation result using the SEIR method is plotted in Figure 5. The top part of Figure 5 contains two curves, the true and estimated INL_k. They match very well and the difference between them can hardly be seen from the plot. The estimation error is dramatically reduced as plotted on the bottom part of Figure 5, from more than 80 LSB in Figure 3 to 1 LSB at the 16-bit level. The residue errors mainly come from the noise effect due to the small number of samples. We run another simulation with 500 ppm linear drift to represent a worse test environment, and the results are shown in Figure 6. The estimation errors remain at about the same level, not increasing with the reference voltage drifting and are mainly due to noise.

The observations above confirm that the proposed arrangement method for the first and second signal can eliminate the effect of test environment nonstationarity very well and give out accurate linearity test results for high-resolution ADCs when used together with the SEIR algorithm. The INL_k of a 16-bit ADC can be tested to 1 LSB level accuracy by using less than 7-bit linear signals under an environment with more than 100 ppm reference voltage drifting.

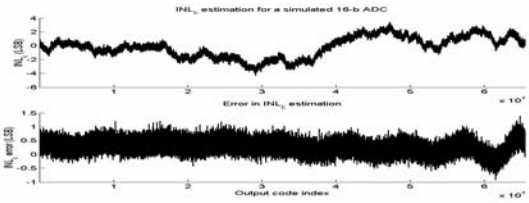


Figure 5 INL_k estimation, α = 0.5%, 100 ppm drifting.

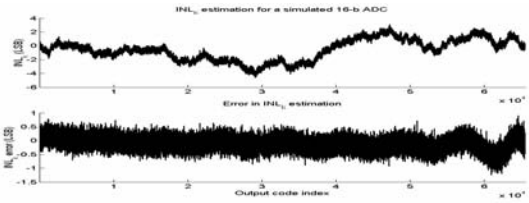


Figure 6 INL_k estimation, α = 0.5%, 500 ppm drifting.

5. Experimental Results

Commercially available 16-bit ADCs were tested to verify the performance of the combined method of the SEIR algorithm and the signal arrangement strategy. The sample used as the device under test was a laser trimmed 16-bit successive-approximation register (SAR) ADC with excellent linearity performance with typical *INL* of about 1.5 LSB, which is a known test challenge. The test hardware used for the verification of the proposed method is the same as used in the production test of the device.

5.1. Test setup

Verification of the performance of this ADC requires extreme attention to test hardware design. A 12-layer handler interface board was used with extensive ground, supply and reference coverage. Extreme care was given to reduce ground loops and to obtain proper bypassing. High performance contactors, high precision resistors, high performance capacitors, and precision op-amps were used throughout the board. Latching relays were used to reduce temperature gradients generating metal to metal contact noise effects. The digital outputs were damped and buffered properly to avoid current surges. The test platform was a Teradyne A580 Advanced Mixed Signal Tester. The source generating both the linear and the synthetic nonlinear excitations was a 20-bit multi-bit delta-sigma DAC with 2ppm typical linearity error, 100μV/minute typical drift characteristics, and 2 kHz bandwidth. This signal source is a typical example

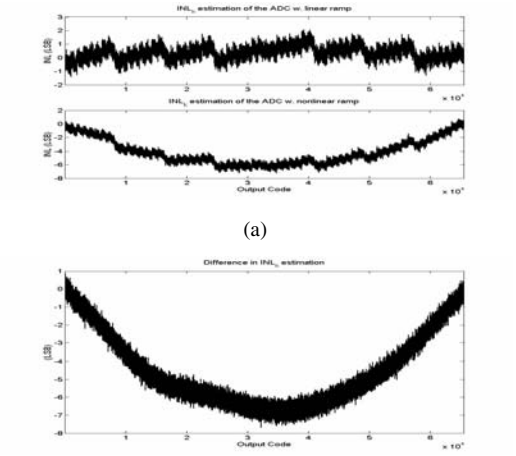
demonstrating that an expensive signal generator is not always good enough to provide low drift, high speed and good linearity all at the same time. The DC offset of the nonlinear excitation was generated using an analog summing circuit. In the experiment, the capture of histogram data using nonlinear signals and identification of INL_k using the proposed method were done on different platforms. The tester setup, including the shape of input nonlinearity and offset between the two signals were not known to the identification algorithm. Only two sets of histogram bin counts were sent to the analysis program.

5.2. Test data collection and analysis

The INL_k of the ADC was tested by both the traditional method and by the SEIR method. 32 samples per code were used to keep the test time reasonable. The two nonlinear signals were synthetically generated by programming the source memory with a nonlinear digital waveform so that they had about 7-bit linearity.

The first experiment was done without carefully arranging the two signals, simply generating the second signal after the first signal was completed. The offset was set to 0.1%. Figure 7 gives the test results. To do comparison, the ADC was first tested by using the conventional histogram method with a 20-bit linear signal and the tested INL_k is plotted on top of Figure 7 (a). This INL_k will be used as a reference to determine the performance of the following SEIR test. The SEIR algorithm tested ADC by using the two 7-bit linear signals and the tested INL_k is plotted on bottom of Figure 7 (a). The difference between the two tested INL_k is plotted in Figure 7 (b), which mostly comes from the error in SEIR test introduced by the non-constant offset. As can be seen from the plot, SEIR test results have errors of a "bell" shape and a maximum value of more than 7 LSB. This error is expected because there are always nonstationarity existing in the test system.

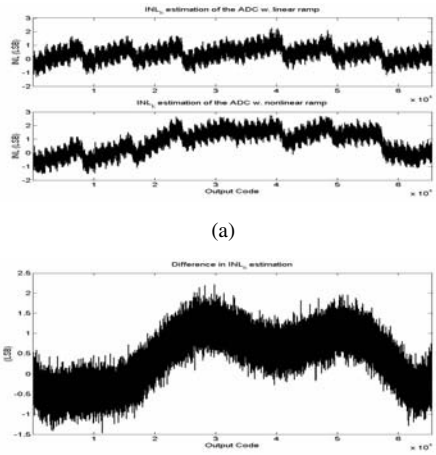
Next the ADC was tested with an improved arrangement of signals, while all other setups are unchanged. Instead of letting the second signal go after the first one, the triangular waves of the two signals were evenly interleaved, which means $\Lambda = \{1, 3, 5, \ldots\}$. Figure 8 gives the test results. Again a test result with a 20-bit linear signal is used as a benchmark and plotted on top of Figure 8 (a). The SEIR result is on the bottom. This time test errors of the SEIR algorithm with 7-bit linear signals were reduced to about the 2-LSB level, and did not have a big "bell" shape. That means the even interleaving arrangement of two signals can reduce the non-stationary effects on offset, but it is still not good enough for testing the 16-bit ADC.



(a)

(b)

Figure 7 INL_k measurement. Top of (a): test results with 20-bit linear signal. Bottom of (a): test results with 7-bit linear signals, α = 0.1%. (b): difference between results.



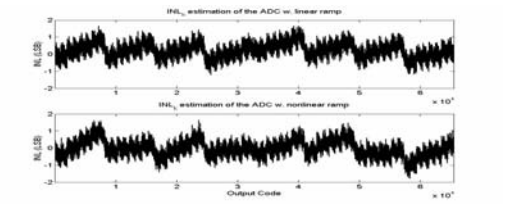
(a)

(b)

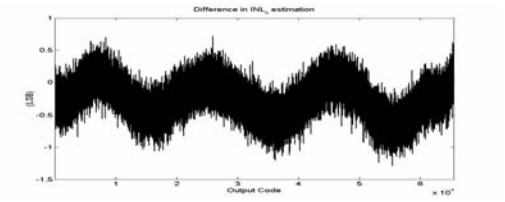
Figure 8 INL_k measurement. Top of (a): test results with 20-bit linear signal. Bottom of (a): test results with 7-bit linear signals, α = 0.1%. (b): difference between results.

Finally the signal arrangement method developed in this work was used in the SEIR test. This time the DC offset was set to a smaller value, 0.05%, which may lead to larger test errors as compared to the 0.1% offset. N_s was set to 32 and consequently the seventh sequence in Figure 2 (a) was used to determine the set Λ, canceling up to the fifth order reference drifting errors. The test results are plotted in Figure 9. As our old convention, the ADC was first tested by using a highly linear signal with the traditional histogram method, with the results plotted on top of Figure 9 (a). The corresponding measured *INL* is 1.66 LSB. Then histogram data were obtained with the 7-bit linear input signals and analyzed using the SEIR algorithm with 10 basis functions. The estimated INL_k is plotted on bottom of Figure 9 (a). The estimated *INL* with nonlinear signals is 1.77 LSB. We can see that when using

the proposed signal arrangement method, the INL_k estimated using linear and nonlinear signals are really close. The difference in *INL* estimation is only 0.11 LSB. The difference between the estimates is shown in Figure 9 (b). The errors in INL_k prediction are mostly less than 1 LSB. That means the proposed approach can effectively make the offset between two signals a constant in non-stationary environments and is an acceptable solution as far as 16-bit converters are concerned.



(a)



(b)

Figure 9 INL_k measurement. Top of (a): test results with 20-bit linear signal. Bottom of (a): test results with 7-bit linear signals, α = 0.05%. (b): difference between results.

In Figure 9 (b), the difference between testing results mainly come from two sources. First, the high frequency errors are introduced by the additive noise, which gives a band of about +/- 0.5 LSB. Second, the low frequency error component is contributed by the residue of non-constant errors in the offset, which are not completely cancelled by the signal arrangement approach. Based on (24), this kind of error is inversely proportional to the offset amount. Since the offset value is only 0.05% in the last test, there is some room for increasing the offset amount to further reduce the INL_k test error to well below the noise error level.

The experimental test results presented in this section show that by combining the SEIR algorithm with the proposed signal arrangement technique, linearity of high-precision ADCs can be accurately tested by using low-linearity signals in non-stationary environments. The non-stationary effects of the environment can be eliminated by appropriate signal arrangement that gives a constant offset. The input nonlinearity can be identified and removed by the SEIR algorithm. The test time penalty of the SEIR algorithm was found to be insignificant. The actual test time for this 16-b ADC was about 1 minute, and the post-processing took 1.2 seconds in Matlab to calculate all of the INL_k values from the collected bin counts. Once coded in the tester workstation, the algorithm is expected to complete well within 100 milliseconds.

6. Conclusions

In this paper, a test strategy that can eliminate the effects of input nonlinearity and environment stability errors on the test results of high-resolution ADCs is introduced. Using the SEIR algorithm along with the proposed signal arrangement technique, 16-bit ADCs were tested accurately with only 7-bit linear input signals in an environment with more than 100 ppm nonstationarity in the test window. This strategy is promising to solve test problems that are very challenging to state-of-the-art technologies, such as full characterization of ADC linearity at more than 16-bit resolution levels, since both the signal linearity and environment stability are no longer required to be better than ADC specifications. This strategy can also help control the cost of existing test solutions by allowing the use of cheap instruments. Furthermore, the strategy has the potential to be used in on-chip test environment, where accurate test devices may not be available.

7. References

[1] *International Technology Roadmap for Semiconductors*, 2003 edition, available online: http://public.itrs.net.

[2] T. Kuyel, "Linearity Testing Issues of Analog-to-Digital Converters," in *Proc. 1999 International Test Conference*, pp. 747-756, Sept 1999.

[3] J. Doernberg, H.-S. Lee, and D.A. Hodges, "Full-Speed Testing of A/D Converters," *IEEE J. Solid-State Circuits,* SC-19, pp. 820-827, December 1984.

[4] J. Blair, "Histogram measurement of ADC nonlinearities using sine waves," *IEEE Trans. Instrum. Meas.,* vol. 43, pp. 373-383, June 1994.

[5] *IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters*, Dec 2000.

[6] E. Siragusa and I. Galton, "A Digitally Enhanced 1.8-V 15-Bit 40-MSample/s CMOS Pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 39, pp 2126- 2138, Dec 2004.

[7] A. Roy, S. Sunter, A. Fudoli, and D. Appello, "High Accuracy Stimulus Generation for A/D Converter BIST," in *Proc. 2002 International Test Conference*, pp. 1031-1039, Oct. 2002.

[8] S. Bernard, M. Comte, F. Azais, Y. Bertrand, and M. Renovell, "A New Methodology for ADC Test Flow Optimization," in *Proc. 2003 International Test Conference*, vol. 1, pp. 201-209, Sept 2003.

[9] S. Max, "Ramp Testing of ADC transition Levels Using Finite Resolution Ramps," in *Proc. 2001*

International Test Conference, pp. 495-501, Nov 2001.

[10] S. Sunter and N. Nagi, "A Simplified Polynomial-Fitting Algorithm for DAC and ADC BIST," in *Proc. 1997 International Test Conference*, pp. 389-395, Nov 1997.

[11] B. Provost and E. Sanchez-Sinencio, "On-Chip Ramp Generators for Mixed-Signal BIST and ADC Self-Test," *IEEE J. Solid-State Circuits*, vol. 38, pp. 263-273, Feb 2003.

[12] L. Jin, K. Parthasarathy, T. Kuyel, D. Chen and R. Geiger, "Accurate testing of analog-to-digital converters using low linearity signals with stimulus error identification and removal," *IEEE Trans. Instrum Meas.*, vol. 54, pp. 1188 – 1199, June 2005.