Yield Enhancement With Optimal Area Allocation for Ratio-Critical Analog Circuits

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***Abstract*—Parametric yield models for widely used area allocation schemes in ratio-critical analog circuits are developed. It is shown that some of the most widely used schemes are suboptimal and that significant improvements in parametric yield can be achieved with less intuitive area allocation approaches. Simulations results are presented which show quantitatively what improvements in yield can be achieved with improved area allocation strategies for resistive feedback amplifiers and R-2R ladders.**

***Index Terms*—Area allocation, contact resistance, parametric yield, resistor strings, R-2R ladders, yield.**

I. Introduction

IT IS WELL known that different layouts of a given matching-critical circuit can have significantly different performance and yield and considerable effort is often focused on developing good layout strategies. Much of this effort has been focused on managing gradient effects, propagation delays, ohmic voltage drop in interconnects, and parasitic capacitances. Gradient-tolerant layouts including segmented common centroid structures, path-length matching, orientation awareness, the use of dummy devices on the periphery of matching critical components, and careful sizing of interconnects have proven useful for improving effective matching performance [1]–[3]. Local random variations in process parameters, however, are often a significant contributor to performance degradation and parametric yield loss and none of the layout strategies mentioned provide any relief for the problems caused by the local random variations. Unless some form of calibration is incorporated, about the only effective method most designers use for managing the adverse effects of local random parameter variations is to increase the area or physical size of the matching-critical components. It is well known that the standard deviation of many performance parameters of interest often decreases proportionally to the reciprocal of the square root of the area [1], [4]–[7]. Thus, a factor of 4 increase in area is required for each factor of 2 reduction in the standard deviation of the random component of the performance parameter. In addition to the adverse effect on device area, the larger devices often introduce additional parasitic capacitances and limit the speed of operation of the circuit, and in some cases also increase the power dissipation.

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Invariably the area allocated to matching-critical passive and active devices is dependent upon and often proportional to the component value of the devices. For example, the area conventionally allocated by designers to each of the "R" resistors in an R-2R ladder is the same and the area allocated to each of the "2R" resistors is also the same. Correspondingly, if the ratio of two resistors is K, the area allocated to one of the two resistors is conventionally K times of the area allocated to the other resistor. This component-ratio based area allocation strategy is natural and supports the concept of realizing a ratio-critical circuit with the appropriate interconnection of unit cells.

Considering the cost of the silicon area not only in terms of the real estate but also the performance implications associated with the area-dependent parasitic capacitances and power dissipation, the question naturally arises: Is the component-ratio based area allocation strategy optimal? Or, equivalently, can parametric performance and yield be improved within a fixed silicon area constraint with other area allocation strategies?

In this paper, we focus on the relationship between parametric performance, parametric yield, and area allocation in matching-critical circuits. In particular, the issues of area allocation in feedback networks, R-2R ladders, and resistor string DACs are addressed.

In what follows it will be assumed that the only nonideal effects are the random variation in matching critical components. That is, the effects of gradients, placement, and orientation of matching-critical components will not be considered but it will be assumed that known existing layout strategies including segmentation, common-centroid layouts, and peripheral dummy devices are used to manage such nonideal effects. The beneficial properties, ensuring from good layout strategies that provide insensitivity to local nonrandom variations are, in general, not adversely affected by the optimal area allocation strategies introduced in this paper.

As an example, for a negative feedback amplifier with a nominal gain of -16, if an optimal area allocation strategy is used instead of the widely used component-ratio area allocation approach, it will be shown that the parametric yield due to local random variations in the sheet resistance can be increased from 78% to 99% with the same total area in a typical process.

With decreasing feature sizes in emerging processes, the cross-sectional area of contacts is decreasing with feature size. This is driving up the contact resistance and usually increasing the variance of the contact resistance between two closely placed contacts. The implication is that the effective resistance of film resistors is becoming increasingly dependent upon contact resistance and the variance of the effective resistance is becoming increasingly dependent upon the variance of the

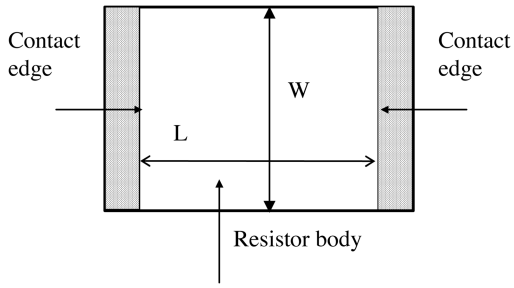

Fig. 1. Homogeneous rectangular thin film resistor.

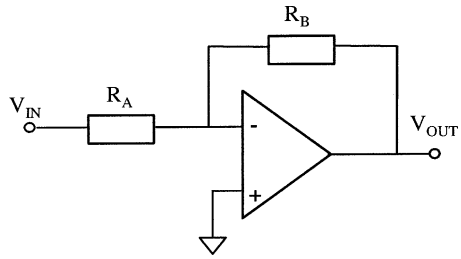

Fig. 2. The basic resistor feedback amplifier.

contact resistances. A statistical model for the effects of contact resistance on the performance of matching-critical circuits is also discussed and included in the formulation of the area allocation problem in matching-critical circuits.

II. Area-Partitioning

The effects of local random variations in the sheet resistance on the resistance of a rectangular film resistor depicted in Fig. 1 will be considered in this section. In this simplified description, the resistor body is a rectangular region of length $L$and width W with contacts along the left and right sides of the resistor. The film material that comprises the resistor body is assumed to be homogeneous, that is, the nominal sheet resistance is independent of position in the resistor body. It will be assumed initially that the contact resistance of the rectangular resistor is 0 Ω. It will also be assumed that the local random variations in the sheet resistance from one point to another distinct point are uncorrelated, and that the length L and width W are equal to their nominal values. Comments about the random variations in W or L, which may play a role in matching properties when W or L is small, will be made later. With these assumptions, it follows that the nominal resistance of a rectangular resistor is given by the expression

$$R_N = R_{\square N}\frac{L}{W} \tag{1}$$

where $R_{\square N}$ is the nominal value of the sheet resistance. The variance of the normalized resistance can be expressed as [1], [5], [8], Appendix

$$\sigma^2_{\frac{R}{R_N}} = \frac{1}{\mathrm{WL}}\cdot\left(\frac{A_\rho}{R_{\square N}}\right)^2 = \frac{1}{A_R}\cdot\left(\frac{A_\rho}{R_{\square N}}\right)^2 \tag{2}$$

where the random variable R is the resistance, A_ρ is a process parameter that characterizes the random local sheet resistance variation, and A_R is the area of the resistor.

A. Feedback Amplifier

A basic negative feedback amplifier is shown in Fig. 2. The gain, θ, of the amplifier is given by the well-known expression $\theta = -R_B/R_A$ [9] where the resistors R_A and R_B are random variables that differ from their nominal values because of the local random variations in the sheet resistance. The nominal value of the gain is given by the expression $\theta_N = -R_{BN}/R_{AN}$ where R_{AN} and R_{BN} are the nominal values of the resistors R_A and R_B, respectively. The random variables $R_A - R_{AN}$ and $R_B - R_{BN}$ are assumed to be uncorrelated with zero mean and have a nearly Gaussian distribution [10], [11]. If the random component of R_A or R_B is appreciable relative to the nominal component, a closed-form explicit expression of the probability density function (PDF) of the gain is difficult or impossible to obtain. In such situations, however, the gain accuracy would be so poor that these amplifiers would be of little use in precision applications. Correspondingly, in the practical applications of interest in this work where accurate gain is required, the random component of R_A, denoted as R_{AR}, and the random component of R_B, denoted as R_{BR}, must be very small relative to the nominal component if reasonable yields are to be obtained. In these situations, it can be shown that the normalized gain can be approximated by the expression

$$\frac{\theta}{\theta_N} \approx 1 - \frac{R_{AR}}{R_{AN}} + \frac{R_{BR}}{R_{BN}} \tag{3}$$

where θ_N is the nominal gain, i.e., $\theta_N = -R_{BN}/R_{AN}$.

Since R_{AR} and R_{BR} are independent Gaussian random variables and since it is well known that the linear combination of Gaussian random variables is Gaussian, it follows that the normalized gain is also Gaussian with variances given by

$$\sigma^2_{\frac{\theta}{\theta_N}} = \sigma^2_{\frac{R_A}{R_{AN}}} + \sigma^2_{\frac{R_B}{R_{BN}}}. \tag{4}$$

It follows from (2) and (4) that the variance of the normalized gain can be rewritten as

$$\sigma^2_{\frac{\theta}{\theta_N}} = \left(\frac{1}{A_{R_A}} + \frac{1}{A_{R_B}}\right)\cdot\left(\frac{A_\rho}{R_{\square N}}\right)^2 \tag{5}$$

where A_{R_A} and A_{R_B} are the areas of R_A and R_B, respectively.

Two natural methods for area allocation for the resistors are what we term the "conventional series" allocation and the "conventional parallel" allocation. If θ_N is an integer, the conventional series allocation is characterized by the formation of R_B with the series connection of θ_N unit cells while R_A is comprised of a single unit cell. This is depicted in Fig. 3(a). The unit cell itself may be physically a series or parallel combination of smaller unit cells if a common centroid layout is used to minimize gradient effects. Correspondingly, the conventional parallel allocation is characterized by the formation of R_A with the parallel connection of θ_N unit cells while R_B is comprised of a single unit cell. This is depicted in Fig. 3(b).

If A_{CELL} is the area of the unit cell, it follows from (5) that the variance of θ_N for both of the conventional area allocation strategies is given by

$$\sigma^2_{\frac{\theta}{\theta_N}} = \frac{1}{A_{\mathrm{CELL}}}\cdot\left(1+\frac{1}{\theta_N}\right)\cdot\left(\frac{A_\rho}{R_{\square N}}\right)^2 \tag{6}$$

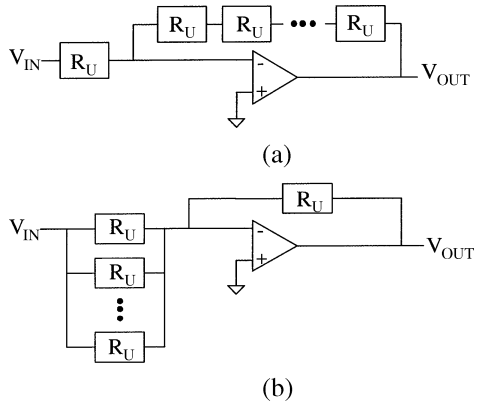

Fig. 3. Conventional (a) series and (b) parallel area allocation strategies for amplifier.

or, if A_T is the total area allocated to the resistors, it can be expressed in terms of A_T as

$$\sigma^2_{\frac{\theta}{\theta_N}} = \frac{1}{A_T} \cdot \left(\frac{1}{\sqrt{\theta_N}} + \sqrt{\theta_N} \right)^2 \cdot \left(\frac{A_\rho}{R_{\square N}} \right)^2. \tag{7}$$

It follows from (7) that the standard deviation of the gain can be expressed as

$$\sigma_\theta = \frac{1}{\sqrt{A_T}} \cdot \left(\theta_N^{0.5} + \theta_N^{1.5} \right) \cdot \left(\frac{A_\rho}{R_{\square N}} \right). \tag{8}$$

It should be apparent from (8) that for a fixed total area, the standard deviation increases rather rapidly with θ_N and that for large gains, it increases with $\theta_N^{1.5}$.

Both the conventional series and conventional parallel area allocation strategies can be viewed as component-ratio based area allocation schemes since the area allocated to the resistors is proportional to the values of the resistors.

The issue of optimal area allocation for a fixed total resistor area will now be addressed. It follows from (5) that the variance can be expressed in terms of A_T as

$$\sigma^2_{\frac{\theta}{\theta_N}} = \left(\frac{1}{A_{R_B}} + \frac{1}{A_T - A_{R_B}} \right) \cdot \left(\frac{A_\rho}{R_{\square N}} \right)^2. \tag{9}$$

If this expression is minimized for a fixed A_T with respect to A_{R_B}, it follows from a simple derivation that the variance is minimized if

$$A_{R_A} = A_{R_B} = \frac{A_T}{2} \tag{10}$$

and $\sigma^2_{\theta\min/\theta_N}$ is given by

$$\sigma^2_{\frac{\theta_{\min}}{\theta N}} = \frac{4}{A_T} \cdot \left(\frac{A_\rho}{R_{\square N}} \right)^2. \tag{11}$$

It follows from (11) that the standard deviation of the gain for the optimal area allocation can be expressed as

$$\sigma_\theta = \frac{2\theta_N}{\sqrt{A_T}} \cdot \left(\frac{A_\rho}{R_{\square N}} \right). \tag{12}$$

These results can be summarized with the layout principle for ratio-matched resistors.

Layout Principle for Ratio-Matched Resistors: The effects of local random variations in sheet resistance in the ratio matching accuracy of two rectangular resistors will be minimized for a given total resistor area if equal area is allocated to the two resistors.

A comparison of (7) with (11) shows a rather substantial difference. Specifically, the conventional series and conventional parallel allocation strategies have a standard deviation dependent upon $\theta_N^{1.5}$ whereas the optimal area allocation strategy has a standard deviation dependent upon θ_N. This difference can be quite significant for large gains.

As an example, if an amplifier with a gain of 16 is implemented with the conventional series area allocation, the standard deviation will increase by a factor of 2.125 over that for an optimal area allocation. This difference may be better appreciated from a parametric yield comparison. If the gain of 16 must be accurate to 1% and the total resistor area is allocated to achieve a 99.999% parametric yield with an optimal area allocation scheme, then the parametric yield would drop to 96.75% for either the conventional series or the conventional parallel area allocation strategy. Although it may appear that this is only a drop of 3.25% in yield, the economical impact of this yield drop is very significant. For example, if a circuit required 32 channels with a gain of 16 all with an accuracy requirement of 1%, then the optimal area allocation strategy, assuming a Gaussian distribution, would provide a parametric yield of $0.99\,999^{32} = 99.97\%$ whereas that of the conventional series layout would be $0.9675^{32} = 34.74\%$.

In some cases it may not be convenient to exactly allocate the same area to R_A and R_B. Such might be the case, for example, if the desired gain is 3. In these cases, it is useful to quantify the parametric yield loss or correspondingly the deterioration in the standard deviation of the gain from the optimal value. If we define the area split factor γ by the expression $\gamma = A_{R_B}/A_T$, it follows from (9) and (11) that

$$\sigma_\theta = \sigma_{\theta\min} \frac{1}{2\sqrt{\gamma(1-\gamma)}} \tag{13}$$

where it is apparent that the standard deviation achieved its minimum value when $\gamma = 1/2$.

A plot of the normalized standard deviation of the gain versus γ is shown in Fig. 4. From this plot it is apparent that the minimum at $\gamma = 1/2$ is shallow but that the standard deviation penalty goes to infinity if the area differences are large. For example, if we want the standard deviation to be at most 0.5% above the optimal value, then $0.4502 \leq \gamma \leq 0.5498$ whereas if a 1% deviation is acceptable, then $0.4298 \leq \gamma \leq 0.5702$. A near-minimum standard deviation and correspondingly near-optimal yield will be achieved only if the standard deviation of the ratio is within the insensitive shallow region of the curve in Fig. 4.

An example of where it is not practical to achieve an equal split in the area but where near-optimal yield is still achievable is worth mention. If the desired gain is 8, then R_B can be implemented with eight unit resistors in series and R_A can be implemented with nine unit resistors in a 3 by 3 series-parallel combination. This results in a γ value of 8/17 which is in the insensitive shallow region near the optimal value of $\gamma = 0.5$.

An appreciation for the significance of the improvement of the optimal area allocation strategy relative to that of the conventional series layout or the conventional parallel layout can be obtained from Fig. 4. It should be apparent that for small gains,

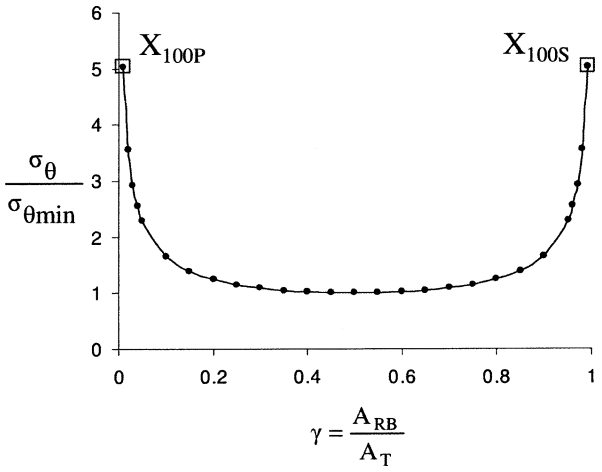

Fig. 4. Effects of area partitioning on the normalized standard deviation.

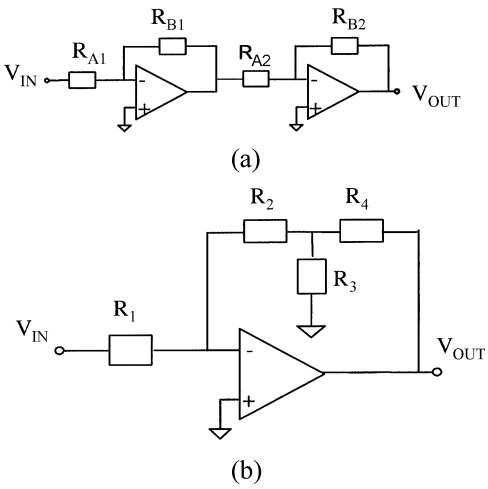

Fig. 5. (a) Cascade amplifier. (b) T-feedback network amplifier.

the benefits for going from the conventional series or the conventional area allocation strategy to the optimal area allocation strategy are minimal. However, the benefits are very significant when large gains, e.g. 100 with the series or parallel layout designated with points $X_{100\mathrm{S}}$ and $X_{100\mathrm{P}}$ in Fig. 4, are required.

When large gains are required it is apparent from (11) that even with the optimal area allocation strategy, the standard deviation increases with the gain. There is also concern about the large component spread required to achieve large gains. There are two common strategies used for reducing the component spread. One uses the cascade of lower gain stages and the other is based upon using a T-feedback network. These are depicted in Fig. 5(a) and (b), respectively. The issue of what impact these alternate architectures have on gain accuracy with the presence of random variations in sheet resistance will now be investigated.

For the cascaded amplifier of Fig. 5(a), it can be shown following a technique similar to that used for the basic amplifier of Fig. 2 that the standard deviation of the gain will be minimized if

$$A_{R_1} = A_{R_2} = A_{R_3} = A_{R_4} = \frac{A_T}{4} \tag{14}$$

and $\sigma^2_{\theta\,\min/\theta_N}$ is given by

$$\sigma^2_{\frac{\theta\,\min}{\theta_N}} = \frac{16}{A_T} \cdot \left(\frac{A_\rho}{R_{\square N}}\right)^2. \tag{15}$$

A comparison of (11) and (15) shows that the standard deviation doubles when the same gain is realized with a cascade of two amplifier stages. This can cause a significant penalty in yield if the cascaded amplifiers are used instead of using a single stage amplifier. For a cascade of k amplifiers, it can be shown that the standard deviation will be minimized if all resistors have the same area which is $A_T/2k$ and the corresponding minimum variance is given by

$$\sigma^2_{\frac{\theta\,\min}{\theta_N}} = \frac{4k^2}{A_T} \cdot \left(\frac{A_\rho}{R_{\square N}}\right)^2 \tag{16}$$

It should be apparent that the penalty in the yield for a given area becomes significant if a large number of cascaded gain stages are used.

The analysis of the amplifier with the T-feedback network is somewhat more tedious. It is straightforward to show that the magnitude of the nominal gain of the amplifier of Fig. 5(b) is given by the expression

$$\theta_N = \frac{R_{2N}}{R_{1N}}\left(1 + \frac{R_{4N}}{R_{2N}} + \frac{R_{4N}}{R_{3N}}\right) \tag{17}$$

and the variance of the gain is given by

$$\sigma^2_\theta = a_1^2\sigma^2_{\frac{R_{1r}}{R_{1N}}} + a_2^2\sigma^2_{\frac{R_{2r}}{R_{2N}}} + a_3^2\sigma^2_{\frac{R_{3r}}{R_{3N}}} + a_4^2\sigma^2_{\frac{R_{4r}}{R_{4N}}} \tag{18}$$

where the subscript r denotes the random part of the variable and the subscript N denotes the nominal part of the variable. The intermediate variables a_1, a_2, a_3 and a_4 are defined by

$$a_1 = \left|R_1\frac{\partial\theta}{\partial R_1}\right| = \frac{R_{2N}}{R_{1N}}\left(1 + \frac{R_{4N}}{R_{2N}} + \frac{R_{4N}}{R_{3N}}\right) \tag{19}$$

$$a_2 = \left|R_2\frac{\partial\theta}{\partial R_2}\right| = \frac{R_{2N}}{R_{1N}}\left(1 + \frac{R_{4N}}{R_{3N}}\right) \tag{20}$$

$$a_3 = \left|R_3\frac{\partial\theta}{\partial R_3}\right| = \frac{R_{2N}}{R_{1N}}\frac{R_{4N}}{R_{3N}} \tag{21}$$

$$a_4 = \left|R_4\frac{\partial\theta}{\partial R_4}\right| = \frac{R_{4N}}{R_{1N}}\left(1 + \frac{R_{2N}}{R_{3N}}\right). \tag{22}$$

If A_{R1}, A_{R2}, A_{R3} and A_{R4} are the areas of $R_1 \ldots R_4$, respectively, it follows after substituting (2) into (18) that

$$\sigma^2_\theta = \left(\frac{A_\rho}{R_{\square N}}\right)^2 \cdot \left(\frac{a_1^2}{A_{R1}} + \frac{a_2^2}{A_{R2}} + \frac{a_3^2}{A_{R3}} + \frac{a_4^2}{A_{R4}}\right). \tag{23}$$

If A_T is the total area, we can express the constraint equation as

$$A_T = A_{R1} + A_{R2} + A_{R3} + A_{R4}. \tag{24}$$

Minimizing the variance in (23) with the constraint of (24), we obtain the optimal area allocations

$$A_{Rk\ \mathrm{OPT}} = \frac{a_k}{\sum_{k=1}^{4} a_k} \cdot A_T, \qquad k = 1,2,3,4 \tag{25}$$

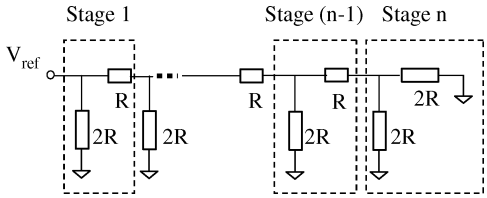

Fig. 6. n-stage R-2R resistance ladder.

Substituting (25) into (23) and combining with (17)–(22), $\sigma^2_{\theta\min/\theta_N}$ is given by

$$\sigma^2_{\frac{\theta\min}{\theta N}} = \left(1 + \frac{1}{\frac{R_{3N}}{R_{4N}} + \frac{R_{3N}}{R_{2N}} + 1}\right)^2 \cdot \frac{4}{A_T} \cdot \left(\frac{A_\rho}{R_{\square N}}\right)^2. \quad (26)$$

Compared to (11), $\sigma^2_{\theta\min/\theta_N}$ for T-feedback network is always larger than that of basic structure, because here the first term in the bracket is always larger than one.

Although the closed form solution appears to be quite simple, when expressed in terms of the component values in the circuit, it becomes quite unwieldy. A numerical comparison of the T-feedback network amplifier with the basic single-stage amplifier and the cascaded structures, all under the assumption of optimal area allocation with the same total resistor area, will now be made. If the magnitude of the overall gain is to be 100, the standard deviation for the basic amplifier is given by $200(A_\rho/R_{\square N}\sqrt{A_T})$, that of a two amplifier cascade is given by $400(A_\rho/R_{\square N}\sqrt{A_T})$, that of a three amplifier cascade is given by $600(A_\rho/R_{\square N}\sqrt{A_T})$ and that of the T-network with $R_2 = R_4 = 10R_1$ and $R_3 = 1.25R_1$ is given by $360(A_\rho/R_{\square N}\sqrt{A_T})$. The deterioration in the standard deviation from that attainable with the basic single-stage amplifier should be apparent.

B. R-2R DAC

The basic R-2R ladder network depicted in Fig. 6, with appropriate termination resistors on the two-port, is widely used in R-2R DACs and other integrated applications because of what most view as two attractive properties. One is the linear increase in area with resolution. The other is the ability to implement the ladder with multiple instantiations of a single unit cell with each additional bit of resolution requiring only 3 additional unit cells. Inherent in the rationale behind this view is the unquestioned premise that the area allocated for each R-2R segment is the same irrespective of the number of bits of resolution of the structure. Consistent with this view are two standard area allocation schemes for implementing the R-2R ladder. One uses two unit cells connected in series to realize each of the "2R" resistors and a single unit cell to realize each of the "R" resistors as depicted in the bit-cell of Fig. 7(a). This is descriptively termed the "conventional series" area allocation strategy. The second area allocation scheme uses two unit cells connected in parallel to form each of the "R" resistors and a single unit cell to realize the "2R" resistors as depicted in Fig. 7(b). This is descriptively termed the "conventional parallel" area allocation strategy.

There are several variant applications of the R-2R network. The question of whether the conventional series or the conventional parallel area allocation offers better performance naturally arises but once this question is raised, the more general

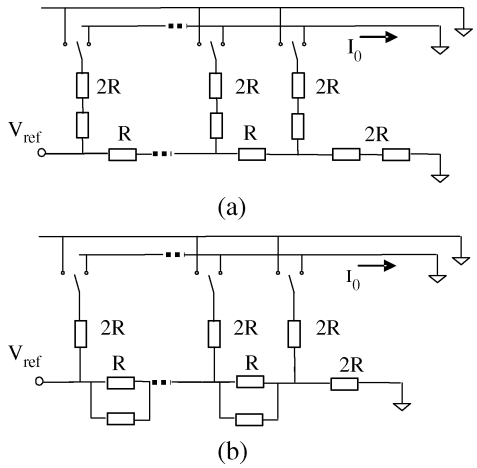

Fig. 7. Conventional (a) series (b) parallel area allocation strategies for R-2R ladder.

question of whether either of these is optimal deserves consideration. In has been previously shown [12], [13] that the conventional series and the conventional parallel area allocations are not optimal in one application. It will also be shown here that the optimal area allocation strategy is application dependent.

An application of the R-2R network in an n-bit DAC that was an $(n-1)$ stage R-2R structure is shown in Fig. 8. This structure has $(2n-1)$ resistors grouped as $(n-1)$ bit slices denoted as slice(2), . . ., slice(n) in the figure. There is one termination resistor, denoted as $R_2(T)$, has been included in the nth bit slice. The DAC ideally has $N = 2^n$ output levels. Since emphasis is on the performance of the R-2R network, it will be assumed that the current sources are all matched and that the op amp is ideal. The linearity of a DAC is one of the most important characteristics of the DAC in many applications. Various metrics are used to characterize the linearity of a DAC. One of the most widely used metrics is the integral nonlinearity (INL), defined relative to a fit line between the end points of the transfer characteristics [14]. The INL is generally expressed relative to the ideal change in the output due to a least significant bit (LSB) change in the Boolean input [14]. This output change is denoted as an LSB change in the output. The endpoint INL in LSB for output k,$0 \le k \le N-1$, is given by

$$\mathrm{INL}_k = \frac{I_k - I_0 - k\left(\frac{I_{N-1}-I_0}{N-1}\right)}{\left(\frac{I_{N-1}-I_0}{N-1}\right)} \quad (27)$$

where I_k is the current I_{OUT} corresponding to the Boolean input with decimal equivalent k. The INL is defined to be the maximum of the absolute values of the INL_k and is formally expressed as

$$\mathrm{INL} = \max_{0\le k\le N-1}\{|\mathrm{INL}_k|\}. \quad (28)$$

The standard deviation of the INL is denoted by σ_{INL}. The INL is a random variable and is the Nth order statistic of the N correlated random variables, $\{|\mathrm{INL_k}|, 0 \le \mathrm{k} \le \mathrm{N}-1\}$. Analytical expressions for statistics of the INL such as σ_{INL} are not mathematically tractable. This information is, however, essential for soft yield prediction and for determining the optimal

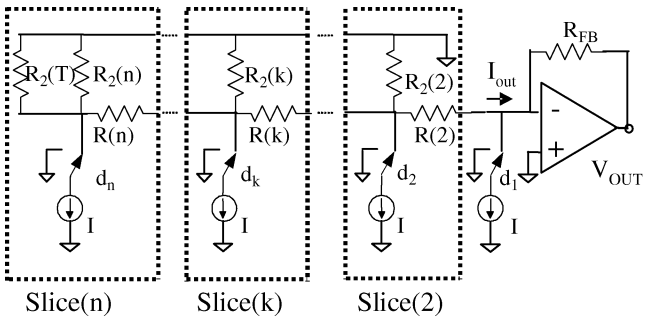

Fig. 8. Equal-current R-2R DAC.

area allocation strategy in the R-2R network. Computer simulations can be used for characterizing the INL. For this characterization it will be assumed that the total area A_T, for an n-bit R-2R ladder is fixed. The optimal area allocation problem for the $(n-1)$ stage R-2R ladder of Fig. 8 is, thus, that of determining the area that should be allocated to each of the $(2n-1)$ resistors in the R-2R ladder so that the standard deviation of the INL, σ_{INL}, is minimized. Formally, if the variables $\{A_1, \ldots A_{2n-1}\}$ denoted the areas of the $(2n-1)$ resistors, then the optimal area allocation problem becomes that of determining $\{A_1, \ldots A_{2n-1}\}$ that will minimize σ_{INL} subject to the constraint $\sum_i^{2n-1} A_i = A_T$. This $(2n-1)$ parameter optimization problem with one constraint is not readily solvable even with a simulator when n is large because of the large number of calculations needed to determine the INL. A near-optimal solution can be obtained, however, by making three simplifying assumptions that will dramatically reduce the dimensions of the optimization space. These assumptions are the following.

1) The ratio of the area allocated to bit slice j, denoted as A_{B_j}, to that allocated to bit slice $(j+1)$, denoted as $A_{B_{j+1}}$ is constant for all $2 \leq j \leq (n-1)$. This ratio can be characterized by the parameter m, thus

$$m = \frac{A_{B_j}}{A_{B_{j+1}}}, \qquad 2 \leq j \leq (n-1). \tag{29}$$

2) The ratio of the area allocated to the "2R" resistor, $R_2(j)$, in bit slice j, denoted as A_{2R_j}, to that of the "R" resistor, in the same bit slice, denoted as A_{R_j}, is constant for bit slice(2) to $(n-1)$. This ratio can be characterized by the parameter k, thus

$$k = \frac{A_{2R_j}}{A_{R_j}}, \qquad 2 \leq j \leq (n-1). \tag{30}$$

3) The ratio of the area allocated to the two "2R" resistors, $R_2(T)$ and $R_2(n)$, denoted as $A_{2R(T)}$ and $A_{2R(n)}$, to that of the "R" resistors, denoted as A_{R_n} in the nth bit slice is k, thus

$$k = \frac{A_{2R(T)} + A_{2R(n)}}{A_{R_n}} = \frac{2A_{2R(n)}}{A_{R_n}}. \tag{31}$$

With these assumptions, the two parameters m and k uniquely determines the area allocation and reduces the size of the optimization space from $(2n-1)$ variables to 2 variables. This two-variable optimization is, thus, that of obtaining values of k and m that minimize σ_{INL}.

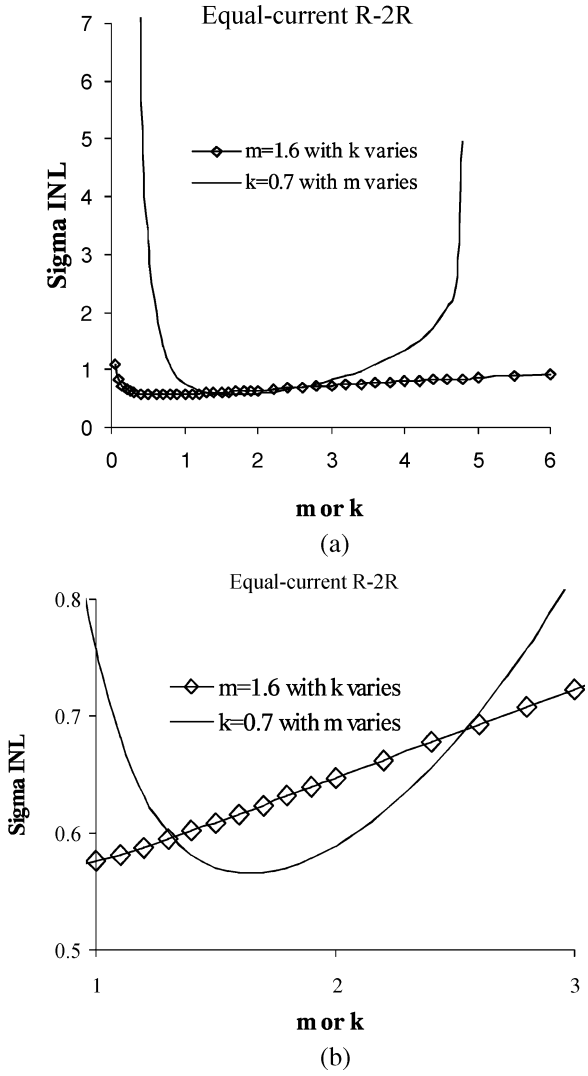

Fig. 9. Sensitivity of standard deviation to m and k of an 8-bit equal-current R-2R DAC. (a) Coarse view. (b) Expanded view.

For convenience, a C-program was developed to perform this optimization using a standard statistical simulation approach. In this simulation, it was assumed that every resistor can be expressed as $R = R_N + R_R$ where R_N is the nominal value and R_R is a random component of the resistor. It was assumed that R_R is a Gaussian variable with mean of zero and standard deviation of $\sigma = (A_\rho / R_{\square N}\sqrt{A_R})$ where the A_R is the area assigned to this resistor as determined by the m and k values and A_T. It can be shown that the optimal values for m and k are not dependent on A_T, A_ρ, or $R_{\square N}$. Thus, for convenience in the optimization, a total area A_T was selected so that a resistor with area A_T will have a standard deviation of 0.1%. For each estimate of (m, k) in the simulation, 10 000 DACs were generated by randomly selecting resistor values from the Gaussian distribution just described. For each of the 10 000 DACs, the INL was determined. The mean and standard deviation of the INLs were computed. With this two-variable optimization, optimal values of m and k were determined to be $m \approx 1.6$ and $k \approx 0.7$. Since k is somewhat less than unity, this would suggest that the conventional parallel layout should give better performance than the conventional series layout. A plot of the standard deviation

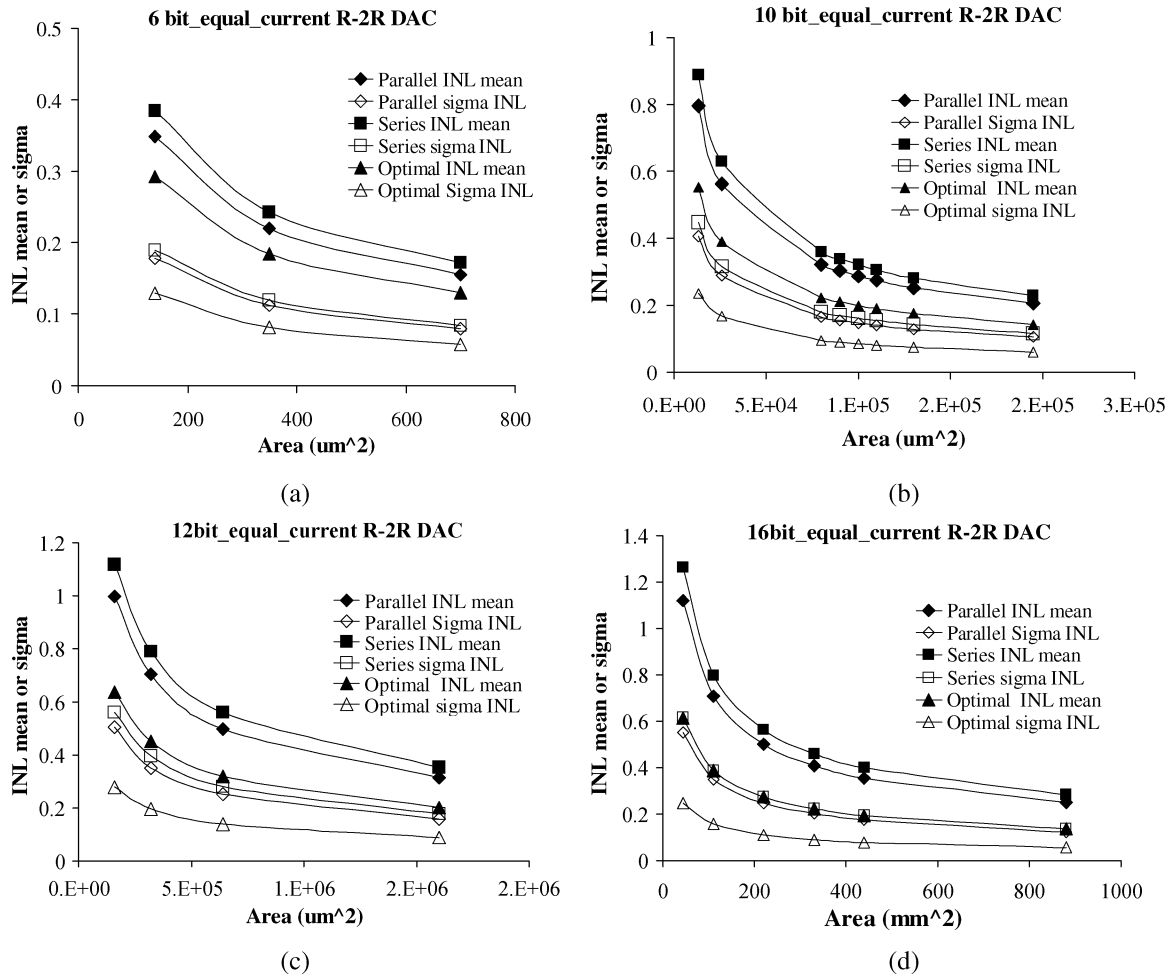

Fig. 10. Mean and sigma of INL of: (a) 6-bit; (b) 10-bit; (c) 12-bit; (d) 16-bit equal-current R-2R DAC.

in the INL versus m for fixed k and versus k for fixed m which shows the sensitivity of the standard deviation to each of these parameters is shown in Fig. 9. The plot in Fig. 9(b) is an expanded version of that of Fig. 9(a). This plot shows that the local minimum is quite shallow in either the m or k variable, suggesting that near optimum performance can be obtained even if m and k differ somewhat from their optimal values but the yield penalty will be quite large if m deviates significantly from the optimum.

It is useful to make a comparison of the optimal area allocation approach with the conventional series and the conventional parallel area allocation strategies discussed earlier. It can be shown that the conventional series strategy is characterized by $m = 1$ and $k = 2$ and the conventional parallel strategy is characterized by $m = 1$ and $k = 0.5$. Fig. 10 shows comparisons of the standard deviation of the INL, σ_{INL}, and the mean of the INL, σ_{INL}, of the optimal area allocation strategy with those of the conventional series and the conventional parallel strategies. For convenience, we have assumed a process with $A_\rho/R_{\square N} = 0.1314\ \mu$m. In this figure, σ_{INL} and μ_{INL} are plotted versus area for different resolution levels. Each point of the curve was obtained from a sample of 10 000 INLs generated by the same method used in the optimization. It can be observed that the conventional parallel layout has a lower standard deviation than the conventional series layout but both are appreciably larger than that of the optimal area allocation strategy. The implications on yield of these differences in standard deviation will be discussed in the next section.

The issue of optimality of the two-variable optimization instead of a $(2n-1)$-variable optimization deserves comments. In related work [12], [13], a more general three-variable optimization of a closely related optimization problem showed little difference between the two-variable and the three-variable optimization. All that we can claim here, however, is that this two-variable optimization results in an area allocation that provides a significant improvement in performance for a given area when compared to a standard area allocation strategy. We do believe however, that two-variable optimization does provide near-optimal values for m and k.

An alternative application of the R-2R ladder in a DAC is shown in Fig. 11. The optimal area allocation and the performance of the optimal structure relative to that of the conventional series and the conventional parallel strategies were considered in [13]. For comparison with the R-2R application of Fig. 8, the previous results will be repeated here. The parameters m and k as defined by (29) and (30) can be used to characterize the R-2R DAC in this application as well. Optimal values of $m \approx 1.7$ and $k \approx 2.2$ were obtained. Although the value of m is comparable to that for the DAC of Fig. 8, the value of k differs significantly suggesting that more area should be al-

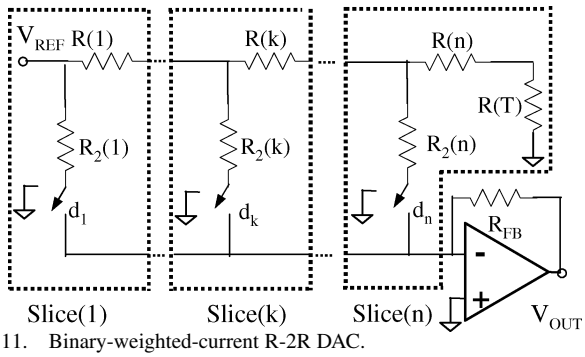

Fig. 11. Binary-weighted-current R-2R DAC.

located to the 2R resistors than to the R resistors in contrast to the results obtained for the circuit of Fig. 8. Since k is somewhat larger than unity, these results also suggest that the conventional series layout should give better performance than the conventional parallel layout for the DAC application of Fig. 11, in contrast to what was observed for the application of Fig. 8. A plot of the standard deviation of INL versus m for fixed k and versus k for fixed m which shows the sensitivity of the standard deviation to each of these parameters is shown in Fig. 12. This plot shows that the local minimum is quite shallow in either of the m or k variable, suggesting that near optimum performance can be obtained even if m and k differ somewhat from their optimal values but the yield penalty will be quite large if m deviates significantly from the optimum. It should be noted by comparing the results in Fig. 9 with those in Fig. 12 that there is a significant difference in the functional form of the INL for the two DAC applications. A yield comparison of the optimal area allocation scheme for the circuit of Fig. 11 with that of the conventional series and the conventional parallel layout is shown in Fig. 13. In this plot the total area for the three allocation schemes is the same and the standard deviation is normalized relative to that of the conventional parallel layout. As conjectured, in contrast to the DAC application of Fig. 8, these results show that the conventional series scheme gives better performance than the conventional parallel scheme. But as for the previous structure, the optimal layout gives considerably better performance than either of the conventional schemes.

These results show that the optimal area allocation strategy for the R-2R network is application dependent. Some applications favor allocating more area to the "R" resistors whereas other favors allocating more area to the "2R" resistors. Both applications, however, show that with a fixed area constraint, it is advantageous to allocate proportionally more area to the most significant bit (MSB) portion of the network than toward the LSB portion. Although the geometric decrease in the scaling of area from the MSB to the LSB gives optimal performance, there are challenges associated with continued scaling of area if the number of bits of resolution is large. It was shown in [13] that the major benefit in performance for the DAC of Fig. 11 is obtained from scaling of the few MSB slices and that near-optimal performance can be obtained if the latter LSB slices are all equally sized and that near-optimal performance can be obtained using a small number of standard unit resistors for arbitrary gain values. The same results apply to the DAC of Fig. 8.

These results can be summarized with the layout principle for the R-2R DACs considered in this section.

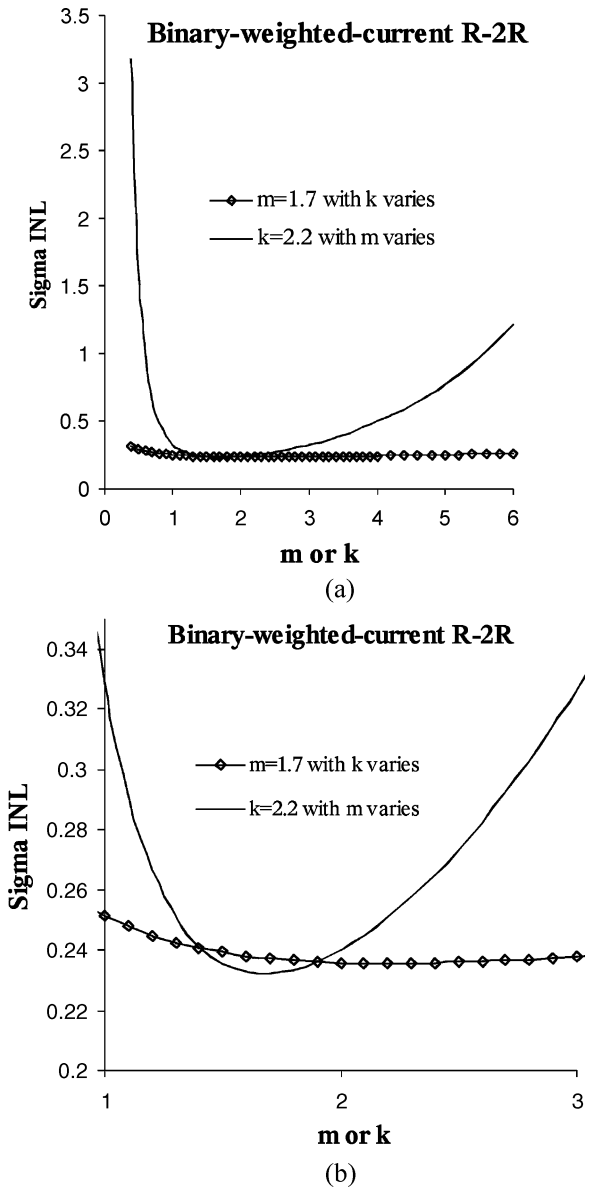

Fig. 12. Sensitivity of standard deviation to m and k of an 8-bit binary-weighted current R-2R DAC. (a) Coarse view. (b) Expanded view.

Layout Principle for R-2R DACs: The effects of local random variations in sheet resistance in the INL for R-2R DACs comprised of rectangular resistors will be minimized for a given total resistor area if proportionally more area is allocated to the more significant bits. But the optimal area allocation is dependent upon how the R-2R network is used. The optimal area allocation for the R-2R DAC of Fig. 8 corresponds to rationing the area between successive bits by 1.6 and maintaining a ratio of the area of the "2R" resistors to the "R" resistors of 0.7. The optimal area allocation for the R-2R DAC of Fig. 11 corresponds to rationing the area between successive bits by 1.7 and maintaining a ratio of the area of the "2R" resistors to the "R" resistors of 2.2.

C. Resistor-String DAC

The resistor-string is also widely used in DACs and these DACs are descriptively termed "R-String DACs" or simply "String DACs." The standard approach of implementing a

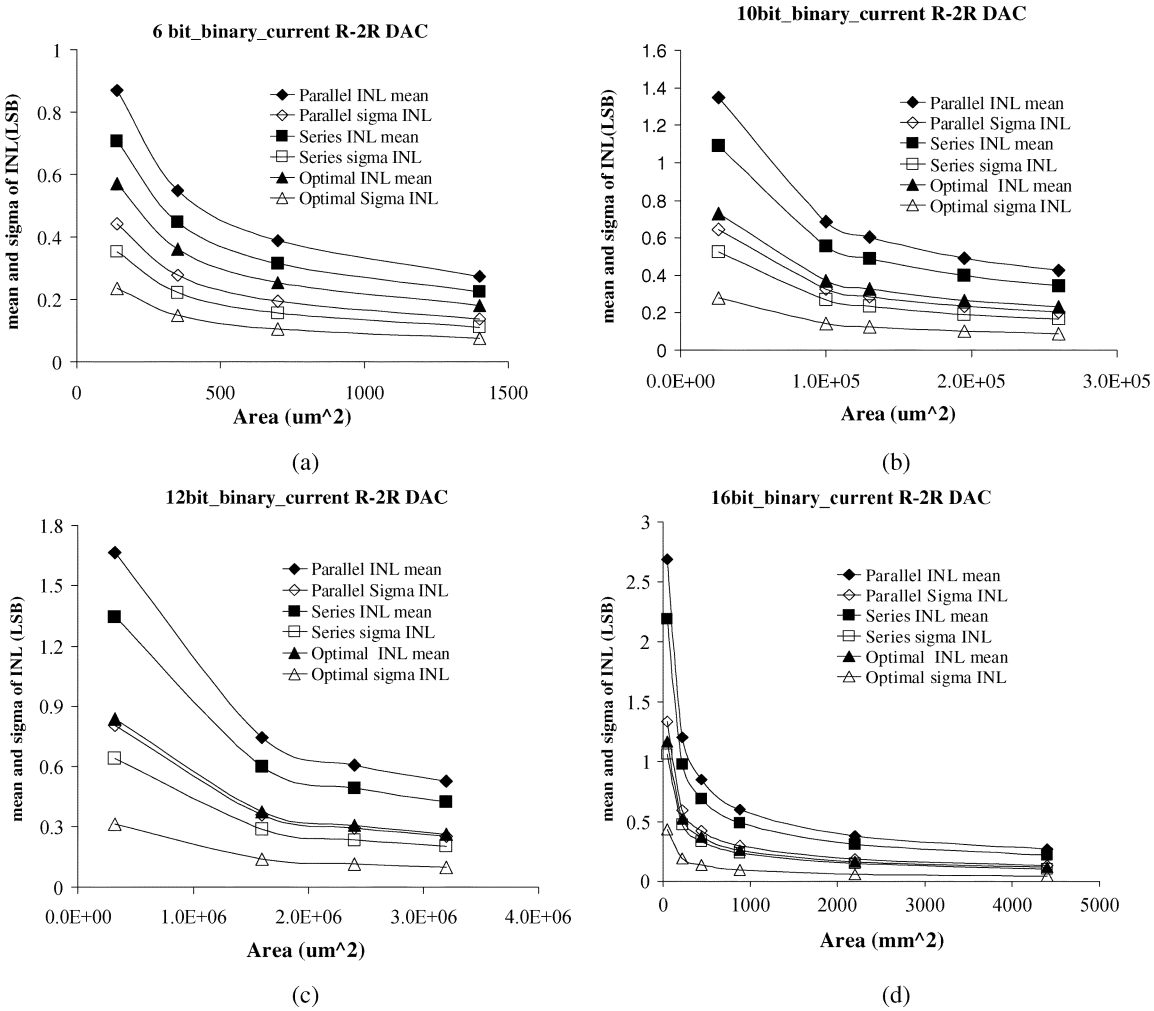

Fig. 13. Mean and sigma of INL of: (a) 6-bit; (b) 10-bit; (c) 12-bit; (d) 16-bit binary-weighted-current R-2R DAC.

resistor string is to allocate equal area to each of the resistors in the R-string. As was the case for the finite gain amplifiers and the R-2R DACs, the question of whether the equal area allocation strategy in string DACs is optimal naturally arises.

The R-string DAC is shown in Fig. 14 where the resistors all have the same nominal value. The DAC has N output levels and the endpoint INL at the kth output, in LSB, is given by

$$\mathrm{INL}_k = \begin{cases} 0, & k = 1, N \\ N \cdot \dfrac{\sum_{i=1}^{k-1} R_i - \frac{k-1}{N-1} \cdot \sum_{i=1}^{N-1} R_i}{\sum_{i=1}^{N} R_i}, & 2 \le k \le N-1 \end{cases}. \quad (32)$$

It will be assumed that the value of each resistor can be expressed as

$$R_i = R_N + R_{ir} \quad (33)$$

where R_N is the nominal value and R_{ir} is the random deviation of resistance R_i from its nominal value. With this notation, if it is assumed that

$$\sum_{i=1}^{N} \frac{R_{ir}}{R_N} \ll N \quad (34)$$

(32) can be rewritten as

$$\mathrm{INL}_k = \sum_{i=1}^{k-1} \frac{R_{ir}}{R_N} \cdot \frac{N-k}{N-1} - \sum_{i=k}^{N-1} \frac{R_{ir}}{R_N} \cdot \frac{k-1}{N-1}. \quad (35)$$

If each resistor has the same area and the random part of the resistors are all uncorrelated and identically distributed with standard deviation σ_{R_r/R_N}, it follows from (35) that the standard deviation of INL_k can be expressed as

$$\sigma_{\mathrm{INL}_k} = \sigma_{\frac{R_r}{R_N}} \cdot \sqrt{\frac{(N-k)\cdot(k-1)}{N-1}} \quad (36)$$

It follows from (2) and (36) that

$$\sigma_{\mathrm{INL}_k} = \frac{1}{\sqrt{A_k}} \cdot \sqrt{\frac{(N-k)\cdot(k-1)}{N-1}} \cdot \left(\frac{A_\rho}{R_{\square N}}\right). \quad (37)$$

It is apparent from (37) that σ_{INL_k} will have a maximum value around $k = (N+1)/2$. Since $(N+1)/2$ is not an integer, the maximum value occurs at $k = N/2$ or $k = (N/2)+1$ and is given by

$$\sigma_{\mathrm{INL}_{k\,\mathrm{MAX}}} = \frac{1}{\sqrt{A_k}} \cdot \sqrt{\frac{N(N-2)}{4(N-1)}} \cdot \left(\frac{A_\rho}{R_{\square N}}\right) \underset{N\ \text{large}}{\cong} \frac{\sqrt{N}}{2\sqrt{A_k}} \cdot \left(\frac{A_\rho}{R_{\square N}}\right). \quad (38)$$

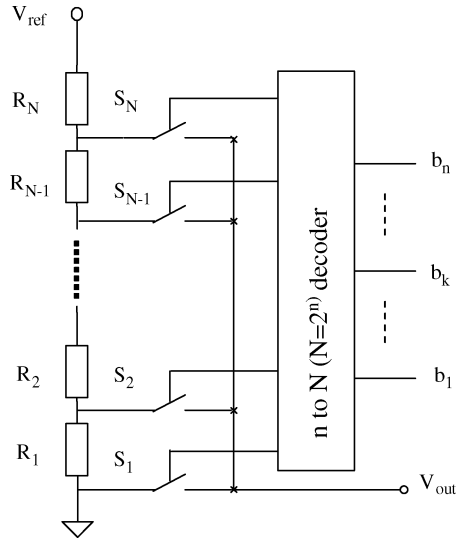

Fig. 14. Symbolic structure of resistor-string DAC.

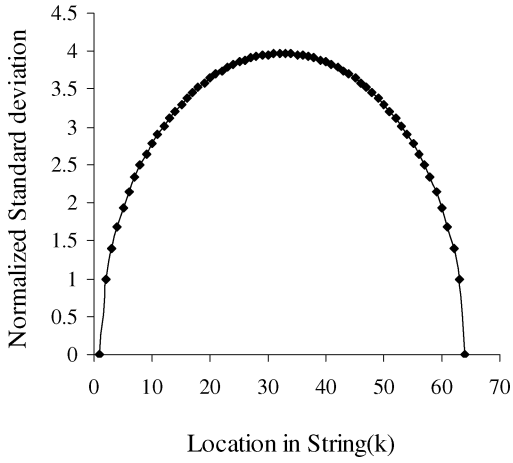

Fig. 15. Plot of normalized standard deviation of INLk for $N = 64$.

A plot of σ_{INL_k} normalized with respect to the process parameters and area (for $N = 64$) appears in Fig. 15. σ_{INL_k} is symmetrical about the midpoint and the peak value increases with increasing resolution.

The plot of Fig. 15 suggests that the INL is strongly dependent upon the maximum of the INL_k, and that it may be possible to reduce the standard deviation in maximum of the INL_k by increasing the area allocated to mid-range resistors in the R-string relative to that of those resistors near the ends of the string. This intuition, however, may be misleading since the simple functional form of (36) was obtained from the more complex summations in (35) under the assumption that the variances of the individual resistors were the same. Of course, the issue of how the INL relates to the INL_k is also of concern.

We will now address directly the issue of minimizing the maximum of the INL_k, or, more specifically, the issue of minimizing the INL_k at the mid-range of the R-string. It follows from (35) that the midrange INL_k is given, for large N, by

$$\mathrm{INL}_{\frac{N}{2}} \cong \frac{1}{2}\sum_{i=1}^{\frac{N}{2}-1}\frac{R_{ir}}{R_N} - \frac{1}{2}\sum_{i=\frac{N}{2}}^{N-1}\frac{R_{ir}}{R_N}. \tag{39}$$

Under the assumption that the random part of the resistor values are uncorrelated, the variance of $\mathrm{INL}_{N/2}$ can be expressed as

$$\sigma^2_{\mathrm{INL}_{\frac{N}{2}}} = \frac{1}{4}\sum_{i=1}^{N-1}\sigma^2_{\frac{R_{ir}}{R_N}}. \tag{40}$$

It follows from (2) that this can be expressed in terms of the area allocated to the ith resistor in the string, A_i, by

$$\sigma^2_{\mathrm{INL}_{\frac{N}{2}}} = \frac{1}{4}\left(\frac{A_\rho}{R_{\square N}}\right)^2\sum_{i=1}^{N-1}\frac{1}{A_i}. \tag{41}$$

If it is assumed that the total resistor area is fixed at A_T, we obtain the constraint equation

$$A_T = \sum_{i=1}^{N} A_i \tag{42}$$

The minimization of $\sigma^2_{\mathrm{INL}_{N/2}}$ with respect to the constraint of (42) results in the solution $A_i = A_T/N$ for all i. This indicates the midrange INL_k will be minimized if the area allocated to all resistors is the same. This suggests that the INL will be minimized if equal area is allocated to each resistor as well. Extensive simulations were conducted in an attempt to verify that the equal area allocation strategy also minimizes the INL. The simulation time required for minimizing the INL with respect to the area is very large even for modest values of N so lower-dimensional parameterized optimizations were explored in which proportionally more as well as proportionally less area was allocated to resistors near the middle of the string. In all cases these parameterized optimizations resulted in a larger INL than what was obtained for equal area allocation. It is, thus, conjectured that the INL is minimized when equal area is allocated to each resistor in the R-string.

These results can be summarized with the layout principle for R-strings.

Layout Principle for Resistor Strings: The effects of local random variations in sheet resistance in the INL for Resistor String DACs comprised of rectangular resistors will be minimized for a given total resistor area if equal area is allocated to each of the resistors.

III. Contact Resistance Issue

The previous discussions were based upon the explicit assumption that the dominant contributor to mismatch is the random variations in the sheet resistance. In particular, the effects of random variations in contact resistance and edge variations of the resistor body were neglected. In this section, the effects of random variations in contact resistance will be considered and the effects of edge variations of the resistor body will be discussed.

With the feature sizes of the process decreasing, the sizes of the contacts are also decreasing and correspondingly the contact resistance is increasing as is the variance of the contact resistance. Unfortunately, the statistical variation of the contact resistance from one contact to the next is quite large. The effects of the random effects of the contact resistance and the combined effects of the random effects of the contact resistance and the

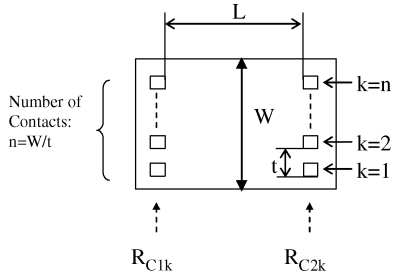

Fig. 16. Rectangular film resistor with contacts.

sheet resistance will be considered in this section. It will be assumed that the contact resistance can be modeled as the sum of a nominal component and a random component where the nominal component is assumed to be the same for all contacts in a matching critical region. It will be further assumed that the random components are uncorrelated from one contact to the next. This latter assumption, which is essentially equivalent to neglecting gradient effects, will not significantly affect the results that will be developed in this section.

Fig. 16 shows a symbolic layout of a rectangular resistor. In the figure, W and L are the width and length of the film resistor and t is the pitch of the contacts. If W is large enough, the number of contacts, n, is approximately given by

$$n = \frac{W}{t}. \tag{43}$$

A tedious but straightforward analysis (see the Appendix) provides a good approximation of the variance of a reference resistor which includes the effects of both the random variations in the sheet resistance and the random variations in the contact resistance

$$\sigma^2_{\frac{R_{\rm UR}}{R_{\rm UN}}} \approx \left(\frac{2R^2_{\rm CN}}{n^3\left(\frac{2R_{\rm CN}}{n}+R_{\rm SHN}\right)^2}\right)\cdot\sigma^2_{\frac{R_{\rm CR}}{R_{\rm CN}}} + \left(\frac{R^2_{\rm SHN}}{\left(\frac{2R_{\rm CN}}{n}+R_{\rm SHN}\right)^2}\right)\cdot\sigma^2_{\frac{R_{\rm SHR}}{R_{\rm SHN}}}. \tag{44}$$

In this expression, $R_{\rm UN}$ is the nominal resistance value of unit resistor cell, $R_{\rm UR}$ is the random component of the cell resistance, $R_{\rm CN}$ is the nominal value of the resistance of a single contact, $R_{\rm CR}$ is the random component of a single contact resistance, $R_{\rm SHN}$ is the nominal value of resistance of the sheet resistor film, and $R_{\rm SHR}$ is the random component of the sheet resistance. The term $\sigma^2_{R_{\rm CR}/R_{\rm CN}}$ is the variance of the local random component of the contact resistance and is a constant characteristic of the process.

The first term on the right-hand side (RHS) of (44) is the contribution from the variance of the contact resistance and the second term is the contribution from the variation of the sheet resistance.

A standard cell is widely used in matching critical applications so that gradient effects can be cancelled by connecting an appropriate number of these standard cells in an appropriate series or parallel way to form a common-centroid layout. Although this approach will increase the total area and increase the effects of edge variations, it is usually justifiable because of the importance of minimizing gradient effects. If the resistor layout of Fig. 16 is used as a unit cell, this cell has an area $A_{\rm RU}$. If k of these resistors are placed in parallel or if k of these resistors are placed in series and it is assumed that the local random variations of both the sheet resistance and contact resistances are uncorrelated, it can be shown that the normalized standard deviation of the parallel or series combination is

$$\sigma_{\frac{R_{\rm kR}}{R_{\rm kN}}} = \frac{1}{\sqrt{k}}\sigma_{\frac{R_{\rm UR}}{R_{\rm UN}}} \tag{45}$$

where $R_{\rm kR}$ is the random part of the parallel or series combination, $R_{\rm kN}$ is the nominal resistance of the parallel or series combination.

Equation (45) was developed under the assumption that the local random variations of the sheet resistance and contact resistance are uncorrelated, and in this case the relationship between $\sigma^2_{R_{\rm UR}/R_{\rm UN}}$ is given by (44). However, it can be shown that (45) is applicable even if random edge variations are included or if correlations exit between the sheet resistance and the contact resistance, provided the random variations in the resistance of the unit cells are uncorrelated. The area of the parallel or series combination relates to the area of the unit cell by

$$A_{\rm kRU} = {\rm k}A_{\rm RU}. \tag{46}$$

Substituting (46) into (45), we obtain the expression

$$\sigma_{\frac{R_{\rm kR}}{R_k}} = \frac{1}{\sqrt{A_{\rm kRU}}}\cdot\left(\sqrt{A_{\rm RU}}\cdot\sigma_{\frac{R_{\rm UR}}{R_{\rm UN}}}\right). \tag{47}$$

The first factor on the RHS of (47) is the reciprocal of the square root of the area of the unit cell and the term in brackets is a constant characteristic of the process. This same expression holds for a parallel series array of unit cells as well. All resistances in this expression include the combined effects of the sheet resistances and the contact resistances. A comparison of (47) to (2) indicates they are of the same functional form. Specifically the normalized standard deviation of an array of parallel or series or parallel-series connected unit cells is equal to the reciprocal of the square root of the total area multiplied by a parameter that is characteristic of the process alone. All of the derivations in the previous sections for the amplifiers, the R-2R networks, and the R-string DACs were dependent only upon the functional relationship of (2), specifically the fact that the normalized standard deviation of a component is proportional to the reciprocal of the square root of the area times a process dependent constant. Thus, all of the results of the previous section are directly applicable to unit cells that contain the local random effects of both the contact resistance and the sheet resistance. This relationship was developed under the assumption that the resistor is rectangular with a nominally homogenous sheet resistance and, thus, nominally uniform current density. Thus, the layout principle for ratio-matched resistors can be restated to include the effects of the random variations of the contact resistance and the effects of edge variations as follows.

Layout Principle for Ratio-Matched Resistors (Including Contact Resistance Effects): The combined effects of local random variations in sheet resistance, contact resistance and edge variations in the ratio matching accuracy of two resistors will be minimized for a given total resistor area if an equal number of unit cells, connected in a parallel, series, or parallel-series configuration, are allocated to the two resistors.

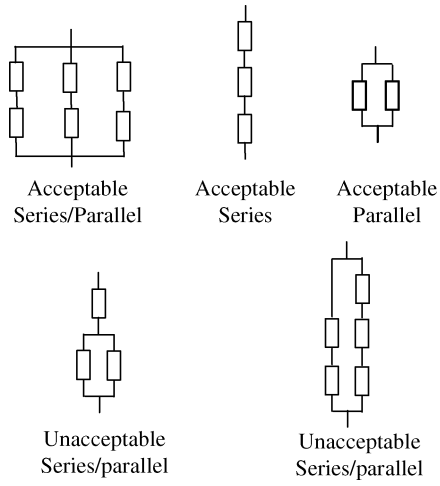

Fig. 17. Examples of acceptable and unacceptable series, parallel, and series/parallel implantation.

By a parallel, series, or parallel series configuration of cells to form a resistor, we mean a connection where the nominal current is the same in each unit cell of the resistor. Fig. 17 shows acceptable and unacceptable parallel, series and parallel/series connections.

Equation (47) does not provide an explicit relationship for the variance in terms of process parameters. The effects of edge variations on the unit cell will be negligible if L and W are large. Drennan [15] suggests, at least in some processes, the effects of width variations are negligible even if L is small. A parametric expression for $\sigma_{R_{\rm UR}/R_{\rm UN}}$ showing the effects of edged variations on the unit cell, if of concern for a given process, can be readily derived following the approach of Pelgrom [6] or Drennan [15].

We will now concentrate on an explicit expression for the variance of the unit cell in terms of the sheet resistance and contact resistance process parameters. This can be obtained by substituting (1), (2) and (43) into (44) to obtain

$$\sigma^2_{\frac{R_{\rm UR}}{R_{\rm UN}}} = \frac{1}{\rm WL}\cdot\left(\frac{2\cdot R^2_{\rm CN}\cdot\sigma^2_{\frac{R_{\rm CR}}{R_{\rm CN}}}\cdot t^3\cdot L + L^2\cdot A^2_\rho}{(2R_{\rm CN}\cdot t + R_{\square N}\cdot L)^2}\right) \quad (48)$$

where W and L are dimensions of the unit cell as depicted in Fig. 16. Finally, by substituting (47) into (48), we obtain an expression for the variance of a resistor of value R that is formed by a series, parallel, or series-parallel connection of k unit cells.

$$\sigma^2_{\frac{R}{R_N}} = \frac{1}{A_{\rm kRU}}\cdot\left(\frac{A_{\rm RU}}{\rm WL}\right)\cdot\left(\frac{2\cdot R^2_{\rm CN}\cdot\sigma^2_{\frac{R_{\rm CR}}{R_{\rm CN}}}\cdot t^3\cdot L + L^2\cdot A^2_\rho}{(2R_{\rm CN}\cdot t + R_{\square N}\cdot L)^2}\right). \quad (49)$$

Note the term in parenthesis in (49) differs slightly from unity since the effective length and the drawn length differ because of the presence of the rows of contacts on each end of the resistor as shown in Fig. 16.

It is not apparent from (48) whether the random variations in the sheet resistance or the random variations in the contact resistance are dominant. For small unit cells, the contact resistance and the contact resistance variations will dominate whereas for larger cells the sheet resistance and the sheet resistance variations will dominate. We will now determine the physical characteristics of the cell that represents a transition from contact resistance variance dominated to sheet resistance variance dominated. To determine this, it can be observed from (48) that the leftmost summand in the numerator is the contribution of the contact resistance variation and the rightmost summand is the contribution of the sheet resistance contribution. Crossover between contact resistance dominated and sheet resistance dominated will occur when these two terms are equal. Equating these terms we find that the width plays no role (provided W is wide enough that the assumption of (43) is valid) in the crossover and obtain the critical length as

$$L_{\rm crit} = \frac{2\cdot R^2_{\rm CN}\cdot\sigma^2_{\frac{R_{\rm CR}}{R_{\rm CN}}}t^3}{A^2_\rho}. \quad (50)$$

If we assume the pitch of the contact is 4λ, (50) can be rewritten as

$$L_{\rm crit} = \frac{2^7\cdot\lambda^3\cdot R^2_{\rm CN}\cdot\sigma^2_{\frac{R_{\rm CR}}{R_{\rm CN}}}}{A^2_\rho}. \quad (51)$$

As can be seen from (51), the critical length is a process parameter. When the length of the resistor is larger than $L_{\rm crit}$, the variation of sheet resistance will dominate the contribution to the variance and when smaller, the contact resistance variations will dominate.

Good statistical information about a process is essential for predicting parametric yield. Test structures that can be used to measure parameters such as A_ρ and $\sigma^2_{R_{\rm cr}/R_{\rm CN}}$ are necessary for process characterization. Since these parameters characterize local process variations and not gradient effects or process variations from die to die, from wafer to wafer, or from process lot to process lot, different test structures are needed to extract these parameters. Some results [16] relating to extracting these parameters have been reported in the literature but it is the authors' experience that this information is often missing from a description of the technology provided by many foundries. It is also the authors' experience that those responsible for extracting this information at several major semiconductor companies either do not have test structures that are needed to extract this information or do not distinguish between the effects of local and global mismatch. The issue of propriety further limits the availability of this information in the open literature. On smaller unit cells, however, the contact resistance variations significantly dominate those of the sheet resistance variations as governed by (51).

IV. Yield Analysis

Parametric yield predictions are strongly dependent upon the statistical distributions of the random variables affecting yield. In this work, the amplifiers discussed in Section II have a gain that has a random component with a nearly Gaussian distribution. In contrast, the INL of the n-bit R-2R DAC is an Nth order statistics of N non-Gaussian correlated random variables where $N \approx 2n$. In the former case, closed form expression relating yield to the standard deviation of the Gaussian variables can be readily derived. Closed form expression for the yield of the R-2R DAC is not mathematically manageable. In this section we

will derive expression for the yield of the amplifier structures. Graphical results will be presented to compare yield potential of the R-2R DACs.

A. Yield of Feedback Amplifier Structures

The statistical analysis in the preceding sections is used primarily to predict yield of the feedback amplifier structures. In this section, the benefits of optimal area allocation will be discussed. It is well known that if x is a performance parameter of interest and if $\Delta\mu$ defines the yield tolerance window on the parameter x about a specified value of μ, then the parametric yield with respect to random variations in the parameter x can be expressed as

$$Y = \int_{\mu-\Delta\mu}^{\mu+\Delta\mu} f(x)\mathrm{d}x \tag{52}$$

where f(x) is the probability density function (pdf) of x.

The local random variations of parameters such as the sheet resistance and the contact resistance can be approximated with a zero-mean Gaussian distribution provided that the total parameter variation is somewhat smaller than the nominal value of the parameter. With this approximation, it is convenient to express the yield, Y, in terms of the normalized random variable $\tilde{x} = (x - \mu)/\sigma$ where σ is the standard deviation as

$$Y = \int_{-\frac{\Delta\mu}{\sigma}}^{\frac{\Delta\mu}{\sigma}} f_n(\tilde{x})\mathrm{d}\tilde{x} \tag{53}$$

where $f_n(\tilde{x})$ is the PDF of the zero-mean unit-variance normal distribution generally designated with the distribution notation $N(0,1)$. In terms of the normalized Gaussian cumulative probability density function (cdf) $F_n(x)$, it follows from (53) that

$$Y = 2 \cdot F_n\left(\frac{\Delta u}{\sigma}\right) - 1 \tag{54}$$

The yield of the ratio-based area allocation strategy for the basic amplifier of Fig. 2 is compared with that of the optimal area allocation strategy in Fig. 18 for different closed-loop gains. In the yield comparison, it has been assumed that a good amplifier must have a gain specification that is within 1% of the target value. Since the conventional series and the conventional parallel area allocations give the same yield, a distinction between these two strategies is not necessary. In this comparison, the total area for the resistors was the same and the total area was set at the level needed to obtain a 99% yield with the optimal area allocation. Although one might argue that even for the gain of 100, the yield drop is only a factor of approximately 2, the impact of this yield drop is most significant. For example, if an integrated circuit had an array of 100 gain of 5 amplifiers with total area allocated to obtain a yield of 99% for each of the amplifiers with optimal area allocation, the amplifier parametric yield would be $Y_{\mathrm{OPT}} = (0.99)^5 = 95\%$ whereas if the same total area were allocated to the conventional ratio-based allocation scheme, the yield would drop to $Y = (0.39)^5 = 0.9\%$. The importance of doing a statistical analysis when making an area allocation should be apparent from this simple example.

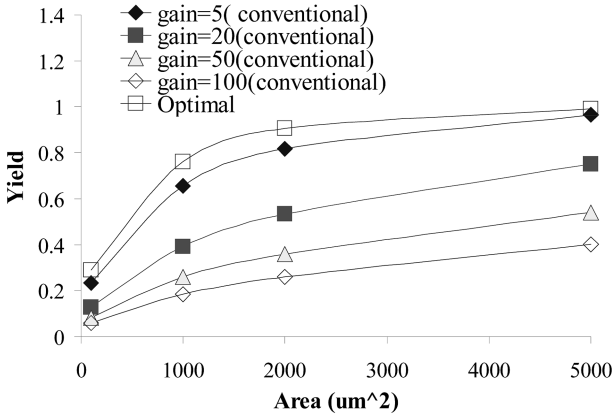

Fig. 18. Yield of feedback amplifier.

Of equally importance is the realization that significant yield penalties or equivalently area increases will be incurred if conventional area allocation strategies are used when the gain of the amplifier is large.

A comparison of the ratio-based area allocation scheme for the cascaded amplifiers and the T-feedback amplifier is made with that of the optimal area allocation scheme in Fig. 19. In these comparisons, the total area was the same for each architecture and the area was allocated to obtain a 99% yield with the basic single-stage amplifier optimal area allocation. Fig. 19 also shows a comparison of the yield for the conventional architecture with that of the cascaded amplifiers and that of the T-feedback amplifier. A series layout with $R_1 = R_3$ and $R_2 = R_4$ was assumed for the T-feedback amplifier. Included in this figure are the yields that would be obtained if the conventional ratio-based area allocations were used. The impact of both architecture and area allocation on yield should be apparent from this figure.

B. Yield of R-2R DACs

The yield of the R-2R ladder DAC of Fig. 8 for the conventional series and the conventional parallel area allocations are compared with that of the optimal area allocation of $m = 1.6$ and $k = 0.7$ in Fig. 20 for varying levels of resolution. In this comparison, it has been assumed that a good R-2R DAC must have an INL less than 0.5 LSB. A similar comparison [13] for the ladder of Fig. 11 with optimal values of $m = 1.7$ and $k = 2.2$ is shown in Fig. 21. It should be apparent from Fig. 21 and Fig. 20 that significant improvements in yield can be obtained if an optimal area allocation strategy is used. Finally, Fig. 22 shows a comparison of the yield of the two R-2R networks. In this figure, the networks are compared using the conventional series, the conventional parallel and the optimal area allocation layouts for different levels of resolution. This comparison shows that the relative yield is bit-level and area dependent. When the resolution is high, the yield improvement is more significant. It was also shown that he optimal area allocation for the R-2R DAC of Fig. 8 offers higher yield than the optimal area allocation for the structure of Fig. 11. The smooth curve of the yield and area relationship is intuitively expected. If a resistor has area A_1 or A_3 with A_3 larger than A_1, then it will have smaller standard deviation of resistance with A_3 than

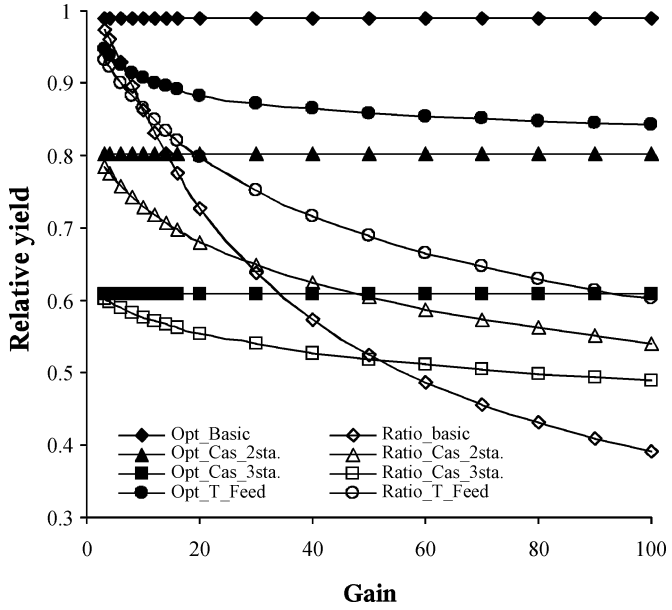

Fig. 19. Yield of different configuration for feedback amplifier. "Opt" denotes optimal area allocation for a given structure; "Ratio" denotes a ratio-based area allocation strategy.

that with A_1. If a resistor has area of A_2 whose value is between A_1 and A_3, then the standard deviation of resistance is also in between.

It should be observed that in the yield comparisons, the issue of the relative role of the variations in sheet resistance and in contact resistance was intentionally not raised nor was the issue of the values for the parameters that characterize the local mismatch effects. The yield comparisons were intentionally all made in the relative sense so that the results apply in the general case since the values of the process parameters have been normalized out. Although not explicitly stated, it has been assumed in the yield assessment that a unit cell was used to form all resistors and that larger resistors were obtained with series/parallel connections of the unit cell.

V. Effects of Optimal Area Allocation on Other Circuit Properties

The issue of what effect optimal area allocation has on other circuit characteristics deserves consideration. Since optimal area allocation results were all dependent only upon how area is distributed between various components and not upon the component values themselves, the designer has the option of keeping all resistance values the same as in the original circuit or scaling the resistance values when adopting an optimal area allocation approach. If the designer chooses to leave the impedance values unchanged, then the circuit schematic remains unchanged and essentially all other circuit characteristics will remain unchanged as well, except possibly for some second-order effects due to a change in parasitic in the optimal area approach. If the designer chooses to also scale the impedance values, however, when using the optimal area allocation approach, the resultant circuit schematic will change and this change could affect other characteristics of a circuit such as linearity, power dissipation, signal swing, etc.

VI. Practical Layout Considerations

The layout principles for area allocation that optimize parametric yield for ratio-matched resistors and for R-2R networks give little guidance on how the layout should be done to achieve optimal performance and in many applications, it will be difficult to practically allocate area to achieve optimal yield. It should be re-emphasized that a common centroid layout is generally necessary to minimize the effects of linear gradient effects, that an interconnection of unit cells should be used to minimize the effects of length and width variations as well as contact resistance variations, and that well-known layout matching methods such as maintaining a common cell orientation, maintaining appropriate interconnect matching, and managing peripheral or dummy peripheral devices are important. Fortunately, it was also shown that the standard deviation of the performance metrics discussed earlier have a rather shallow minimum and, as such, near-optimal performance can be obtained even if the optimal area allocation is not precisely achieved.

The layout of the feedback resistors for an amplifier with an integer gain such as 4 or 16 is easy to achieve with optimal area allocation. For example, the gain of 4 can be achieved using two unit cells connected in series for one resistor and two unit cells connected in parallel for the second resistor and a common centroid layout of these 4 cells is straightforward. It is difficult to achieve equal area ratios, however, with some other gain values. For example, an exact area ratio of 1 with a gain of 5 or 10 can not be readily achieved but for the gain of 5, five unit cells can be connected in series to form one resistor and the parallel combination of two strings of two resistors can be used to form the second resistor. This will result in an area ratio of 1.25 or a value of $\gamma = 0.444$ which provides near-optimal performance as can be seen from Fig. 4. A gain of 10 can be achieved by connecting 10 unit cells in series to form one resistor and by connecting three strings of three resistors in series to form the second resistor to achieve a value of $\gamma = 0.47$.

A layout of the R-2R network to achieve the precise area allocation for minimizing the standard deviation of the INL with an interconnection of a practical number of unit cells can not be realized. As with the ratio matching problem, however, near-optimal performance can be obtained with practical unit cell based common centroid layouts. In the R-2R network, the biggest benefits are obtained by maintaining slice area ratios close to the optimum on the first few most significant bits in the network with little additional benefits derived from optimal area scaling for the latter bits in the network. As an example, consider the R-2R network of Fig. 11 with the optimal values of $m = 1.7$ and $k = 2.2$. If area were assigned to an 8-bit R-2R array to achieve a yield with optimal area allocation of 97.4%, simulation results show that the yield for the standard series connection with the same total area would be 66.3% and the standard parallel connection with the same total area would provide a yield of 80.1%. If the "2R" resistor in the MSB block is realized with a parallel series connection of 18 unit cells (parallel connection of 3 strings of 6 resistors), the "R" resistor in the MSB block is realized with a parallel series connection of 9 unit cells (parallel connection of 3 strings of 3 resistors), the "2R" resistor in the second MSB block is realized with a parallel series combination of 8 unit cells and the "R" resistors in

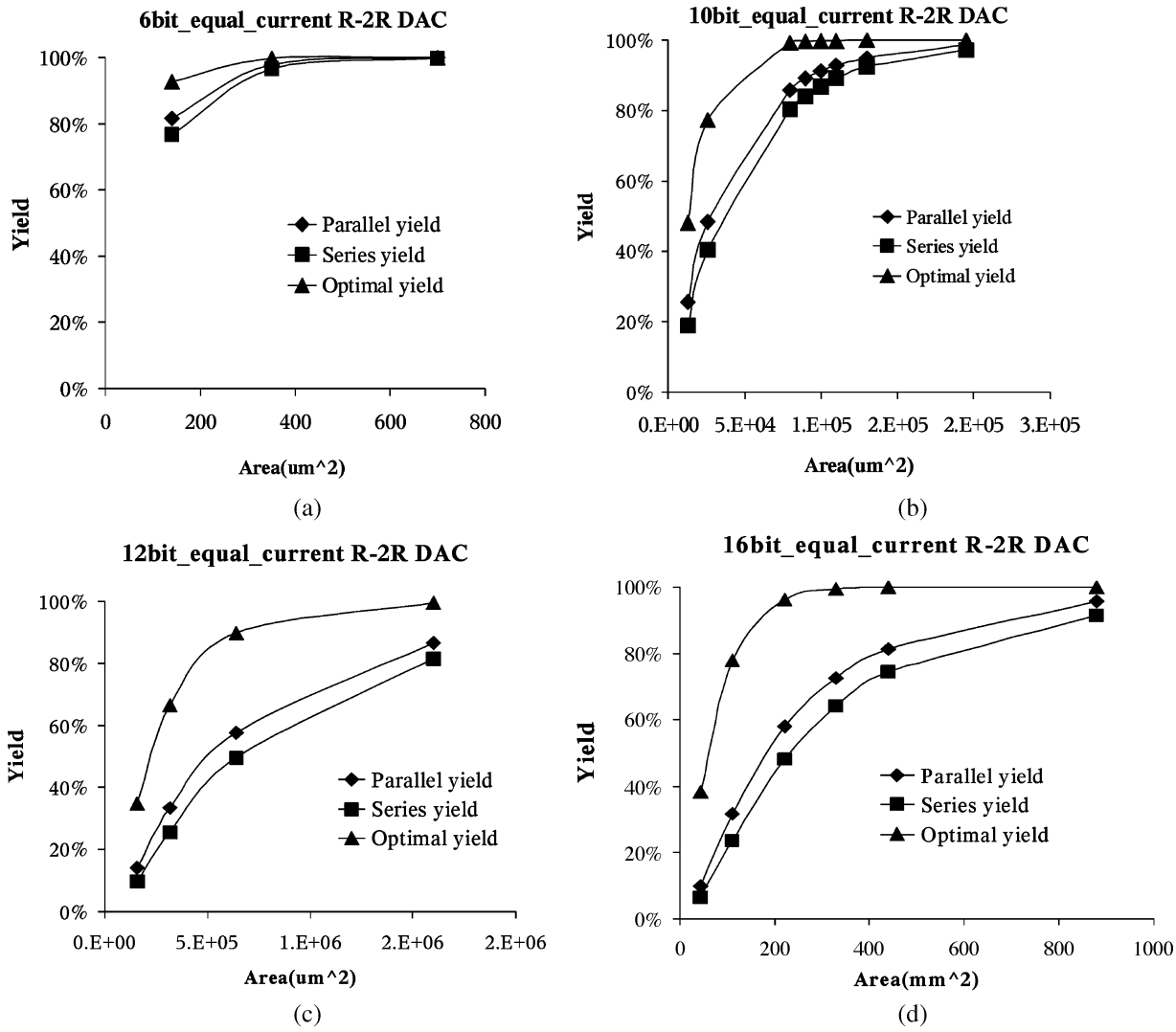

Fig. 20. Yield of (a) 6-bit; (b) 10-bit; (c) 12-bit; (d) 16-bit equal-current R-2R DACs.

the second MSB block is realized with a parallel series connection of 4 unit cells, all remaining "2R" resistors are realized with the series combination of 2 unit cells, and all remaining "R" resistors are realized with a single unit cell, simulation results show the yield will be 95.1%. Although not quite at the optimal value of 97.4%, near-optimal yield is achieved with a unit cell approach that is practical and that can be layed out in a common-centroid configuration. For notational convenience we term this the $\langle 18, 9, 8, 4, 2, 1, 2, 1, 2, 1, 2, 1, 2, 1, 2, 2\rangle$ standard cell allocation strategy. If instead of scaling just the two MSBs, the first three MSBs are scaled with a parallel series connection using the $\langle 32, 16, 18, 9, 8, 4, 2, 1, 2, 1, 2, 1, 2, 1, 2, 2\rangle$ standard cell allocation strategy, simulation results show that the yield will be increased to 96.7%.

VII. Extensions

The concepts of optimal area allocation for ratio-sensitive resistor networks can be extended to ratio-sensitive transistor or capacitor structures but with some restrictions. Such extensions will be briefly discussed in this section.

A feedback amplifier using MOS transistors biased in the triode region to form the feedback network is shown in Fig. 23. The nominal gain of the amplifier is given by

$$A_{\mathrm{G}} = \frac{R_{\mathrm{FETB}}}{R_{\mathrm{FETA}}} \tag{55}$$

where R_{FETA} and R_{FETB} are the triode-region impedances of M_A and M_B, respectively. These impedances are approximately given by

$$R_{\mathrm{FET}} = \frac{L}{(V_{\mathrm{GS}} - V_T) \cdot \mu \cdot C_{\mathrm{OX}} \cdot W} \tag{56}$$

where W and L are the width and length of the transistor, V_T is the threshold voltage, $V_{\mathrm{GS}} - V_T$ is the excess bias voltage of the transistor, μ is the mobility, and C_{OX} is the oxide capacitance density. If the random variation of the edges of the channel is neglected, the local random deviations of V_T, μ and C_{OX} have a standard deviation proportional to the square root of the channel area given by [4]

$$\sigma_{\frac{\mu}{\mu_N}} = \frac{A_\mu}{\sqrt{A}} \tag{57}$$

$$\sigma_{\frac{V_T}{V_{\mathrm{TN}}}} = \frac{A_{V_T}}{\sqrt{A}} \tag{58}$$

$$\sigma_{\frac{C_{\mathrm{ox}}}{C_{\mathrm{oxN}}}} = \frac{A_{\mathrm{Cox}}}{\sqrt{A}} \tag{59}$$

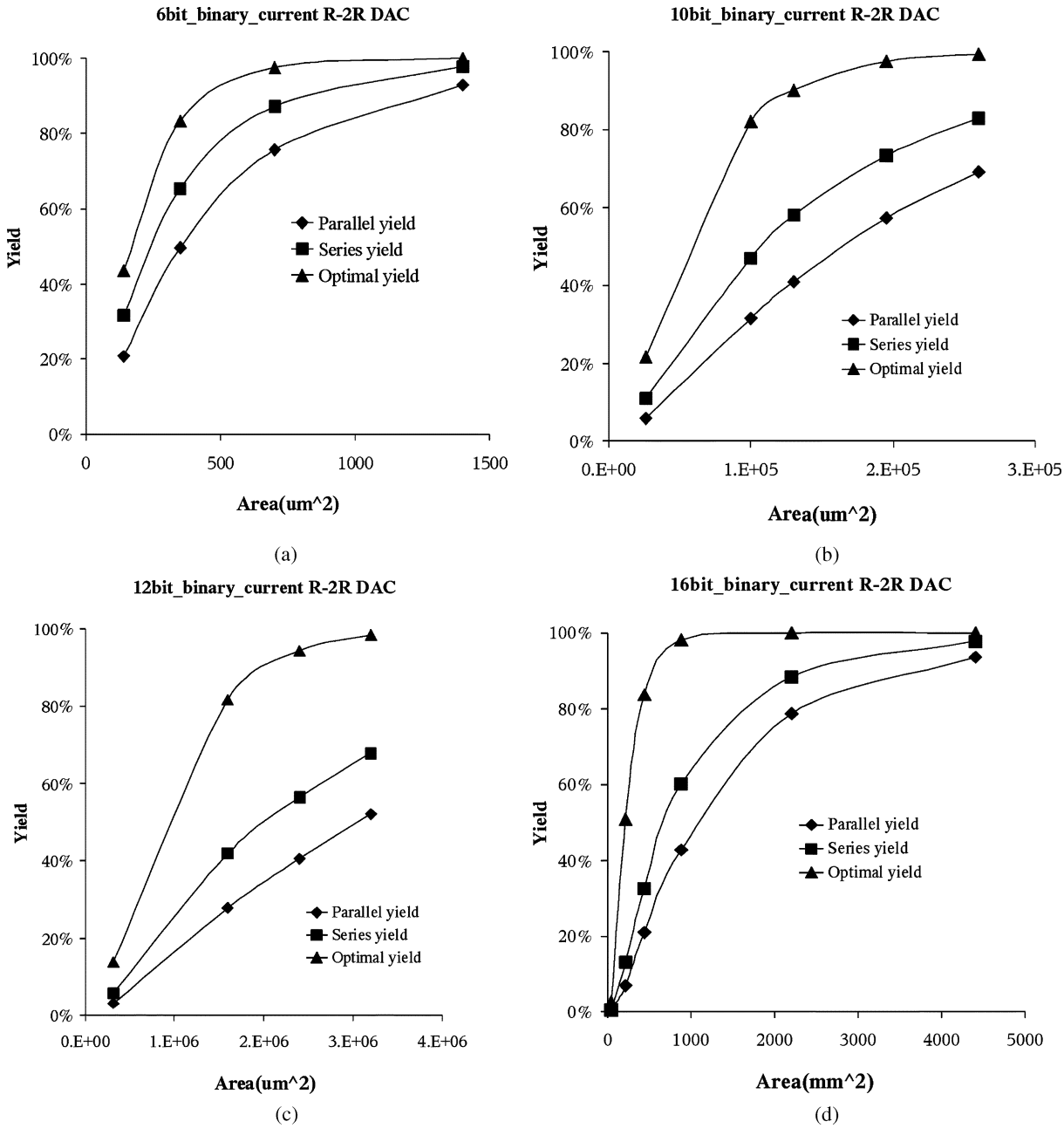

Fig. 21. Yield of (a) 6-bit; (b) 10-bit; (c) 12-bit; (d) 16-bit binary-weighted-current R-2R DACs.

where the subscript N means nominal value, the parameters A_μ. $A_{\rm VT}$ and $A_{\rm Cox}$ are process parameters characterizing the standard deviation of μ, V_T, and $C_{\rm OX}$ and A is the area of the channel area of the transistor. If these two transistors are biased with the same excess bias voltages, it follows from a straightforward derivation that the normalized standard deviation of the gain can be expressed as

$$\sigma_{\frac{A_{\rm G}}{A_{\rm GN}}} = \sqrt{\left(A_\mu^2 + A_{C_{\rm OX}}^2 + \frac{V_{\rm TN}^2 A_{V_T}^2}{(V_{\rm GSN} - V_{\rm TN})^2}\right) \cdot \left(\frac{1}{A_A} + \frac{1}{A_B}\right)} \tag{60}$$

where A_A and A_B are the channel areas for transistors $\rm M_A$ and $\rm M_B$, respectively, and where $V_{\rm GSN} - V_{\rm TN}$ is the nominal excess bias voltage. If the total channel area of $\rm M_A$ and $\rm M_B$ is fixed, it follows that the standard deviation will be minimized when the area of transistors area equal. This is the same result that was obtained for the layout of resistors. As with the resistors, a unit transistor cell would be used and parallel and series interconnections of these cells would be used to realize the elements of the feedback network.

A basic current mirror is shown in Fig. 24. The nominal current mirror gain is given by the expression

$$A_{\rm MN} = \frac{W_B L_A}{W_A L_B}. \tag{61}$$

If again the random variations of the edges of the channel are neglected, it can be shown that the normalized standard deviation of the mirror gain is given by

$$\sigma_{\frac{A_{\rm M}}{A_{\rm MN}}} = \sqrt{\left(A_\mu^2 + A_{C_{\rm OX}}^2 + \frac{4V_{\rm TN}^2 A_{V_T}^2}{(V_{\rm GSN} - V_{\rm TN})^2}\right) \cdot \left(\frac{1}{A_A} + \frac{1}{A_B}\right)}. \tag{62}$$

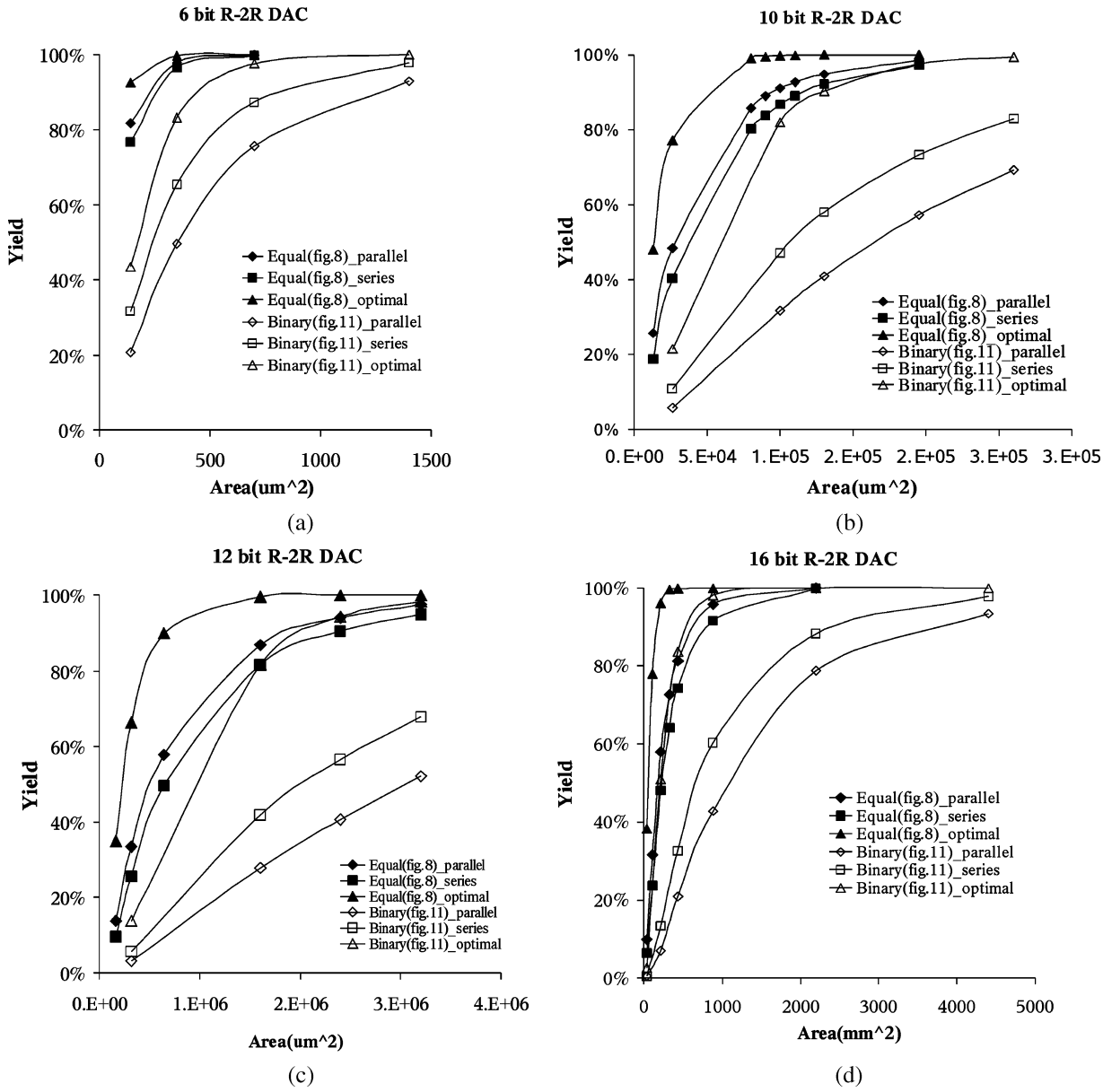

Fig. 22. Yield of (a) 6-bit; (b) 10-bit; (c) 12-bit; (d) 16-bit R-2R DACs.

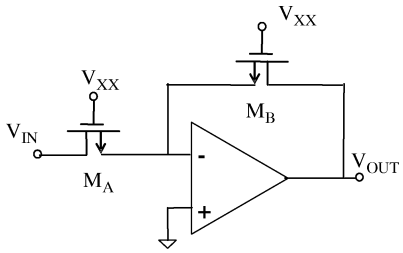

Fig. 23. Basic transistor feedback amplifier.

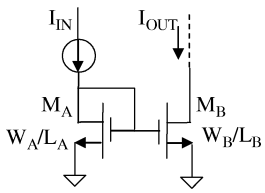

Fig. 24. Basic current mirror.

This RHS of (62) is similar to that of (60) and, thus, it can be concluded that the standard deviation of the mirror gain will be minimized for a given total channel area if the channel area of the input and output devices of the mirrors are the same.

The issues of variance and absolute accuracy are distinct and a particular layout or area allocation strategy that minimizes standard deviation may not necessarily give the best overall accuracy. For example, three circuits that provide a nominal current mirror gain of 4 are shown in Fig. 25. In all cases, multiple instantiations of a unit transistor cell are used to form the input and output devices. The circuit of Fig. 25(a) is the most common and all devices have essentially the same gate and source voltages. The circuit of Fig. 25(b) is an equal area allocation strategy and will provide the smallest variance in the mirror gain. The source voltage of the upper cell on the input is, however, different than that of the other 3 cells. The source voltages for the three upper

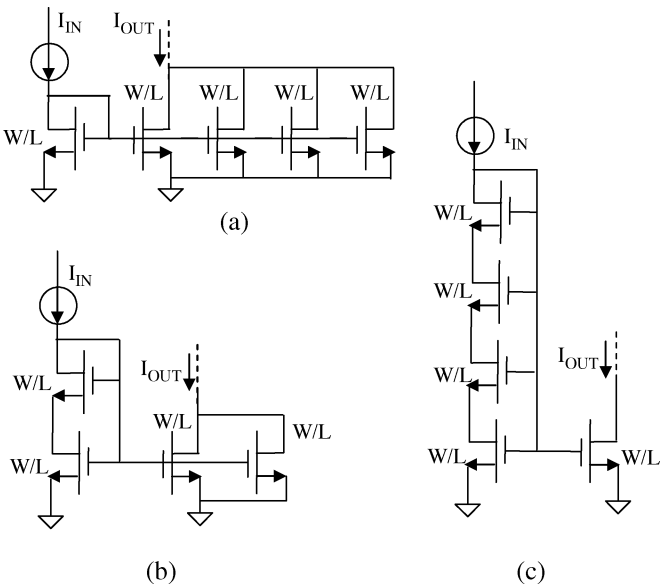

Fig. 25. Different area allocation scheme for current mirrors with current gain = 4.

cells on the input side in the circuit of Fig. 25(c) are all different and different from those of the other two cells. The systematic error in the mirror gains may not be the same for the different area allocation schemes but the equal area allocation scheme will exhibit the smallest standard deviation.

Accurately controlling capacitor ratios is also of concern as is the parametric yield for analog circuits that depend upon accurate capacitor ratios. In contrast to a resistor in which the area and resistor value of a rectangular device can be independently established, a rectangular capacitor (or actually any arbitrarily shaped parallel plate capacitor) has a capacitance value that is uniquely determined by and proportional to the capacitor area. As a result, the component-ratio based area allocation scheme in which the area is allocated in proportion to the capacitor ratio is almost exclusively used for the layout of ratio-matched capacitors irrespective of whether the capacitor is a standard planar vertical structure or a thick-metal MEM device. If the parameter $\theta = C_1/C_2$ defines the ratio of two capacitors, the component-ratio area allocation requirement establishes a constraint in the relationship between the area of the capacitors and the total area given by

$$A_{\mathrm{C1}} = \left(\frac{\theta_N}{1+\theta_N}\right) A_T$$
$$A_{\mathrm{C2}} = \left(\frac{1}{1+\theta_N}\right) A_T \tag{63}$$

where θ_N is the nominal capacitor ratio and A_T is the total area. In what follows the discussion will be restricted to the vertical planar capacitor although similar results apply to lateral MEM structures as well. If it is assumed that the local random variations in the capacitance density are due to variations in the oxide thickness, it follows that the standard deviation of the ratio is given by

$$\sigma_\theta = \frac{A_{\mathrm{C}}}{\sqrt{A_T}} \cdot (1+\theta_N)\sqrt{\theta_N} \tag{64}$$

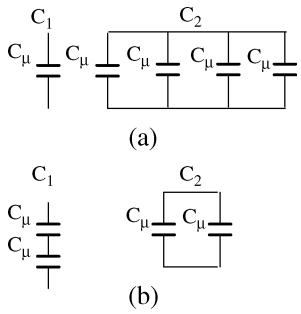

Fig. 26. Different area allocation scheme for capacitor ratio of 4.

where A_{C} is a constant dependent upon the process that characterizes the local random variations in the capacitance density. This equation is similar to that of (7) for the gain of an amplifier with resistive feedback and, thus, it can be concluded that the yield penalty will be quite significant if capacitors ratios significantly different than 1 are required as was shown in Fig. 4.

As was the case for the resistor ratios, the standard deviation for the capacitor ratio can be expressed in terms of the area of capacitor C_1, A_{C1}, as

$$\sigma_\theta = \theta_N A_{\mathrm{C}} \cdot \sqrt{\frac{1}{A_{C_1}} + \frac{1}{A_T - A_{C_1}}} \tag{65}$$

If the component-ratio constraint of (63) could be removed, then (65) could be minimized with respect to A_{C1} to obtain the area allocation strategy for minimizing the standard deviation which is

$$A_{\mathrm{C1}} = A_{\mathrm{C2}} = \frac{A_T}{2}. \tag{66}$$

Paralleling the results for the ratio matching of resistors, it follows on substituting (66) into (65) that the minimum standard deviation is given by

$$\sigma_{\theta\,\min} = 2\theta_N \frac{A_{\mathrm{C}}}{\sqrt{A_T}}. \tag{67}$$

Comparing with (64) it follows that for large or small values of θ_N, the minimum given by (67) is considerably lower than that obtained for the component-ratio area allocation scheme.

If ideal capacitors are available, an equal area allocation scheme or a nearly equal area allocation scheme can be used. For example, the circuit of Fig. 26 shows a standard area allocation scheme and an optimal area allocation scheme for a 4:1 capacitor ratio. Whether the optimal area allocation scheme is practical or even feasible does, however, depend on applications. In many applications the floating capacitor node would cause unacceptable parasitic and/or charge accumulation that would either be unacceptable or that could possibly cause device failure.

VIII. Conclusion

Area-allocation between components in matching-critical applications has received minimal attention in the literature. Optimal area allocation strategies for several practical applications including finite gain amplifiers, R-2R networks, R-string DACs, and current mirrors have been introduced. It has been shown that

the optimal area allocation strategies can provide a significant reduction in variance for a fixed total area in some useful applications and, thus, a significant increase in yield when compared to more standard area allocation schemes that are based upon the component ratios. It was also shown that the random component of the contact resistance is of growing concern in applications requiring ratio-matched resistors and strategies for minimizing the variance due to contact resistances were also developed.

APPENDIX

A. Contact Resistance Modeling

Consider the rectangular resistor with (n) contacts on each side shown in Fig. 16. If the resistance in the metal is neglected, the total resistance of this resistor can be approximated by

$$R \approx \frac{1}{\sum_{k=1}^{n} \frac{1}{R_{C1_k}}} + R_{SH} + \frac{1}{\sum_{k=1}^{n} \frac{1}{R_{C2_k}}} \tag{A1}$$

where R_{SH} is the resistance contributed by the thin film sheet resistance, R_{C1k} is the resistance of the kth contact on the left-hand side of the structure, and R_{C2k} is the resistance of the kth contact on the RHS of the structure.

Neglecting any gradient effects in the sheet resistance and the contact resistances, resistors R_{SH}, R_{C1k} and R_{C2k} can be expressed as

$$R_{SH} = R_{SHN} + R_{SHR} \tag{A2}$$

$$R_{C1k} = R_{CN} + R_{C1kR} \qquad k = 1, \ldots, n \tag{A3}$$

$$R_{C2k} = R_{CN} + R_{C2kR} \qquad k = 1, \ldots, n \tag{A4}$$

where R_{SHN} is the nominal resistance contribution from the thin film sheet resistance, R_{SHR} is the random component of R_{SH}. R_{CN} is the nominal value of the local contact resistance, R_{C1kR} is the random component of R_{C1k} and R_{C2kR} is the random component of R_{C2k}.

It will be assumed that the random components of the contact resistances are uncorrelated. From (A3), it follows that

$$\sum_{k=1}^{n} \frac{1}{R_{C1_k}} = \sum_{k=1}^{n} \frac{1}{R_{CN} + R_{C1_{kR}}} = \frac{1}{R_{CN}} \sum_{k=1}^{n} \frac{1}{1 + \frac{R_{C1_{kR}}}{R_{CN}}}. \tag{A5}$$

Since the random component of the contact resistance is small compared to the nominal component, a power series expansion for each of the terms can be used to linearize the sum in (A5). Thus, by neglecting second- and higher-order terms in this expansion, we obtain

$$\sum_{k=1}^{n} \frac{1}{R_{C1_k}} \approx \frac{1}{R_{CN}} \sum_{k=1}^{n} \left(1 - \frac{R_{C1_{kR}}}{R_{CN}}\right) = \frac{n}{R_{CN}} \left(1 - \frac{1}{n} \sum_{k=1}^{n} \frac{R_{C1_{k_R}}}{R_{CN}}\right). \tag{A6}$$

By repeating the power series expansion process, it follows that

$$\frac{1}{\sum_{k=1}^{n} \frac{1}{R_{C1_k}}} \approx \frac{R_{CN}}{n} \left(1 + \frac{1}{n} \sum_{k=1}^{n} \frac{R_{C1_{k_R}}}{R_{CN}}\right). \tag{A7}$$

A similar approach can be used to obtain

$$\frac{1}{\sum_{k=1}^{n} \frac{1}{R_{C2_k}}} \approx \frac{R_{CN}}{n} \left(1 + \frac{1}{n} \sum_{k=1}^{n} \frac{R_{C2_{k_R}}}{R_{CN}}\right). \tag{A8}$$

Substituting (A2), (A7) and (A8) in (A1), it follows that

$$R \approx \frac{2R_{CN}}{n} + R_{SHN} + \frac{R_{CN}}{n^2} \left(\sum_{k=1}^{n} \frac{R_{C1kR}}{R_{CN}} + \sum_{k=1}^{n} \frac{R_{C2kR}}{R_{CN}}\right) + R_{SHR}. \tag{A9}$$

It follows from (A9) that the nominal value of the resistor is

$$R_N = \frac{2R_{CN}}{n} + R_{SHN} \tag{A10}$$

and the random component of the resistor is

$$R_R \approx \frac{R_{CN}}{n^2} \left(\sum_{k=1}^{n} \frac{R_{C1kR}}{R_{CN}} + \sum_{k=1}^{n} \frac{R_{C2kR}}{R_{CN}}\right) + R_{SHR}. \tag{A11}$$

If it is assumed that the random components of the contact resistance are identically distributed, it follows that

$$\sigma^2_{\frac{R_{C1kR}}{R_{CN}}} = \sigma^2_{\frac{R_{C2kR}}{R_{CN}}} = \sigma^2_{\frac{R_{CR}}{R_{CN}}}. \tag{A12}$$

Since the random variable in (A11) are assumed to be uncorrelated, it follows from (A9), (A10), (A11), and (A12) that the value of the resistance R can be approximated by

$$\sigma^2_R = \sigma^2_{R_R} \approx \frac{R^2_{CN}}{n^4} \left(2 \cdot n \cdot \sigma^2_{\frac{R_{CR}}{R_{CN}}}\right) + \sigma^2_{R_{SHR}}. \tag{A13}$$

Or equivalently as

$$\sigma^2_R \approx \frac{2R^2_{CN}}{n^3} \cdot \sigma^2_{\frac{R_{CR}}{R_{CN}}} + R^2_{SHN} \sigma^2_{\frac{R_{SHR}}{R_{SHN}}}. \tag{A14}$$

By dividing both sides of (A14) by R^2_N, we can obtain an expression for the variance of the normalized resistance R/R_N, which takes the form

$$\sigma^2_{\frac{R}{R_N}} \approx \frac{2R^2_{CN}}{n^3 \left(\frac{2R_{CN}}{n} + R_{SHN}\right)^2} \sigma^2_{\frac{R_{CR}}{R_{CN}}} + \left(\frac{R^2_{SHN}}{\left(\frac{2R_{CN}}{n} + R_{SHN}\right)^2}\right) \sigma^2_{\frac{R_{SHR}}{R_{SHN}}}. \tag{A15}$$

REFERENCES

[1] A. Hastings, *The Art of Analog Layout*. Englewood Cliffs, NJ: Prentice-Hall, 2000.

[2] A. Grebene, *Bipolar and MOS Analog Integrated Circuit Design*. New York: Wiley, 1994.

[3] M. Ismail and T. Fiez, *Analog VLSI Signal and Information Processing*. New York: McGraw-Hill, 1994.

[4] J. Shyu, G. Temes, and F. Krummenacher, "Random error effects in matched MOS capacitors and current sources," *IEEE J. Solid State Circuits*, vol. SC-19, pp. 948–955, Dec. 1984.

[5] W. Lane and G. Wrixon, "The design of thin-film polysilicon resistors for analog IC applications," *IEEE Trans. Electron Devices*, vol. 36, pp. 738–744, Apr. 1989.

[6] M. Pelgrom, A. Duimaijer, and A. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. SC-24, pp. 1433–1440, Oct. 1989.

[7] K. Lakshmikumar, R. Hadaway, and M. Copeland, "Characterization and modeling of mismatch in MOS transistors for precision analog design," *IEEE J. Solid-State Circuits*, vol. SC-21, pp. 1057–1066, Dec. 1986.

[8] Y. Lin and R. Geiger, "Resistor layout techniques for enhancing yield in ratio-critical monolithic applications," in *Proc. IEEE Midwest Symp. Circuits and Systems*, vol. 1, Aug. 2001, pp. 259–262.

[9] A. Sedra and K. Smith, *Microelectronic Circuits*. New York: Oxford Univ. Press, 1998.
[10] S. Kuboki, K. Kato, N. Miyakawa, and K. Matsubara, "Nonlinearity analysis of resistor string A/D converters," *IEEE Trans. Circuits Syst.* , vol. CAS-29, no. 6, Jun. 1982.
[11] A. Pergoot, B. Graindourze, E. Janssens, J. Bastos, M. Steyaert, P. Kinget, R. Roovers, and W. Sansen, "Statistics for matching, microelectronic test structures," in *Proc. 1995 Int. Conf.*, Mar. 1995, pp. 193–197.
[12] Y. Lin and R. Geiger, "Resistor Layout for Enhancing Yield in R-2R DACs," in *IEEE Int. Symp. Circuits and Systems*, vol. 5, May 2002, pp. V-97–V-100.
[13] Y. Lin and R. Geiger, "Area allocation strategies for enhancing yield in R-2R ladders," *J. Analog Integrated Circuits and Signal Processing*, vol. 37, no. 2, pp. 123–132, Nov. 2003.
[14] *IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters*, 2001.
[15] P. Drennan, "Diffused resistor mismatch modeling and characterization," in *Bipolar/BiCMOS Circuits and Technology Meeting*, Sep. 1999, pp. 27–30.
[16] P. Drennan and C. McAndrew, "Understanding MOSFET mismatch for analog design," *IEEE J. Solid State Circuits*, vol. 38, no. 3, pp. 450–4456, Mar. 2003.

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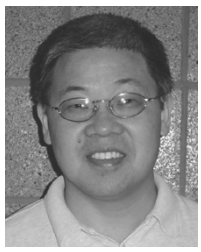

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