# Dynamic Calibration of Current-Steering DAC

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***Abstract*—High accuracy Digital to Analog Converters (DACs) are becoming increasingly important as the common used building block in communication systems. With the increasing of the update rate, dynamic performance of such DACs at high frequencies is of particular interest. The dynamic performance is often characterized by the spurious free dynamic range (SFDR) and the SFDR is limited by the spectral harmonics which are attributed by system nonlinearities. In this paper, the dynamic nonlinearity is analyzed and its effect on the output waveform is discussed. A novel approach is presented to calibrate the dynamic errors. The validity of this approach is demonstrated with a 15-bit current steering DAC. Simulation results show that the approach is robust and the SFDR can be correspondingly significantly improved by using this calibration scheme.**

## I. INTRODUCTION

In signal processing and telecommunication systems, high accuracy Digital to Analog Converters (DAC) are becoming more and more important. The DAC is used to reconstruct an analog signal from an arbitrary digital waveform. This key part often limits the accuracy and speed of the overall system. Several different architectures are used to build the DACs. Amongst them, the resistor-loaded current-steering DAC is exclusively used when high speed and high accuracy are required. In communication applications, DAC quality is often determined by the high frequency spectral purity of the output signal and this is dominantly determined by the nonlinearities of the DAC. The spurious free dynamic range (SFDR) is a widely used measure for the linearity of the converter [1].

SFDR degrades with both static and dynamic nonlinearities. The main static errors arise from the current sources mismatch and their finite output impedances. These error sources cause inaccurate settling of DAC outputs. The current source mismatch is mainly due to the random variations that can be attributed to local random variations and gradient effects [2]. Special layout and placement techniques, such as common centroide technique, judicious switch sequencing, and $Q^2$ random walks [3]-[5] can be used to reduce these effects. Even if the current sources are perfectly matched, the output current of the current sources may still vary with the output voltage because the finiteness of the output impedance of the current sources. Strategies exist for improving the output impedance of the current source. For example, cascoded current sources and current-steering switches can be used to increase the output impedance.

Many calibration approaches [2], [5], [6] have been reported in the literatures for improving DAC performance focusing mainly on reducing the static nonlinearity. In higher frequency ranges, little has been presented to lower the dynamic nonlinearities [7]. Some modest improvements in high frequency SFDR have been reported with return-to-zero structures (RTZ) at the expense of sacrificing half of the signal power.

For video and wireless telecommunication applications, both static linearity and dynamic linearity are important because the static and dynamic nonlinearities contribute to the undesired harmonics in the DAC output. In this paper, a novel dynamic DAC nonlinearity calibration approach is proposed that can improve high frequency SFDR without attenuation of the output signal power by compensating dynamic errors at the output with extra pulses. Simulation results from a prototype 15-bit current-steering DAC are used to validate this approach.

## II. DYNAMIC NONLINEARITIES ANALYSIS AND CALIBRATION APPROACH

In a DAC, nonlinearities exist during transient. The influence of the nonlinearities on the distortion performance of the DAC can be described in both time and frequency domain. In time domain, the static nonlinearities are dominantly attributable to nonlinear settling artifacts in the output such as insufficient settling time while the dynamic nonlinearities are caused by timing skew, slewing and glitches, etc.

Dynamic properties are given by the transition between two states. Most of these occur at the start of the transition period. As the input signal frequency or the sampling frequency increases, the dynamic nonlinearity components become larger, so the linearity degrades and the magnitude of SFDR decreases. In order to improve the SFDR of the DACs, the effects of the dynamic nonlinearities must be reduced. Cong in her paper [2] improved low and high frequency SFDR with very low power and small area. The

approach is good at low frequency but the SFDR still degrades quickly with increasing frequency. Bugeja's structure [7] improved dynamic linearity at high frequency by using "attenuate and track" approach. But this improvement is at the price of a factor of 2 in the signal power. The main reason of the improvement of dynamic linearity in Bugeja's approach is primarily due to the suppression of the prior code dependence. So measures can be adopted to improve the dynamic linearity without lose of signal power.

The dynamic distortion is caused by the nonlinear behavior of the DAC. The nonlinear behavior can be modeled as a function of the input sequence. The errors E at the output of the DAC can be expressed as

$$E=f(A_0, A_1, \ldots, A_{n-1}, A_n, \ldots) \quad (1)$$

where $A_0, A_1, \ldots, A_{n-1}, A_n, \ldots$ is the input sequence. For most DACs, the output error is primarily attributed by the present input code and the previous input code, i.e. for an input code of $A_n$, the error will be given by $E=f(A_{n-1}, A_n)$. The error can be divided into two categories: one occurs during the transition region between two consecutive changing states which can be called dynamic glitch error caused by the nonlinearities during this region, the other is the dynamic settling error attributed to the variation of the DAC output settled value compared to the desired one. Both of them are present input code, $X_n$, and the difference, $X_{diff}$, dependent. Here $X_{diff}$ is the difference between the present code and previous code, $X_{n-1}$, $X_{diff}= X_n- X_{n-1}$. The actual DAC output can be regarded as:

$$I_{out} = I_{ideal} - I_d \quad (2)$$

Where $I_{out}$ is the DAC actual output, $I_{ideal}$ is the ideal output, $-I_d$ is the error caused by nonlinearities. $-I_d$ includes the dynamic glitch error and dynamic settling error.

The basic idea of our approach is to generate an amount of current with the same magnitude but opposite sign to $-I_d$ from a dynamic calibration DAC, then an ideal output can be obtained by adding the current to the original DAC to compensate the nonlinearity error.

Fig. 1 shows the architecture of a DAC with its dynamic calibration. It consists of a static error calibrated DAC as used by Cong in [2], a Dynamic Calibration DAC and a delay block. The Dynamic Calibration DAC block is divided into dynamic settling block and dynamic glitch block. The dynamic settling block includes Dynamic Settling Error (DSE) and Dynamic Settling Error Calibration DAC (DSE Cal DAC), the dynamic glitch block includes Dynamic Glitch Error (DGE) and Dynamic Glitch Error Calibration DAC (DGE Cal DAC) block. The delay block is used to get the previous code $X_{n-1}$ for dynamic calibration. Based on $X_n$ and $X_{diff}$, the dynamic glitch error will obtained from DGE then the current pulses $I_{ds}$ will be generated from DGE Cal DAC and similarly $I_{gs}$ for dynamic settling error compensation will be generated. These pulses will be then added to the original static calibrated DAC output. The raw

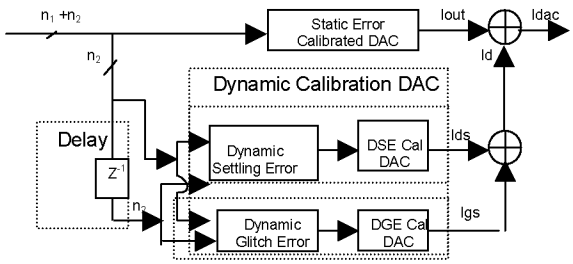


Fig.1 DAC calibration scheme

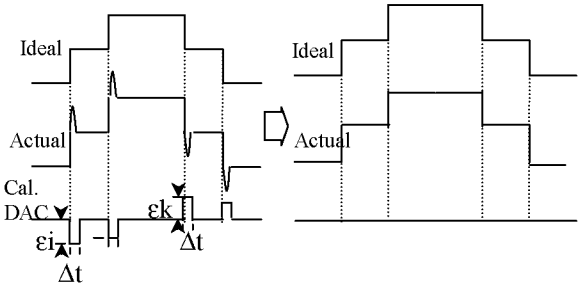


Fig.2 MSB glitch calibration conceptual illustration

DAC is segmented into a most significant bit (MSB) part ($n_2$-bit) and a least significant bit (LSB) part ($n_1$-bit). The thermometer decoding is used in the MSB part to reduce the output glitches. The LSB part is implemented with a binary structure.

For the dynamic settling error calibration, the compensation pulse width $\Delta t_{st}$ is the same as the clock period $T_s$ and the pulse height is the mean variation between the output settled value and the desired output value but opposite sign. The dynamic glitch error width is very narrow compared to the clock period. The error can be simply modeled as glitches with certain width and height for every states transition and can be compensated by narrow pulses. Fig.2 shows a conceptual illustration of the dynamic glitch calibration. If a waveform that is a vertical flip of the glitches can be generated and added to the output waveform at each transition period, the glitches can be canceled perfectly. But it is hard to generate such an analog waveform, so digital pulses are used to compensate the glitches. For simplicity, just one pulse is used to compensate the glitches for every MSB code variation in this paper. The width and the magnitude of the pulse can be set as $\Delta t$ and $\varepsilon_i$ respectively. $\varepsilon_i$ is related to the input code $X_i$ and the two successive input codes difference $X_{diff}$. For each input code and step height, there is a corresponding $\varepsilon_i$ value to compensate the glitches. So a look-up-table can be used to save the calibration pulse magnitude values. A look-up-table can be built for dynamic settling error values in the similar way. After the calibration, the nonlinearities will reduce and the SFDR will improve.

The following is the approach of generating the look-up-tables for dynamic glitch error, $E_{dyn}(x_n, x_{diff})$, and for dynamic settling error, $E_{set}(x_n, x_{diff})$. A sinusoid waveform with frequency $f_0$ is used as the input signal. A Discrete

Fourier Transform (DFT) is applied to the output waveform of the static calibrated DAC to get its frequency domain sequence followed by the removal of the fundamental component pairs $f_0$ to the error signal in frequency domain. An inverse Discrete Fourier Transform (IDFT) is done to the error signal to generate the time domain error signal. The magnitude of the pulse height of $E_{dyn}(x_n, x_{diff})$ is obtained by time averaging of the error values in the region of $\Delta t$ for each transition. The dynamic settling error $E_{set}(x_n, x_{diff})$ can be obtained in a similar fashion where the averaging of the error values is carried out over the whole clock period for each transition. Several input signal frequencies are chosen in the entire range of Nyquist frequency to get error look-up-tables of full scale $X_n$ and $X_{diff}$.

## III. SIMULATION RESULTS AND DISCUSSION

A 15-bit DAC is used to verify the validity of this approach, Fig 3. The raw DAC is segmented into a 7-bit thermometer MSB DAC and a 8-bit binary LSB DAC. An ideal ADC is used to generate the input code. Since most of the nonlinearity errors come from the MSB part, so only the 3 bit upper MSB (UMSB) current sources array are implemented with transistors level to reflect the nonlinearities in the circuit while the 4 bit low MSB (LMSB) and the 8-bit LSB DAC is AHDL behavior model.

The calibration is done for several cases: only dynamic settling error calibration, only dynamic glitch error calibration and both dynamic settling and glitch errors calibration.

In order to compensate the dynamic errors, it is better to calibrate as many bits as possible. But the complexity of the look-up-table will increase dramatically with the increase in the number of calibrated bits. However, the improvement of SFDR may be not obvious if the calibration bits number is too small resulting from insufficient information in the look-up table. So a tradeoff exists between the calibration bits and the complexity. In this paper, the 7-bit MSB (3-bit thermometer transistor level for upper MSB and 4-bit binary behavior model for lower MSB) is used for calibration. Current sources with cascoded structure are used in 3bit UMSB to increase the output impedance in order to reduce the current source drain voltage variation. The clock frequency $f_{clk}$ is 200MHz. The dynamic glitch compensation pulse width is 0.4ns.

The effect of calibration is shown in Fig. 4. From the plot, it can be seen that the SFDR values before and after calibration are close at low frequency. Whereas, a significant increase in the SFDR performance, at least 20dB, can be noticed at higher frequencies when dynamic glitch calibration is taken into account. Not much SFDR improvement is achieved by having both dynamic glitch calibration and dynamic settling calibration as compared to only the dynamic glitch calibration as well as the results show that the SFDR improvement is mainly from the dynamic glitch calibration.

### A. *Robustness of the calibration approach*

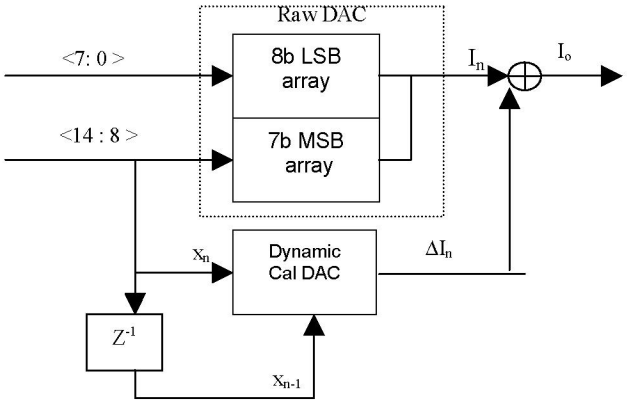


Fig. 3 DAC test structure illustration

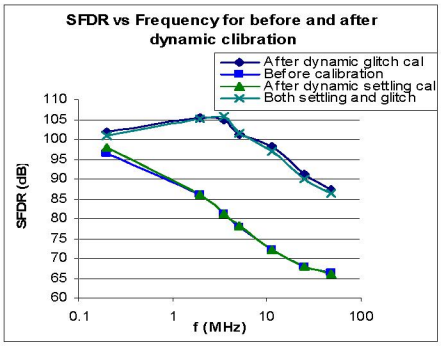


Fig. 4 SFDR vs Input signal frequency between before and after dynamic calibration.

In order to measure the robustness of this approach, the time interval, $\Delta t$, and the delay, $\Delta t_d$, of the pulse used for glitch compensation are varied.

*1) SFDR vs Compensation pulse width*

The nominal value of the compensation current pulse width is assumed to be 0.4ns, the input signal frequency $f_o$ is about 2MHz. The simulation results are shown in Fig. 5. When the width changes ±0.1ns(±25%), the SFDR value changing is about -4dB(-4%). It is within the tolerate range. As it is not difficult to adjust the normalized width within 5%, this results indicates that the compensation pulse width variation has little effect on the SFDR improvement.

*2) SFDR vs Compensation pulse delay*

In calibration technique, it is assumed that the compensation pulse is aligned with the raw DAC output. But it may be not the case in reality. A time difference between the raw DAC output and the calibration pulse, $\Delta t_d$, may exist. This delay will have impact on the SFDR. The effect of different $\Delta t_d$ to SFDR is shown in Fig. 6. In the simulation, the compensation pulse width is 400ps, the input signal frequency is about 11.3MHz. The magnitude of SFDR decreases from about 98dB to about 87dB when the $\Delta t_d$ changes from 0 to 400ps. If the delay can be control under 200ps, the degradation of the SFDR is less than about 6%.

The requirement of this control is not hard, so it is not a big concern in the design.

Both results of 1) and 2) show that this approach is robust.

### *B. SFDR vs shape of compensation pulse*

In the calibration process, not only the robustness of the approach but also implementation possibility is needed to be considered. In the previous calibration, the pulses used in calibration are rectangle in shape. In reality, it is a big challenge to get rectangle waveform with width of half nano second. However, it is much easy to generate a triangle or near triangle waveform. If the SFDR improvement using triangle waveform for compensation can achieve the same or just a little bit below as that with rectangle, it will relax the realization of the calibration. Two kinds of triangle waveforms (a) and (b) as shown in Fig. 7 are used to replace the rectangular waveform, where the height is normalized to the height of the rectangle waveform. The SFDR improvement for different compensation pulse shapes is shown in Fig.8. The results show that the shapes of the triangle have little effect on the SFDR improvement for the same compensation pulse energy as that of the rectangular pulse.

Only one current pulse is employed for each MSB transition during the calibration. So the error waveform caused by dynamic nonlinearity can't be completely compensated. If a current array is applied for each MSB transition, it will compensate nonlinearities more precisely, therefore, achieve a better dynamic performance.

## IV. CONCLUSION

A new approach for dynamic nonlinearity calibration of DAC was presented. The input code dependence can be significantly attenuated and a over 20dB SFDR improvement in higher frequency is achieved by generating an appropriate amount of current pulse and adding it to the raw DAC output current at each states transition.

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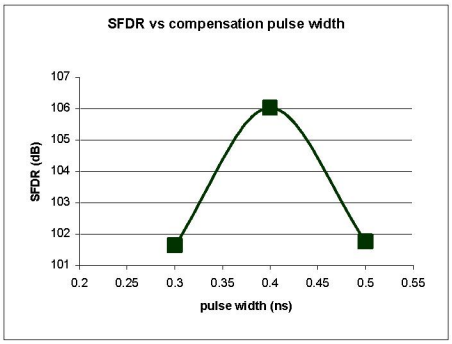


Fig. 5 SFDR vs Compensation pulse width

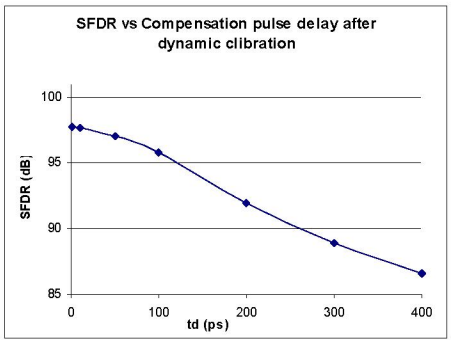


Fig. 6 SFDR vs Compensation pulse delay

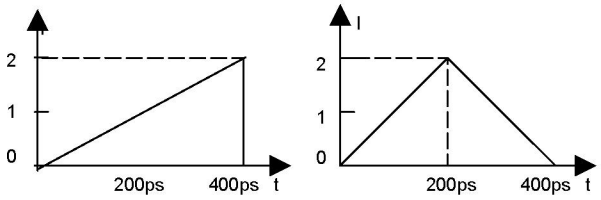


Fig. 7 Two calibration triangle waveforms

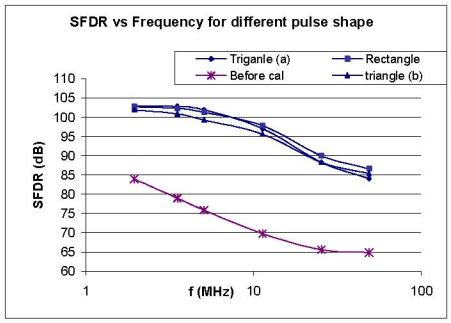


Fig. 8 SFDR vs Input signal frequency for different compensation pulse shapes