Linearity Test for High Resolution DACs Using Low-Accuracy DDEM Flash ADCs

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***Abstract*— This work proposed a built-in self-test (BIST) strategy for DAC linearity test by utilizing the deterministic dynamic element matching (DDEM) technique in a common flash ADC. DDEM technique allows low-resolution and low-accuracy ADCs work as test devices. In order to provide high resolution/accuracy test abilities, a fine quantization stage and an input dithering DAC are incorporated. In this paper, the architecture of the test system and the test procedure are described. The test performance is analyzed theoretically and verified by numerical simulation. Simulation results show that a two-step flash ADC composed of a 6-bit coarse DDEM stage and a 6-bit fine stage, plus an incorporated 5-bit dithering DAC, with linearity of all the blocks no more than 6 bits, is capable of testing 14-bit DACs.**

I. INTRODUCTION

With the continuous development in VLSI techniques, more and more applications are pushing the speed and accuracy requirement of data converters: most applications in communications need DACs with more than 10-bit resolution and at least 100MSPS update rate; for digital audio and some industrial applications, the resolution requirements of DACs are even higher. As s result, testing these data converters has become one of the most challenging problems in the area of analog and mixed–signal (AMS) test [1], because source signals and test equipments used in test usually need higher precision than devices under test, which makes designing test devices an even more difficult task.

To reduce design complexity, techniques that can provide accurate testing results by using inaccurate analog components have been investigated. A new built-in self-test (BIST) technique using an ADC with deterministic dynamic element matching (DDEM) to test DACs' linearity was proposed on ISCAS 2005 [2]. In [2], a two-step DDEM flash ADC with an 8-bit DDEM coarse stage and a 6-bit fine stage was simulated and proved to be capable of testing 14-bit DACs. Flash structure was utilized because of its large bandwidth and good compatibility with DDEM technique. However, the area, power consumption and input capacitance introduced by the comparators of a flash ADC increase exponentially with the resolution. Therefore, the implementation of the 8-bit coarse flash stage is nontrivial, and the large power and area consumption make this BIST method less practical. In this work, the resolution of the coarse stage is reduced to 6 bits, which is a great reduction in design complexity, while the same testing performance is maintained by adding a low-resolution, easy-to-implement dithering DAC at the input of the ADC. Thanks to the simpler implementation, the proposed technique is much more suitable for BIST applications. The rest of the paper is organized as follows. Section II briefly discusses DACs' nonlinear error and the statistical test of data converters. Section III describes the proposed test structure and algorithm as well as the theoretical analysis on test performance. Section VI talks about simulation results and Section V concludes the paper.

II. DACS' LINEARITY TEST

A DAC's linearity performance can be characterized by its differential nonlinearity (*DNL*) and integral nonlinearity (*INL*) [3]. For each input code k, *DNL(k)* and *INL(k)* are defined as

$$DNL(k) = \frac{V_{k+1} - V_k}{LSB} - 1, \quad (1)$$

$$INL(k) = \frac{V_k - V_0}{LSB} - k, \quad (2)$$

where V_k is the analog output of the DAC for input code k, and the least significant bit *LSB* is the ideal voltage increment defined by the end point fit line, which can be expressed as

$$LSB = \frac{V_{2^n-1} - V_0}{2^n - 1}, \quad (3)$$

As shown in (2) and (3), the *DNL* and *INL* of a DAC can be characterized by estimations of V_k-V_0.

Conventionally DAC testing requires a high-resolution high-accuracy ADC as a test device. Assume the ADC's

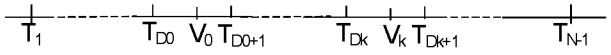

Figure 1. Relative position of input voltage V_k with respect to ADC transition points

digital output codes for inputs V_0 and V_k are D_0 and D_k, respectively, as shown in Fig. 1 where T_k indicates the k^{th} transition point of the ADC. Thus, the estimation of V_k-V_0, D_k-D_0, also indicates the number of ADC transition points between V_0 and V_k.This is similar to that in histogram test of an ADC the number of the ADC's inputs that result in a particular output code is used as an estimation of the width of the code bin. In order to reduce DAC testing errors, the test ADC needs higher resolution than that of the DAC under test and uniformly distributed transition points. Due to component mismatches, this requirement is very challenging especially when the DAC under test has a high resolution. An alternative approach is to use a bunch of low resolution/accuracy ADCs and make the overall transition points conform to the requirement: with high resolution and uniformly distributed. Then the total number of the transition points between two input voltages can still be used to estimate the voltage difference. As has been explained in [2], DDEM can provide ADCs with desired transition points.

III. PROPOSED BIST TECHNIQUE

The description of the proposed BIST method for DAC nonlinearity testing in this section are divided into three parts. The first subsection illustrates the implementation of DDEM in flash ADC and the DDEM algorithm. The second part explains the whole BIST system design. Theoretical analysis is given in the third part.

A. DDEM Implementation in Flash ADC

The structure of the flash ADC with DDEM was discussed in [2]. Different from typical flash ADCs, all the resistors are connected as a loop through switches, as shown in Fig. 2. By opening one switch in the loop and connecting the two broken ends to reference voltages, a resistor string is formed to generate transition voltages, which are sent out for comparison. P switching patterns are applied to the resistor loop to construct different R-strings. P, denoted as iteration parameter, is also the number of digital outputs associated to one analog input. Due to resistance variations, P different sets of ADC transition points can have a nearly uniform overall distribution.

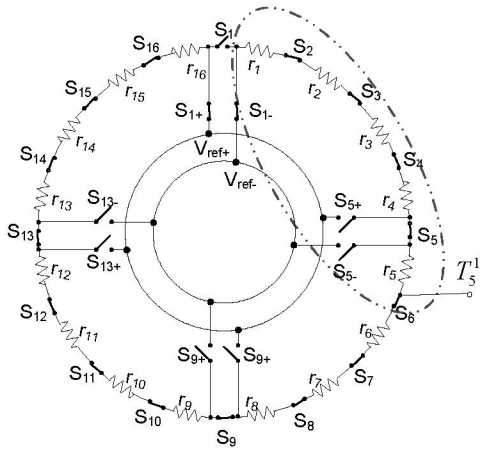

Figure 2. Resistor loop of a 4-bit DDEM flash ADC with P = 4

Assume there are N resistors in the loop. P is selected to be one of the submultiples of N, i.e. $q=N/P$ is an integer. The proposed DDEM technique chooses P different R-strings by each time opening one of P switches which are uniformly distributed in the loop. By doint this, all the resistors in the loop can be almost equally used. Fig. 2 shows the resistor loop of a 4-bit ADC as a simple example to explain how to apply DDEM to obtain different R-strings. There are totally 16 resistors and comparators in the ADC. Assume $P=4$ and $q=N/P=4$, then we can generate four different R-strings by opening one of the switches S_1, S_5, S_9 and S_{13}. For each output code of the DDEM flash ADC, we have four transition points from different switching patterns. For example, by opening S_1 (or S_5, S_9, S_{13}) and closing S_{1+} and S_{1-} (or S_{5+} and S_{5-}, S_{9+} and S_{9-}, S_{13+} and S_{13-}) the transition points corresponding to output code $D=5$ are:

$$T_5^1 = \frac{(V_{ref+} - V_{ref-})}{R_{total}}(r_1 + r_2 + r_3 + r_4 + r_5), \quad (4)$$

$$T_5^2 = \frac{(V_{ref+} - V_{ref-})}{R_{total}}(r_5 + r_6 + r_7 + r_8 + r_9), \quad (5)$$

$$T_5^3 = \frac{(V_{ref+} - V_{ref-})}{R_{total}}(r_9 + r_{10} + r_{11} + r_{12} + r_{13}), \quad (6)$$

$$T_5^4 = \frac{(V_{ref+} - V_{ref-})}{R_{total}}(r_{13} + r_{14} + r_{15} + r_{16} + r_1), \quad (7)$$

where V_{ref+} and V_{ref-} are reference voltages and R_{total} is the total resistance of the R-string, which is assumed to be a constant for all the four R-strings.

B. BIST Structure for DAC Testing

The general structure of the two-step DDEM flash ADC has been described in [2], as shown in Fig. 3. Different from the structure in [2], the sample and hold stage is removed. When test is operating, the inputs of the ADC are step outputs of DACs under test, which compensate for the time delay in the coarse stage automatically. Therefore, the design complexity is significantly reduced. The full-scale input range of the fine stage is equivalent to *2LSB* of the coarse stage for over-range protection. The offset voltage shifts inputs of the fine stage to the middle of its input range to compensate for the effect of comparator offsets.

Concerning the amount of power consumption, area, and input capacitance introduced by the comparators, the resolution of the coarse stage is reduced to from 8 bits in [2]

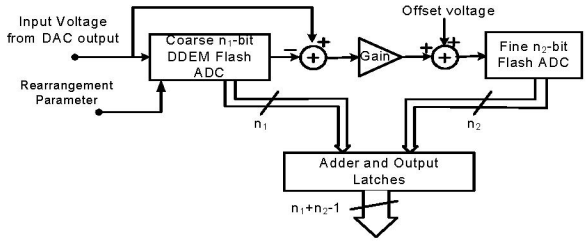

Figure 3. Block diagram of the two-step DDEM flash ADC

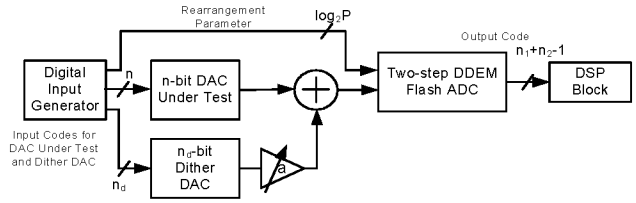

Figure 4. Block diagram of the proposed BIST scheme

to 6 bits. To make the scheme still suitable for high-resolution test, an input dithering DAC is incorporated with the DDEM ADC. Fig. 4 illustrates the structure of the proposed BIST system. The output of the dithering DAC is added to the output of the DAC under test, and the sum is taken as the input to the DDEM ADC. The full-scale output range of the dithering DAC is adjustable and small comparing to the ADC input range, e.g. several LSBs of the coarse stage. This ensures the shifted DAC output signal is still covered by the effective part of DDEM ADC input range.

C. *Theoritical Analysis and Optimization*

Assume V_i is the input analog voltage, which represents the summation of the DAC output and the dithering voltage. Firstly, let us evaluate the estimation of the voltage V_i by using the two-step DDEM ADC. To get the measurement m_i of V_i, we average all the P digital outputs $d_{i,1}$, $d_{i,2}$... $d_{i,P}$ as

$$m_i = \frac{1}{P}\sum_{j=1}^{P} d_{i,j} . \tag{8}$$

If $T_{c,1}^{id}, T_{c,2}^{id}, \quad , T_{c,N-1}^{id}$ are the ideal voltage transition points of the coarse stage, where $N = 2^{n_1}$ is the resolution of the coarse stage, the input analog signal can be accurately expressed as

$$V_i = T_{c,k}^{id} + r_i , \tag{9}$$

Where $T_{c,k}^{id}$ is the nearest ideal transition point smaller than V_i, r_i is the residual voltage by subtracting $T_{c,k}^{id}$ from V_i. The position of the input signal V_i is illustrated in Fig. 5.

Assume for the input V_i the digital outputs of the coarse DDEM ADC are $d_c^1, d_c^2, \quad , d_c^P$, and $r_c^1, r_c^2, \quad , r_c^P$ are the residual voltages which will be estimated by the fine stage with a reasonable accuracy. Then the input analog V_i can also be represented as

$$V_i = T_{c,d_c^j}^{j} + r_c^j, j = 1,2, \quad , P , \tag{10}$$

where $T_{c,d_c^j}^{j}$ is the transition level corresponding to the j^{th} output code d_c^j . In estimation, the coarse output code d_c^j represents the voltage value of the ideal transition point $T_{c,d_c^j}^{id}$, and the fine output code d_f^j is the summation of the residual

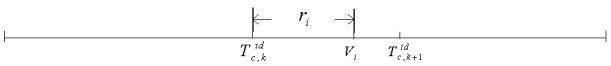

Figure 5. Input voltage relative to ideal transition points

voltage r_c^j and quantization noise of the fine stage. So for j^{th} switching pattern, the measurement of the input V_i, m_i^j is

$$m_i^j = d_c^j + d_f^j = T_{c,d_c^j}^{id} + r_c^j + \varepsilon_Q^j, j = 1,2, \quad , P , \tag{11}$$

where ε_Q^j is the quantization error of the fine stage. The measurement of V_i is taken as the average of the P output codes of the two-step ADC as

$$\begin{aligned} m_i &= \frac{1}{P}\sum_{j=1}^{P} m_i^j = \frac{1}{P}\sum_{j=1}^{P}(T_{c,d_c^j}^{id} + r_c^j + \varepsilon_Q^j) \\ &= T_{c,k}^{id} + \frac{1}{P}\sum_{j=1}^{P}(T_{c,d_c^j}^{id} - T_{c,k}^{id} + r_c^j + \varepsilon_Q^j) \end{aligned} . \tag{12}$$

Using the equality of (9) and (10), (12) is rewritten and the estimation error can be expressed as

$$e_i = m_i - V_i = -\frac{1}{P}\sum_{j=1}^{P} INL^j(d_c^j) + \frac{1}{P}\sum_{j=1}^{P}\varepsilon_Q^j , \tag{13}$$

where $INL^j(d_c^j)$ is the integral nonlinearity error of the j^{th} switching pattern of the coarse flash ADC at transition point $T_{c,d_c^j}^{j}$. The definitions of the differential and integral nonlinearity errors provide the following relationships:

$$INL(k) = \sum_{i=1}^{k} DNL(i) , \tag{14}$$

$$\sum_{i=1}^{N} DNL(i) = 0 , \tag{15}$$

where N is the number of resistors. Then, (13) can be rewritten as

$$e_i = m_i - V_i = -\frac{1}{P}\sum_{j=1}^{P}\sum_{t=1}^{d_c^j} DNL^j(t) + \frac{1}{P}\sum_{j=1}^{P}\varepsilon_Q^j . \tag{16}$$

With proposed DDEM switching method, *DNL(k)*s of the coarse stage satisfy

$$\sum_{j=1}^{P}\sum_{t=1}^{s^*q} DNL^j(t) = s \times \sum_{i=1}^{N} DNL^1(i) = 0 . \tag{17}$$

The expression of the estimation error can be reduced to

$$e_i = m_i - V_i = -\frac{1}{P}\sum_{j=1}^{P}\sum_{t=1}^{d_c^j - s^*q} DNL^j(t) + \frac{1}{P}\sum_{j=1}^{P}\varepsilon_Q^j . \tag{18}$$

Therefore, the first term in (18) is reduced to the summation of a set of non-repeating *DNL(k)*s, the maximum value of which should be comparable to the *INL* of the original coarse stage, INL_C. It is noted that this term is approximately periodic with a period of q *LSB* of the coarse stage. In addition, the estimation error indicates the *INL(k)* of the overall transition points. Assume the quantization error is small. The *INL(k)* of the overall transition points also has the same period as the first term. With the input dithering DAC, whose full-scale input is equal to this period, the estimation error can be further reduced. The procedure that we measure the dither shifted inputs in a period of the overall *INL(k)* is similar to that we shift *INL(k)* of the coarse stage in DDEM to cancel the estimation error, and the maximum estimation error is still comparable to INL_C. Thus, the estimation error with the dithering DAC can be expressed as

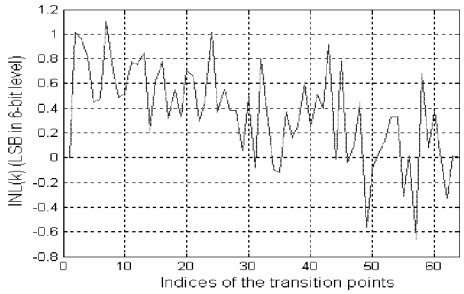

Figure 6. Linearity of the original coarse stage flash ADC

$$e_{tot} \approx \frac{1}{2^{ENOB_d}} \frac{1}{P} INL_C + \frac{1}{2^{n_d}} \frac{1}{P} \sum_{i=1}^{2^{ENOB_d}} \sum_{j=1}^{P} \varepsilon_{Q,i}^{j}, \quad (19)$$

where $ENOB_d$ is the effective number of bits of the dithering DAC.

With the quantization error term much less than the first term, the test performance of the whole system can be calculated as

$$n_{test} \approx ENOB_C + \log_2 P + ENOB_d, \quad (20)$$

where $ENOB_C = n_1 - \log_2 INL_C - 1$ is the effective number of bits of the coarse stage. To optimize the parameters, at first the resolution of the fine stage should be chosen so that the quantization error is small comparing to the desired test performance. Then the resolution of the coarse stage, the value of P and the resolution of the dithering DAC are selected according to (20).

IV. Simulation Results

To verify the proposed structure and the previous analysis, simulations in MATLAB are carried out. In simulation, a 14-bit DAC is modeled as the device under test. The test system has a 6-bit coarse stage, a 6-bit fine stage and a 5-bit dithering DAC. The linearity of the coarse stage is less than 5 bits, as shown in Fig. 6. The fine stage and the dithering DAC are nearly 5-bit linear. The standard deviations of comparator offsets in two stages are more than *0.3LSB* of the coarse and fine flash stages respectively.

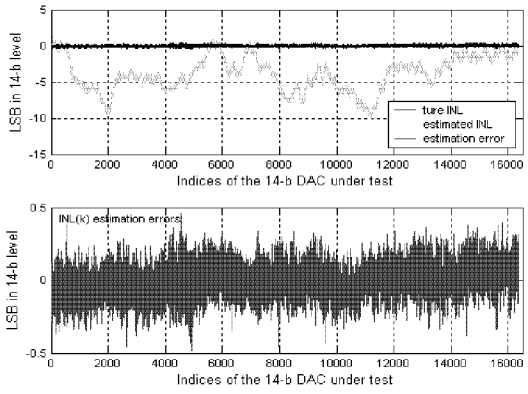

Figure 7. INL(k) estimation error with P=16 and 5-bit dithering DAC, 14 bits DAC under test

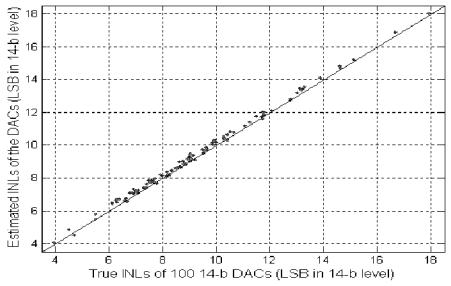

Figure 8. Estimated INLs vs true INLs of 100 14-bit DACs tested by 100 DDEM ADC transition points

With $P=32$, the quantization error is calculated to be less than 16-bit level. The test performance of the specified system can be roughly equivalent to $n_{test}=5+5+5=15$ *bits*. Therefore, it should be capable of testing a 14-bit DAC. Fig. 7 shows that with the above configuration the maximum *INL(k)* estimation error is about *0.5LSB* in 14-bit level and the *INL* error is *0.1361LSB*.

In order to validate the robustness of the algorithm, different DDEM ADCs are implemented. In this simulation, we use 100 different DDEM ADCs, which have the same configuration and accuracy as that in the former simulation, to test 100 different 14-bit DACs. Fig. 8 shows the relationship between the estimated *INL* values of different DACs and the true values, where the estimation errors are in the range from *-0.2425LSB* to *0.3893LSB* and the *INLs* of the DACs are in the range from *4LSB* to *18LSB*. The results show that with *P* equal to 32 and a 5-bit dithering DAC, the proposed two-step DDEM ADC is capable of testing 14-bit DACs.

V. Conclusions

This work focuses on a new BIST scheme for high-resolution DAC testing by using a two-step DDEM flash ADC with an input dithering DAC incorporated. The structure and operation of the testing circuitry is described in details. The DDEM technique can be implemented with simple digital control circuits. The algorithm and the performance analysis have been validated by numerical simulations. Simulation results show using this approach, the static linearity test of 14-bit DACs can be done with only 5-bit linear ADCs. This test approach has potential for BIST of precision DACs because of the low requirement on ADC performance and the simple dynamic element matching strategy.

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