Robust High-Gain Amplifier Design Using Dynamical Systems and Bifurcation Theory With Digital Postprocessing Techniques

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***Abstract*—A CMOS differential positive feedback amplifier (PFA) and its inherent nonlinearity were analyzed. Based on nonlinear dynamical systems and bifurcation theory, we predicted bifurcation and hysteresis phenomena in the PFA. An algorithm, which can be implemented using simple digital logic, was developed to measure the PFA's open-loop stability as the bifurcation parameter changes. Parameter-tuning algorithms were constructed that systematically move the amplifier's operational point towards the bifurcation point, at which an infinite dc gain is achieved. In order to compensate for the PFA's high sensitivity to process and temperature variations, flexible analog design integrating digital programmability and adaptive digital postprocessing techniques were developed. This flexibility and postprocessing capability could dramatically enhance the PFA's yield. Full corner simulation results over wide temperature range verified the bifurcation phenomena and the effectiveness of the control algorithms. It is shown that this amplifier can maintain high performance in advanced digital CMOS technology at very low voltage supply. It is also demonstrated that the proposed approach offers a robust PFA design with both high yield and high performance.**

***Index Terms*—Amplifier, bifurcation, high gain.**

I. Introduction

SYSTEM-ON-A-CHIP (SOC) is identified as one of the next-generation drivers for the semiconductor industry [1]. Integrating analog functions in SOCs is the trend and low cost is a key to success. In particular, high-performance mixed-signal SOCs in inexpensive standard digital CMOS processes will be in high demand. However, it is also identified that mixed-signal design is a difficult challenge, and analog circuit design is a bottleneck in the process towards SOC.

The operational amplifier, or op amp, is by far the most common and important category among analog circuits. Because of the success of MOS technologies, the MOS op amp design has become one of the most important analog circuit designs. Realization of high-performance MOS amplifiers in standard digital CMOS is a key to implementing low-cost mixed-signal SOCs. Among these amplifiers, high-gain high-speed amplifiers is one especially important category.

Cascoding with gain-boosting and multistage cascading have been proven to be effective in achieving high gain with moderate-to-high voltage supplies. On the other hand, positive-feedback technique has been shown to be more promising in achieving high dc gain with good frequency response in low-voltage applications [9]–[13]. Positive feedback has been successfully used in the preamplifier of modern comparators to achieve high-speed operation. The instability and transfer hysteresis caused by the use of positive feedback are subject to significant variations due to random process variability. These variations limit the guaranteeable effective gain of the preamplifier to be low, which is not a big concern in comparator design. However, the use of positive feedback in stand-alone high-gain amplifier design has been scarce since no practical solutions have been found to overcome the challenge of achieving sufficient yield in the presence of mismatches as well as the temperature variations. In fact, previous studies concluded that achieving a fixed positive feedback amplifier design under all variations would gain little improvement while adding too much cost. Yan *et al.* [12] introduced a continuous-time adjusting scheme to calibrate the positive feedback amplifier. He *et al.* [13] investigated a discrete adjusting scheme to digitally calibrate the positive feedback amplifier. Both [12] and [13] used phase-inversion-detection techniques and enhanced the amplifier's gain and yield. However, they require high-gain low-offset comparators which are difficult to realize and required heavy human interference, making calibration time-consuming and amplifiers expensive. Low yield as well as high cost are the major limitations for the positive feedback amplifiers.

Another concern is that positive-feedback amplifiers typically show strong nonlinearity [12], [13]. Efforts have been made to decrease the gain dependence on output swing, but few achieved a practical solution. Traditional circuit designers typically use linear models [14] to study analog circuits or even call those circuits "linear circuits," but nonlinearity in circuits becomes more apparent with feature size shrinking. Although linear models are still valid in certain applications, knowing the nonlinearity at the circuit/device level can help us identify circuit nonideality, avoid the disadvantages of nonlinearity, and even make use of the advantages of nonlinearity.

This study resolves the main limitation of yield in the positive feedback amplifier (PFA) by introducing adaptive-feedback control based on the discovery of bifurcation. This study also

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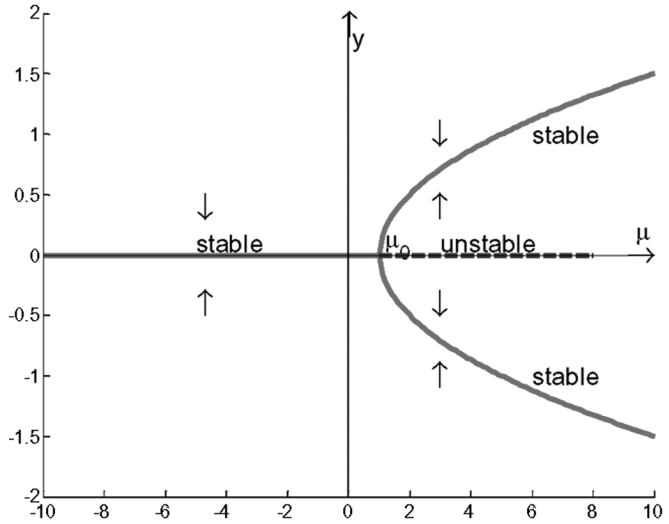

Fig. 1. Supercritical pitchfork bifurcation.

enhances understanding of circuit performance with the help of the nonlinear dynamical systems theory. This paper first introduces bifurcation phenomenon in nonlinear dynamic systems [15]. Section III provides theoretical analysis of dynamic behavior of a PFA [13]. This analysis also explains the nonlinearity in the PFA. Parameter dependency of bifurcation [15] is used to study the positive feedback-to-gate amplifier, and bi-state detection with pull-up and pull-down is developed to maintain a high dc gain. Section IV discusses two digital postprocessing techniques: bifurcation detection and branching parameter-tuning algorithms. Both algorithms were verified valid using MATLAB as well as Cadence mixed-signal simulation tools. These algorithms do not require high-gain low-offset comparators, which overcome the shortcoming of [12] and [13]. Section V presents system- and circuit-level simulation results using industrial BSIM3v3 models, and Section VI concludes this paper.

II. Dynamical System and Bifurcation

Bifurcation [15] is one commonly encountered nonlinear phenomenon in dynamical systems. In order to explain bifurcation clearly, a differential equation is introduced

$$\dot{y} = (\mu - \mu_0)y - y^3 \tag{1}$$

where μ_0 is a constant. For $\mu > \mu_0$, there are two stable equilibrium points at $y = \pm\sqrt{\mu - \mu_0}$ and one unstable equilibrium at $y_0 = 0$. For $\mu \leq \mu_0$, there is only one stable equilibrium at $y_0 = 0$. We call point $(y_0 = 0, \mu_0)$ a bifurcation point and μ the branching parameter. Fig. 1 shows the branch diagram of this supercritical pitchfork bifurcation.

Bifurcation points can be identified by certain algebraic properties. Let

$$f(y, \mu) = (\mu - \mu_0)y - y^3. \tag{2}$$

We can get the derivatives of $f(y, \mu)$ with respect to y and μ as

$$f_y(y, \mu) = (\mu - \mu_0) - 3y^2$$

$$A = \frac{g_{mn}}{g_{op} + g_{on} - \mu g_{mp}}.$$

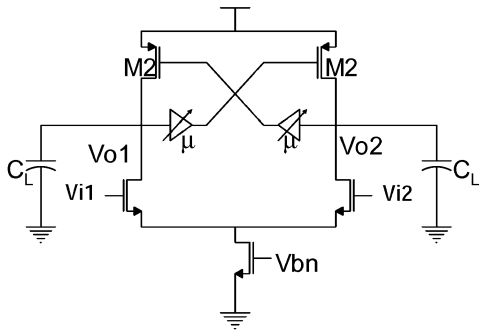

Fig. 2. PFA.

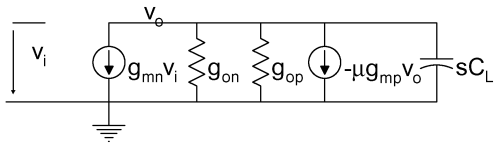

Fig. 3. Small-signal equivalence.

and

$$f_u(y, \mu) = y. \tag{3}$$

If the matrix $[f_y(y_0, \mu_0) f_u(y_0, \mu_0)]$ is singular, the point (y_0, μ_0) is a bifurcation point. In supercritical pitchfork, $[f_y(y_0, \mu_0) f_u(y_0, \mu_0)] = [0\,0]$. This suggests that the branching point (y_0, μ_0) is a bifurcation point. It can be shown that y will converge to $y_0 = 0$ with time going to positive infinity when $\mu \leq \mu_0$ no matter how the initial condition is. If $\mu > \mu_0$, y will converge to $y = \sqrt{\mu - \mu_0}$ when $y|_{t=0} > 0$ or converge to $y = -\sqrt{\mu - \mu_0}$ when $y|_{t=0} < 0$, labeled in Fig. 1. Thus, it is possible to detect and push the branching parameter μ to μ_0. In the following sections, we will demonstrate the application of bifurcation in the realization of a high-performance analog function.

III. PFA

Fig. 2 depicts a PFA [13], where the gates of pMOS transistors (current source load) are connected to its output through a feedback buffer with attenuation of μ. Using small-signal equivalence [14] shown in Fig. 3, we can show that the amplifier has an attenuation-dependent dc gain as

$$A = \frac{g_{mn}}{g_{\rm op} + g_{\rm on} - \mu g_{mp}}. \tag{4}$$

Let

$$\mu_0 = \frac{g_{\rm op} + g_{\rm on}}{g_{mp}}. \tag{5}$$

We can see that the amplifier will have an infinite dc gain when $\mu = \mu_0$.

However, we need more information to search for and maintain the optimal attenuation over process and temperature variations, where the nonlinear dynamical theory is found to be helpful [16].

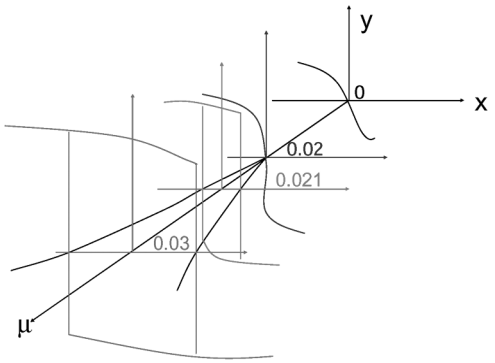

Fig. 4. DC transfer curve of the PFA.

A. Amplifier's Dynamics

Level–1 Schichman–Hodges model [17] is used to derive the system dynamic. This model includes the channel-length modulation effect that $I = \beta V_{\rm EB}^2(1+\lambda|V_{\rm DS}|)$. We denote $V_{\rm EBN} = V_{\rm GSN} - V_{\rm THN}$, $V_{\rm EBP} = V_{\rm SGP} + V_{\rm THP}$, $V_{i1} = V_{\rm ICM} + v_{i1}$, $V_{i2} = V_{\rm ICM} + v_{i2}$, $V_{o1} = V_{\rm OCM} + v_{o1}$, and $V_{o2} = V_{\rm OCM} + v_{o2}$. Using these denotations, the dynamics of this amplifier can be described by

$$\begin{aligned} C_L\frac{dv_{o1}}{dt} &= \beta_p(V_{\rm EBP}-\mu v_{o2})^2\left[1+\lambda_p(V_{\rm DD}-V_{\rm OCM}-v_{o1})\right] \\ &\quad -\beta_n(V_{\rm EBN}+v_{i1})^2\times\left[1+\lambda_n(V_{\rm OCM}+v_{o1}-V_S)\right] \\ C_L\frac{dv_{o2}}{dt} &= \beta_p(V_{\rm EBP}-\mu v_{o1})^2\left[1+\lambda_p(V_{\rm DD}-V_{\rm OCM}-v_{o2})\right] \\ &\quad -\beta_n(V_{\rm EBN}+v_{i1})^2\times\left[1+\lambda_n(V_{\rm OCM}+v_{o2}-V_S)\right]. \end{aligned} \tag{6}$$

For simplicity, we will use $v_{i1} = -v_{i2} = v_i/2$ and $v_o = v_{o1} - v_{o2}$ in our later discussion. If the circuit has very good common-mode rejection ratio (CMRR), we have $v_{o1} = -v_{o2} = v_o/2$. By letting $y = v_o$, $x = v_i$, (6) can be rewritten as

$$\begin{aligned} \dot{y} = &-\frac{g_{\rm op}+g_{\rm on}-\mu g_{mp}}{C_L}y - \frac{\mu^2\beta_p\lambda_p}{4C_L}y^3 \\ &-\frac{\beta_n\lambda_n\left[1+\lambda_n(V_{\rm OCM}-V_S)\right]x^2}{4C_L}y - \frac{g_{mn}}{C_L}x. \end{aligned} \tag{7}$$

B. DC Transfer Characteristics

In (7), solving $\dot{y} = 0$ gives us the amplifier's dc transfer characteristics

$$\mu^2y^3 + \left[a(\mu_0-\mu)+bx^2\right]y + cx = 0 \tag{8}$$

where $a = 4g_{mp}/\beta_p\lambda_p$, $b = (\beta_n\lambda_n[1+\lambda_n(V_{DCOCM} - V_S)])/\beta_p\lambda_p$, and $c = 4g_{mn}/\beta_p\lambda_p$. Fig. 4 shows the solution to (8). When $\mu \le \mu_0$, the dc transfer curve of the PFA behaves like an open-loop amplifier. However, when $\mu > \mu_0$, the circuit shows hysteresis in its dc transfer curves. It is really interesting to study this unusual property.

C. Bifurcation Without Excitation

When $x = 0$, we rewrite (8) as

$$\mu^2y^3 + a(\mu_0-\mu)y = 0. \tag{9}$$

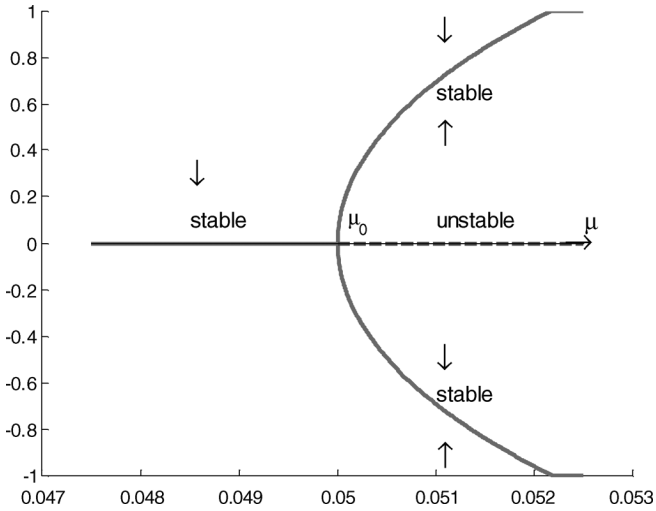

Fig. 5. Branching diagram when $x = 0$.

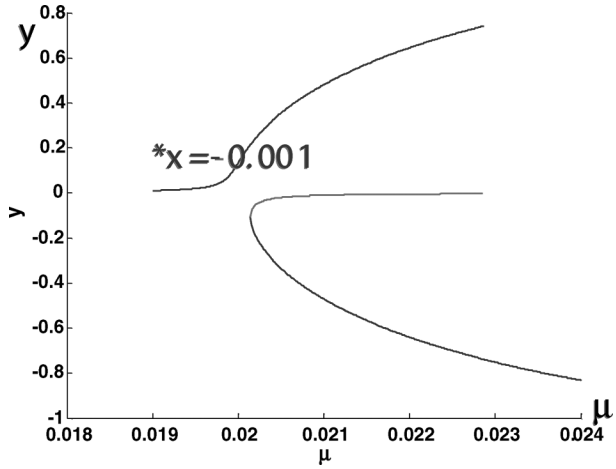

Fig. 6. Bifurcation with nonzero excitation.

It turns out that, for $\mu > \mu_0$, there are two stable equilibrium points at $y = \pm\sqrt{a(\mu-\mu_0)/\mu^2}$ and one unstable equilibrium at $y_0 = 0$, whereas for $\mu \le \mu_0$ there is only one stable equilibrium at $y_0 = 0$. Fig. 5 shows the branching diagram with a branching point at

$$(y_0, \mu_0) = (0, (g_{\rm op}+g_{\rm on})/g_{mp}). \tag{10}$$

It is easy to show that $[f_y(y_0,\mu_0), f_u(y_0,\mu_0)] = [0,\ 0]$. Thus, the branching point is a bifurcation point. Due to the limited supply in real circuits, the amplifier's outputs saturate when the branching parameter is sufficiently large, as shown in Fig. 5.

D. Bifurcation With Excitation

When $x \neq 0$ and x is small, the branching diagram in $y-\mu$ plane shows discontinuity for the two branches of stable equilibriums. Solution of (8) suggests that there exists a one–one mapping between y and x when $\mu < \mu_0 + bx^2/a$, as shown in Fig. 6.

The solution for $f(y,x,\mu) = 0$ becomes complex when $\mu \ge \mu_0 + bx^2/a$. One–one mapping from x to y turns to be invalid. When $|x| < x_0$, we can find two stable equilibria points and

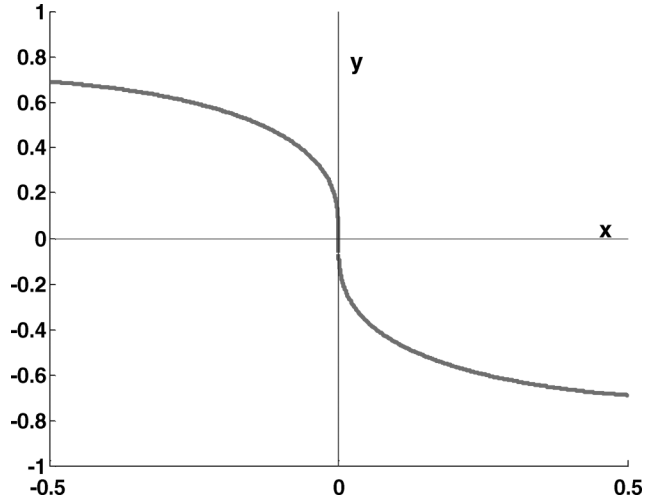

Fig. 7. Branching diagram with respect to input at bifurcation.

an unstable equilibrium. When $|x| > x_0$, there will be only one stable equilibrium point. x_0 is given by a solution to (7) and

$$\frac{g_{\rm op}+g_{\rm on}-\mu g_{mp}}{C_L}+\frac{3\mu^2\beta_p\lambda_p y^2}{4C_L}+\frac{\beta_n\lambda_n\left[1+\lambda_n(V_{\rm OCM}-V_S)\right]x^2}{4C_L}=0. \quad (11)$$

Combining (7) and (11), we obtain

$$(g_{\rm op}+g_{\rm on}-\mu g_{mp})+\frac{3\mu^2\beta_p\lambda_p}{4}\left(\frac{2x}{\mu^2\beta_p\lambda_p}\right)^{2/3}+\frac{\beta_n\lambda_n\left[1+\lambda_n(V_{\rm OCM}-V_S)\right]x^2}{4}=0. \quad (12)$$

The solution to (12) suggests that, in order to observe bifurcation, one has to limit excitation to be a small value, especially when the branching parameter is close to the bifurcation point. Figs. 4–6 all suggest that bi-state stability exists in this nonlinear system when branching parameter $\mu > \mu_o$. This bi-state stability will lead to hysteresis in the amplifier's dc transfer characteristic. This hysteresis in this supercritical pitchfork bifurcation provides a way to detect if branching parameter μ is larger than the bifurcation point.

E. DC Gain and Its Nonlinearity

Based on the definition used in circuit design area, dc gain at operating point (0, 0) (either stable or unstable) is the tangent of $f(y,x,\mu)$ at (0,0,μ) in the (y,x) plane

$$A|_{(0,0,\mu)}=\frac{f_x(0,0,\mu)}{f_y(0,0,\mu)}=-\frac{g_{mn}}{g_{\rm op}+g_{\rm on}-\mu g_{mp}}. \quad (13)$$

Let $\mu_0=(g_{\rm op}+g_{\rm on})/g_{mp}$; this suggests that at bifurcation point (0,0,μ_0), i.e., branching parameter $\mu=\mu_0$, the positive feedback amplifier will achieve an infinite dc gain. μ_0 is typically smaller than 1. Fig. 7 illustrates the dc transfer characteristic of the amplifier at the bifurcation point.

The dc transfer curve in Fig. 7 shows large nonlinearity. From (7), we can derive the small-signal gain (the tangent slope of this dc transfer curve) as

$$A|_{(y,x,\mu)}\approx-\frac{g_{mn}+\frac{\beta_n\lambda_n xy}{2}}{g_{\rm on}+g_{\rm op}-\mu g_{mp}+\frac{3\mu^2\beta_p\lambda_p y^2}{4}+\frac{\beta_n\lambda_n x^2}{4}}. \quad (14)$$

This analysis is valid for any μ value. At normal operating range, $g_m \gg \beta_n\lambda_n xy$, $g_o \gg \beta\lambda(x^2+y^2)$, and $y^2 \geq x^2$.

When there is no positive feedback, i.e., $\mu=0$,

$$A|_{(y,x,0)}=-\frac{g_{mn}+\frac{\beta_n\lambda_n xy}{2}}{g_{\rm on}+g_{\rm op}+\frac{\beta_n\lambda_n x^2}{4}}. \quad (15)$$

For a traditional amplifier, $|xy| \geq x^2$, the numerator will dominate the amplifier's gain nonlinearity. This nonlinearity will limit the performance of certain applications using open-loop amplifiers.

For an ideal PFA that $\mu=\mu_0$

$$A|_{(y,x,\mu)}\approx-\frac{g_{mn}+\frac{\beta_n\lambda_n xy}{2}}{\frac{3\mu^2\beta_p\lambda_p y^2}{4}+\frac{\beta_n\lambda_n x^2}{4}}. \quad (16)$$

Equation (16) shows that the denominator determines the gain nonlinearity of a positive feedback amplifier and suggests that the dc gain rolls off in a rate proportional to the square of the output swing. This explains the strong bell-shave open-loop nonlinearity in the PFA [12]. Equation (16) also suggests that reducing λ will significantly increase open-loop gain at nonzero outputs, given the factor that output conductance of a MOS transistor is proportional to the channel-length modulation factor λ [14]. Equation (17) gives the detailed analysis as

$$\mu=\frac{g_{\rm op}+g_{\rm on}}{g_{mp}}\propto\lambda,\qquad A\propto\frac{1}{\lambda x^2+C\lambda^3 y^2}. \quad (17)$$

The authors [18] showed a relationship between open-loop gain and closed-loop gain linearity. For a PFA with an infinite dc gain at operating point, the gain linearity of a closed-loop configuration can be written as

$$\text{THD}\geq 20\log\left(|y_m/x_m|\right) \quad (18)$$

where y_m is the desired output swing and x_m is the input value. Equation (18) implies that, given y_m fixed, decreasing λ will reduce x_m dramatically. Thus, decreasing λ enhances the gain linearity of a closed-loop configuration using the positive feedback amplifier. Increasing L is the most effective way to decrease λ. However, this will slow down the transistor's speed. Thus, one should take a tradeoff between gain and speed for different specifications.

F. Effect of Offset on Bifurcation

All of the above analyses assume perfect symmetric matching. However, semiconductor fabrication steps will introduce random variation and mismatches from device to device, from die to die, from wafer to wafer, and from lot to

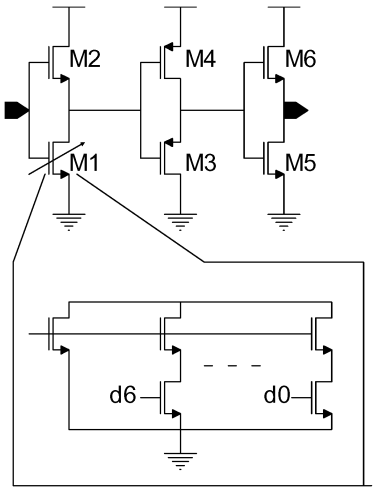

Fig. 8. Digital programmable precise CMOS attenuator.

lot, and imperfect layout will cause deterministic mismatches. For example, a noncommon-centroid pattern will be affected by gradient errors. In this study, input-referred offset is used to model the asymmetric property. Good layout can help reduce or even eliminate the deterministic offset, but it can never remove the random offset. After an amplifier has been fabricated and packaged, the offset characteristics of this amplifier are fixed.

Assuming that an amplifier has offset $V_{\rm OS}$, actual excitation seen by the amplifier is $x = x_e + V_{\rm OS}$ when an external excitation x_e is applied on the amplifier. Thus, the differential equation (7) should be modified as

$$\dot{y} = -\frac{\beta_n \lambda_n \left[1 + \lambda_n (V_{\rm OCM} - V_S)\right](x_e + V_{\rm OS})^2}{4C_L} y - \frac{g_{ot}}{C_L} y - \frac{\mu^2 \beta_p \lambda_p}{4C_L} y^3 - \frac{g_{mn}}{C_L}(x_e + V_{\rm OS}) \quad (19)$$

where $g_{ot} = g_{\rm on} + g_{\rm op} - \mu g_{mp}$. Equation (19) implies that bifurcation will still happen. The only difference is that the whole dc transfer curve will center at the offset voltage instead of the origin.

G. Possible Gain Enhancement

Earlier discussion has shown that the positive feedback amplifier will achieve an infinite dc gain at the bifurcation point. Thus, keeping the amplifier at bifurcation becomes the most important task. However, the PFA is highly sensitive to process and temperature variation. Previous studies have concluded that a fixed design of the PFA could only gain very little performance enhancement while adding too much more cost. Our analyses in earlier sections suggest that we can move the branching parameter μ to change bifurcation. A fixed design cannot provide such capability of change. Thus, we designed a variables-precise CMOS attenuator [13] to provide sufficient coverage of the branch parameter, shown in Fig. 8, and developed specific algorithms to find the bifurcation point. These control algorithms utilize digital processing techniques that could be implemented either in programmable micro-controller or hard-wired with the application-specific integrated circuit (ASIC), both in digital CMOS processes. This approach saves cost and favors more advanced deep submicrometer CMOS processes.

TABLE I
SUMMARY FOR THE AMPLIFIER'S PERFORMANCE AT BIFURCATION POINT

	Fig. 3
Tail current	I
Average DC Gain	∞
Gain-Bandwidth Product	g_{mn}/C_L
Phase Margin	90°

Instead of adjusting branching parameters continuously, digital controlled discrete branching parameter searching is used. As shown in Fig. 8, this digital programmable precise CMOS attenuator consists of three-stage linear MOS attenuators [20] that provide necessary quiescent-voltage shift and decreases sensitivity to single transistor size variation as well as having a minimal step of Δ. The first-stage linear MOS attenuator has 7-b control (control code denoted as Γ) so the total attenuation (nominal) can be expressed as

$$\mu = \mu_{\min} + \Delta\Gamma. \quad (20)$$

It then follows through straightforward analysis that the minimum attenuation step size and bifurcation-searching guarantee a minimal dc gain at operating point, which can be expressed as

$$|A_{\min}| = \frac{g_{mn}}{g_{\rm on} + g_{\rm op} - \mu_{\rm opt} g_{mp}} \geq \frac{g_{mn}}{\Delta \cdot g_{mp}}. \quad (21)$$

The PFA achieves a very high dc gain by selecting an optimal control code to eliminate the bifurcation. At this condition, we have $\mu < \mu_0$ and $0 < g_{\rm res} = g_{\rm on} + g_{\rm op} - \mu_{\rm opt} g_{mp} < \Delta \cdot g_{mp}$. Because of process variation, $g_{\rm res}$ is a random variable. Without loss of generality, we assume that $g_{\rm res}$ follows a uniform distribution between 0 and $\Delta \cdot g_{mp}$. With this assumption, we will find that the average gain enhancement using a bifurcation approach becomes ∞ [19]. Although the random variable $g_{\rm res}$ may not follow the assumption of uniform distribution, minimum gain enhancement is guaranteed on the order of $1/\Delta$, and average gain enhancement of the PFA using our proposed bifurcation method will be sufficiently large.

H. Performance Summary at Bifurcation Point

Table I lists the performance summary for the amplifier shown in Fig. 2. Without sacrificing power efficiency on gain bandwidth, our proposed amplifier achieved infinite dc gain enhancement on average, assuming that the proposed searching procedure generates uniformly distributed residual conductance.

IV. Bifurcation Detection and Branching Parameter Tuning Algorithms

The above analyses suggest that there is a possibility to design high-performance analog amplifiers using bifurcation. However, it is important to know how to properly set the branching parameter to be very close to the bifurcation point

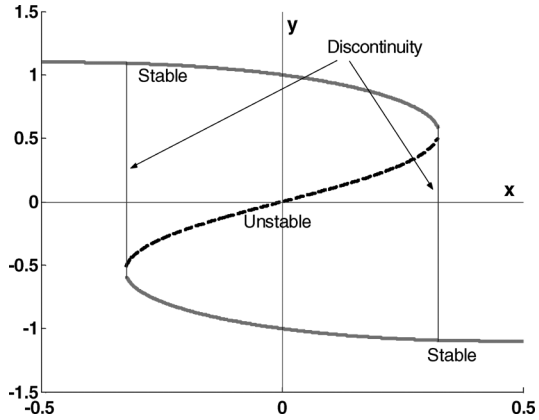

Fig. 9. DC transfer of the PFA with large μ.

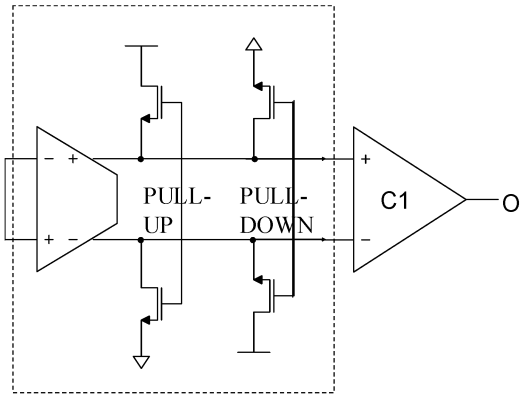

Fig. 10. Bi-state detection with pull-up/pull-down.

and, if it is not there, how to push it back. We now present an easy-to-implement algorithm to robustly detect bifurcation. Based on the bifurcation detection, another quick binary search algorithm will push the branching parameter μ back to near the bifurcation point.

A. Bi-State Detection With Pull-Up/Down and Bifurcation Detection Algorithm

Previous analysis suggests that two stable equilibria exist when $\mu > \mu_0$ and $x = 0$ or within very small input range. When the output stays at one of these two stable equilibria, small disturbance will not change the output state. Fig. 9 illustrates a typical dc transfer curve of the amplifier when the branching parameter is larger then the critical value $\mu > \mu_0$.

In this case, it can be easily seen that, if $x = 0$, y can converge to any of two stable operating points depending on the initial value of the output node. This leads to a bi-state detection idea: when the amplifier's differential input x is set to zero, if the amplifier output stays high when pulled high and stays low when pulled low, then bi-stable states exist and the branching parameter is too large. The detection circuit based on this idea is illustrated in Fig. 10. It consists of the core amplifier, an extra low gain comparator (C1), and two pairs of switches.

Depending on the bifurcation parameter, the output may finally settle to the same value or settle to two different values. If

Step 0: Make excitation to be 0 (short inputs)
Step 1: pull-up output y to be high (e.g., y=1)
Step 2: release y and wait for y to settle
Step 3: obtain comparator output O_H
Step 4: pull-down output y to be low (e.g. y=-1)
Step 5: release y, wait for y to settle
Step 6: obtain comparator output O_L
Step 7: compare O_H *and* O_L
If $O_H = O_L$ *return no*
else return yes
End

Fig. 11. Bifurcation detection algorithm.

the comparator gives the same results after the pull-up and pull-down operations, a single stable state exists and the branching parameter is below the critical value. On the contrary, if the comparator gives different answers from pull-up to pull-down operation, bifurcation is detected. As illustrated in Fig. 11, these procedures are used to develop the bifurcation detection algorithm called *Bifurcation_detect*(μ).

This algorithm works well for supercritical pitchfork bifurcations. Assuming $\mu > \mu_0$, the PFA will stay at one of these two stable equilibriums $y = \pm\sqrt{4(\mu g_{mp} - g_{\rm op} + g_{\rm on})/\mu^2\beta_p\lambda_p}$, which are insensitive to noise. As shown in Figs. 4 and 5, these two equilibria become large even when μ is a little away from μ_0. One can use a low-gain comparator to digitalize it easily (O_H, O_L). We will expect $O_H \neq O_L$ when $\mu > \mu_0$ and $O_H = O_L$ when $\mu \leq \mu_0$ confidently.

B. Branching Parameter Tuning Algorithms

Assuming $\mu_L < \mu_o$, $\mu_H > \mu_o$, one cannot observe bifurcation when $\mu \in [\mu_L, \mu_o]$ and one may observe bifurcation when $\mu \in (\mu_0, \mu_H]$. Due to this bi-state monotonic property, we can use a linear or bisection searching algorithm to drive branching parameter μ.

1) Linear Searching Algorithms: Assume that $[\mu_L, \mu_H]$ is divided into k ($k \in N$) equal distance sections $\Delta = (\mu_H - \mu_L)/k$. In a linear search algorithm, one can start at μ_L and sequentially increase μ by Δ increment. At each increment, the bifurcation detection routine will be used to detect the existence of bi-stable states. The search ends when bi-stable states are first detected. Alternatively, one can start from μ_H and sequentially decrease μ. by Δ. In this case, the search stops when bi-stable states are no longer detected. Mathematically, one can adjust μ. continuously when $k \to \infty$. After the searching is done, the amplifier will be in nonbifurcation mode while the branching parameter is within 1 LSB range of the ideal μ_o. Figs. 12 and 13 illustrate these two algorithms.

2) Bisection Searching Algorithm: According to our assumption, the branching parameter μ monotonically changes with the control code and no-bifurcation exists when $\mu \in [\mu_L, \mu_o]$ and bifurcation exists when $\mu \in (\mu_0, \mu_H]$. Thus, the critical value μ_o would be either in a larger value if no bifurcation exists or in a smaller value when there is bifurcation. Due to this bi-state monotonic property, we can use a bisection searching algorithm to push branching parameter μ. Fig. 14 illustrates this approach.

```
Start: Initial μ = μ_L
Loop A: bifurcation_detect(μ)
        If (no)
          μ := μ + Δ
          Goto A;
        else
          μ := μ − Δ
        Goto B;
B:  end
```

Fig. 12. Linear searching from μ_L algorithm.

```
Start: Initial μ = μ_H
Loop A: bifurcation_detect(μ)
        If (yes)
          μ := μ + Δ
          Goto A;
        else
          μ := μ − Δ
        Goto B;
B:  end
```

Fig. 13. Linear searching from μ_H algorithm.

```
Start: Initial μ = (μ_H + μ_L)/2
Loop A: bifurcation_detect(μ)
        if yes
          μ_H := μ ;
          μ := (μ_H + μ_L)/2
          If( μ_H − μ_L ≤ ε )
            μ := μ_L;
            goto B;
          else
            goto A;
        else
          μ_L := μ ;
          μ := (μ_H + μ_L)/2 ;
          If( μ_H − μ_L ≤ ε )
            μ := μ_L;
            goto B
          else
            goto A
B:  end
```

Fig. 14. Bisection searching algorithm.

All of these algorithms use the conceptual circuit illustrated in Fig. 15.

Because a small offset in the amplifier will saturate the output, all of these algorithms require offset compensation. One high-resolution digital-to-analog converter (DAC) is needed to cancel offset effects.

C. Improved Branching Parameter Searching Algorithm

Conceptually offset should be precompensated before trying to execute the bifurcation detection procedure. However, it is not very practical to judge offset in an open-loop high-gain amplifier. Thus, it is nearly impossible to do offset cancellation separately. Fortunately, bifurcation detection has the potential to tell both input information and bifurcation status information.

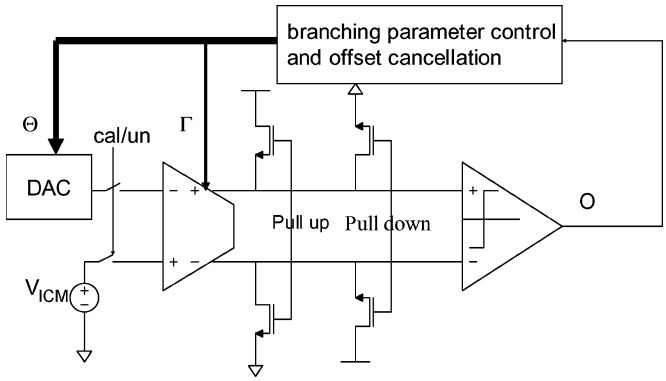

Fig. 15. Automatic branching parameter searching circuit.

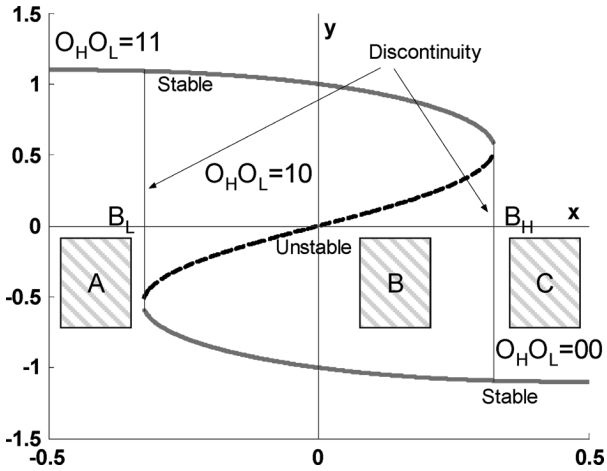

Fig. 16. Different results with pull-up/pull-down operations.

As shown in Fig. 16, the amplifier input range is divided into three regions:

A: smaller than the lower boundary of bifurcation B_L;

B: bifurcation region (B_L, B_H);

C: larger than the upper boundary of bifurcation B_H.

We can see that $B_L < B_H$ when the bifurcation parameter $\mu > \mu_0$ and $B_L = B_H$ when $\mu \leq \mu_0$. Denote $L = B_H - B_L$.

Both pull-up and pull-down operations will stay high in region A while staying low in region C. In region B, pull-up operation will stay high while pull-down operation will stay low. Offset is automatically considered by this type of operation. Thus, we can devise this pull-up and pull-down operation and use their outputs to adaptively adjust the input signal. The input signal will be increased if both are high while it is reduced when both are low. When the two outputs are different, bifurcation has been detected thus input signal has been in the bifurcation window, and this fulfills the major function of these operations.

Based on these observations, a two-loop bifurcation-point searching algorithm was proposed. The inner loop will sweep input and detect bifurcation, while the outer loop tunes bifurcation parameter μ. Both of them use binary search. Fig. 17 shows this algorithm. In our design, the attenuator is an N1-bit (7-bit) DAC (Fig. 8) and the input DAC is a N2-Bit (16-bit) predistortion R-2R DAC. Without complicating the analysis, both DACs are considered to be positive slope with respect to their control codes.

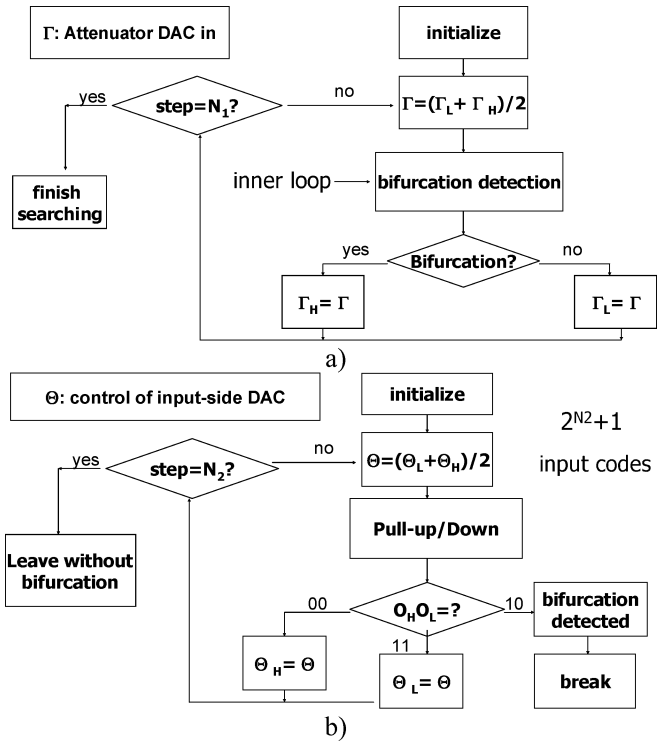

Fig. 17. (a) Bifurcation-parameter pushing algorithm. (b) Bifurcation-detecting algorithm.

D. Property of Input-Side DAC and Attenuator DAC

In order to compensate all possible offsets, the DAC should have sufficient coverage. Furthermore, all tiny bifurcation windows should be triggered in order to catch possible bifurcation with the optimal attenuation factor; it is preferred that all tiny bifurcation windows can be triggered in. Simulations show that an input of 10 μV with 80-dB unstable gain may cause 0.01-V hysteresis output. This 10-μV hysteresis input was considered to be detectable range $L_{\rm spec}$. Thus, a high-resolution DAC with analog out $\chi(\Theta)$ from a digital code Θ is needed. These lead to two main design constraints—sufficient coverage of offset and small positive jump in DAC output change, as shown by

$$\chi(\Theta=0) < \text{Offset}_{\min} < \text{Offset}_{\max} < \chi(\Theta=2^{N2}) \quad (22)$$

$$\varepsilon_\chi = \max_{0\le\Theta\le 2^{N2}-1} \{\chi(\Theta+1)-\chi(\Theta)\} \le L_{\rm spec}. \quad (23)$$

It turns out to be very tedious to get accurate boundary of offset and necessary resolution, as specifications are based on some experiments and empirical knowledge with sufficient margin. This is why a 16-b DAC with 0.2-V full range was proposed.

An input-side 16-b DAC sounds like a very expensive, area-consuming, and difficult design. In reality, it is really a lousy DAC with a small positive step and possible large negative jump R-2R DAC. This R-2R ladder has been predistorted to be R-1.8R so that no large positive jump exists. Fig. 18 shows the 8-b MSB in the 16-b DAC transfer. The simulated largest positive jump is only 5 μV while the negative jump can go to 0.01 V.

Fig. 18 shows the 16-b DAC transfer curve (8-b MSB is used to illustrate the transfer.). Simulated largest positive jump is only 5 μV while negative jump can go to 0.01 V.

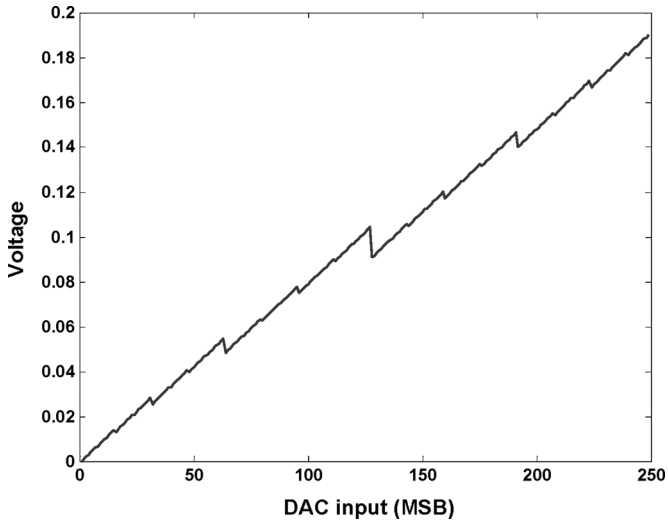

Fig. 18. Offset compensation DAC characteristic (8-MSB).

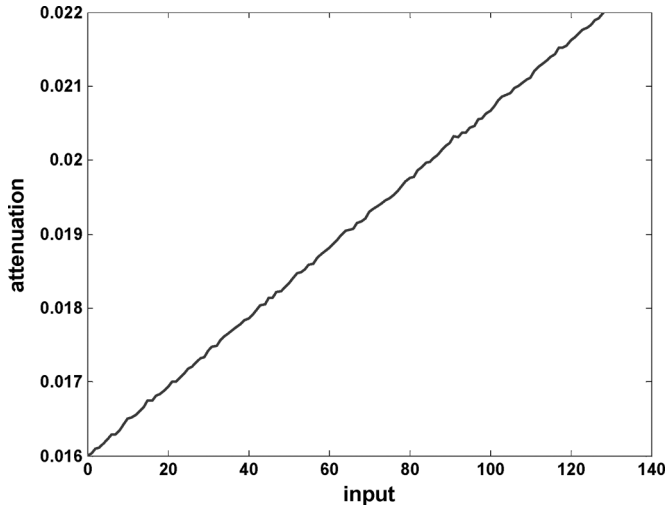

Fig. 19. Attenuator DAC linearity.

A 7-b monotone attenuator DAC was designed to cover desired attenuation range over PVT variations. Fig. 19 shows its transfer characteristics.

E. Implementation of the Two-Loop Binary Searching Algorithm

The proposed two-loop optimal bifurcation parameter tuning algorithm can be realized in integrated-circuits using the finite-state machine (FSM) approach. The flowchart shown in Fig. 17 clearly expresses the necessary state flow. This algorithm is described using Verilog HDL and synthesized as a controller with dc (Synopsys tool) with 0.5-μm standard library cells. This controller was floor-planned and routed using the DSM module in Cadence. Its layout was automatically generated in this flow. Fig. 20 shows the layout.

V. System- and Circuit-Level Simulation Results

Bifurcation detection and branching parameter tuning algorithms are verified in MATLAB and then transferred into synthesizable HDL codes using FSM. Digital logic part is in HDL

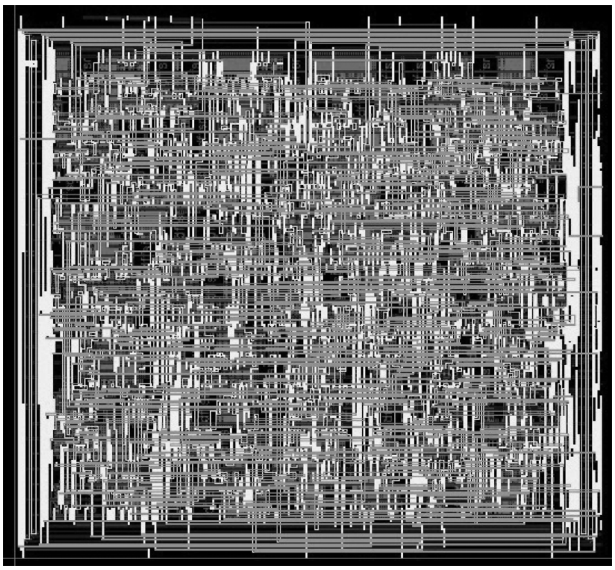

Fig. 20. Layout of the controller realizing bifurcation searching algorithm.

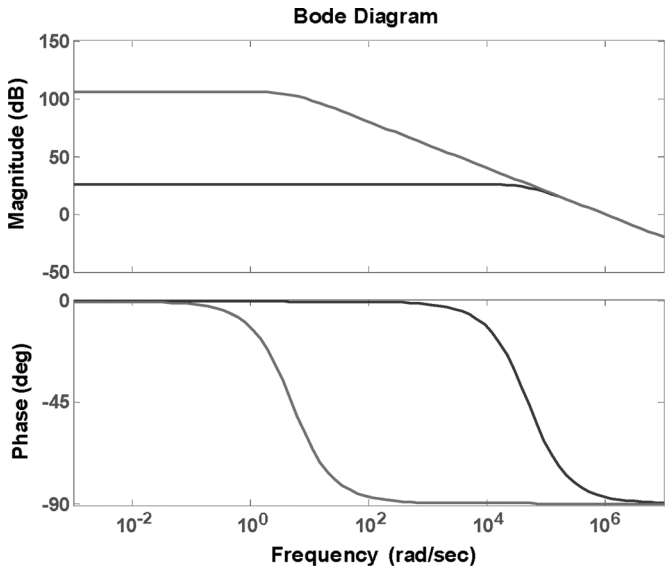

Fig. 21. Frequency responses of the amplifier (precalibration and post-calibration).

codes while all analog circuits are at the transistor-level. The main amplifier in Fig. 16 has been simulated with 65-nm predicted CMOS process as well as 90-nm–0.5-μm processes using either industrial BSIM3v3 models or predicted BSIM4 models. The whole system was simulated in a mixed-signal environment using Cadence tools.

Fig. 21 shows the ac response of the PFA with an automatic-searched optimal control code $\Gamma(0101110)$ (red) and an all-1 control code. As predicted by (21), more than 60-dB gain enhancement was obtained with $\Delta = 0.001$.

Fig. 22 shows the automatic control-code searching procedure by the algorithm. Because of $\mu = \mu_{\min} + \Gamma \times \Delta$, bifurcation presents when Γ is large. After finishing branching parameter tuning, the final control code is the same as $\Gamma(101110)$.

Fig. 23 illustrates dc transfer characteristics of this amplifier with two different codes. One can find that the bifurcation

Γ	64	32	48	52	50	49	48
bifurcation	yes	no	no	yes	yes	yes	no

Fig. 22. Optimal control code searching procedure.

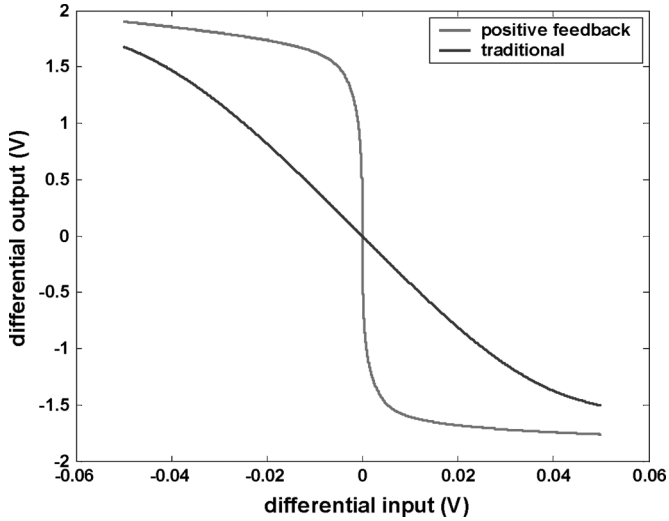

Fig. 23. DC transfer characteristics before/after tuning.

parameter-tuning algorithms boost the amplifier's output to a larger value than untuned part over all excitation ranges.

Simulation results confirmed that the two-loop bifurcation parameter-tuning algorithm works in the same manner as we designed it, and this algorithm found an optimal control code for the PFA. Furthermore, this algorithm is capable of detecting more than 80-dB gain in the bifurcation case that meets our specification.

VI. Conclusion

System dynamics of a CMOS PFA were analyzed, and its nonlinear bifurcation behavior was discussed. The bifurcation leads to a new easy-to-realize detection method in the amplifier output due to memory effect. Thus, bifurcation detection with pull-up/pull-down circuitry was introduced to reflect the amplifier's open-loop stability. Based on the bifurcation detection and programmable attenuation (functioning as bifurcation parameter), a PFA with self-calibration logic was introduced and implemented in digital CMOS technology. This method enhanced the amplifier dc gain dramatically while maintaining high power efficiency and minimizing hardware cost. Extending from traditional circuit design techniques, we developed a robust design method for high-gain low-voltage compatible amplifiers using parameter dependent bifurcation in dynamical systems. Circuit simulation results match the analytical derivation well. Our method also makes it possible to use small feature size devices to construct high-gain amplifiers with low parasitic. Low parasitic helps to enhance speed and reduce parasitic-related nonlinearity in systems such as analog-to-digital converters.

This new design with low-cost digital postprocessing techniques will enhance the stability and yield of the PFA dramatically. It will pave the way toward industrial adoption of PFAs.

Furthermore, our approach demonstrates the feasibility of high-performance analog functionalities in standard digital CMOS. Thus, our work will contribute to solving the difficult challenges in SOC as well as mixed-signal circuits and systems.

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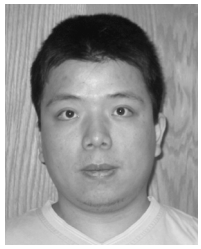
Mr. He is a member of Tau Beta Pi.



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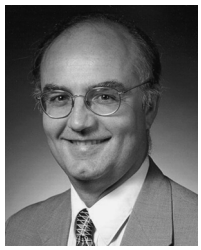

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