Code-Density Test of Analog-to-Digital Converters Using Single Low-Linearity Stimulus Signal

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Abstract

High-precision ADC testing is a challenging problem because of its stringent requirement on test signal's linearity. This work introduces a method using a nonlinear stimulus signal for testing linearity of high-resolution cyclic and pipelined ADCs by exploiting their architecture information. Simulation and experiments show that 16-bit ADCs can be tested to 1- LSB accuracy by using a 7-bit linear signal. This approach provides a solution to both the production and on-chip testing problems of high-resolution ADCs.

1. Background

The analog-to-digital converter (ADC) is one of the world's largest volume mixed-signal products and is viewed as one of the system drivers for AMS chip design [1]. Linearity test of high-performance ADCs is a well-known important and challenging problem. A precision linearity test can help validate the design of an ADC, reduce the number of wasted parts, and enable calibration, so accurate test methods are necessary for high-resolution high-speed ADCs.

The ADC testing capability is mainly determined by three enabling technologies: fast data capture, precision clock timing and linear stimulus generation [2]. The bottle neck in testing of next generation high-performance ADCs is the linear signal generation, as the present technologies on timing and data capture can handle the testing need of up coming ADCs. The code-density test method [3, 4] is widely adopted for testing ADCs' static linearity in the industry, because its implementation is straightforward and its computational complexity is low. The code-density method uses a ramp or sine wave as the stimulus signal, with linearity at least one decade better than the specification of the ADC under test. This linearity requirement makes the test of high-resolution ADCs a very challenging problem.

The authors developed a stimulus error identification and removal (SEIR) algorithm to test linearity of high-resolution ADCs using two nonlinear signals [5], and a strategy that minimizes the effect of environment nonstationarity on the test results [6]. The combination of the two methods provides a solution to testing high-performance ADCs utilizing low-linearity stimuli in a realistic time-varying environment. This methodology is a general I/O based testing method. It takes the ADC under test as a black box and does not make use of any information on the ADC architecture.

Further investigation shows that exploiting knowledge on the ADC architecture can help simplify the SEIR testing algorithm. This work introduces such an approach using a single nonlinear signal for testing ADCs with some widely adopted architectures, including cyclic and pipelined ADCs. It first identifies the input nonlinearity based on the ADC's structure characteristics, and then accurately measures the ADC's linearity. Simulation and experimental results show that 16-bit ADCs can be tested to 1-LSB accuracy by using a 7-bit linear signal. This approach provides a solution to both production and on-chip testing problems of high-resolution ADCs, since it does not have stringent requirement on the stimulus signal and its computational complexity is low.

2. Characteristics of Pipeline ADCs

Among different ADC architectures, the pipelined ADC is a balanced combination of the speed, accuracy, and power consumption. A general block diagram of a pipelined ADC is drawn in Fig. 1 [7]. It usually consists of a front-end sample-and-hold amplifier (SHA), k conversion stages, and some digital circuits for output code generation. The sampled input voltage, v_0, will be quantized by a low-resolution sub-ADC in the first stage, and the residue is amplified and sent to

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the second stage. The subsequent stages will process the residue of the previous stage in a similar way. The output codes of these stages will be appropriately assembled to give a quantized value of the input with very high accuracy.

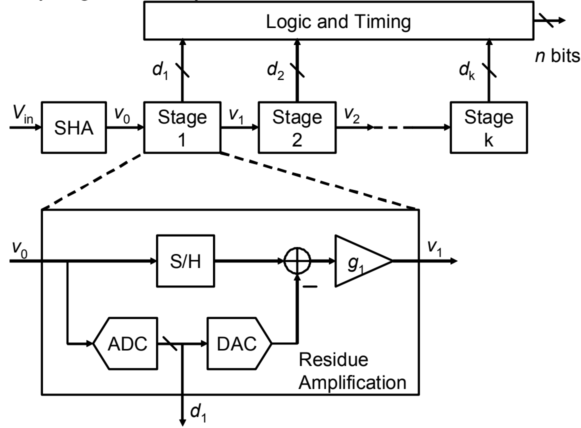

Fig. 1. Block Diagram of an *n*-bit Pipeline ADC.

2.1. Conversion Stage Modeling

Different sources contribute to the final errors in the ADC. The error sources include distortion of the front-end SHA, mismatches and linearity errors in the sub-ADCs and DACs, gain error and nonlinearity of the residue amplifier, and so on. Some of the error sources do not cause significant problems. For instance, existing front-end SHA circuits can have very low distortion at extremely high speed, so they are usually viewed as linear. Other sources can cause errors such as non-monotonicity, missing codes, and nonlinear transfer characteristics.

Common terminologies for ADC parameters and its linearity specifications used in the paper will follow the definitions in [8]. Using the one-bit-per-stage architecture as an example, the transfer function of the first conversion stage of a pipelined ADC can be summarized into a mathematical model as

$$d_1 = \begin{cases} 1, & v_{o1} \le V_{in}; \\ 0, & V_{in} < v_{o1}, \end{cases} \tag{1}$$

and

$$v_1 = \begin{cases} g_1(V_{in} - v_{p1}), & d_1 = 1; \\ g_1(V_{in} - v_{n1}), & d_1 = 0, \end{cases} \tag{2}$$

where V_{in} is the input voltage, d_1 is the one-bit digital output of the first stage, v_1 is the residue of the first stage and the input to the second conversion stage, v_{o1} is the offset voltage, v_{p1} and v_{n1} are input voltages generating a zero residue, and $g_1(\cdot)$ is a transfer function representing nonlinear effects of the first stage's residue amplifier. It is assumed the front-end SHA is linear, so $v_0 = V_{in}$ in Fig. 1.

Ideally, the offset voltage is zero, and the input voltage equal to +/– $V_{ref}/2$ should generate a residue voltage equal to zero. Mismatch errors will cause them to deviate from the desired values. The transfer function $g_1(\cdot)$ is supposed to be a straight line, but the actual gain will drop as the output voltage increases [9]. Fig. 2 shows a realistic residue transfer curve in solid lines, where dashed lines compose the ideal curve. Errors in the figure are exaggerated for a better visualization.

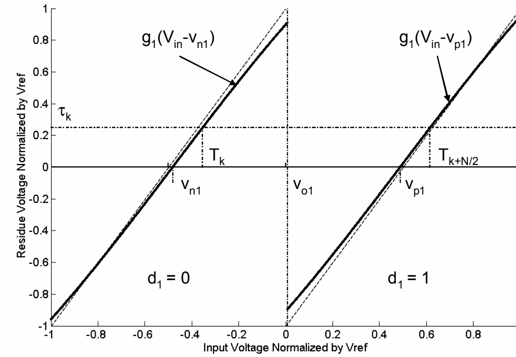

Fig. 2. Transfer curve of residue amplification.

2.2. Transition Level Characterization

The residue voltage of the first stage, v_1, will be quantized by the following stages. To v_1, these stages work as an n–1 bit sub-ADC with transition levels τ_k, k= 1, 2, …, N/2–1, where N=2^n. It is easy to show that when v_1 goes across a specific τ_k, corresponding V_{in} crosses a transition level of the overall ADC $T_{k'}$, because a change in the output of the following stages is obviously a change in the output of the whole ADC. Since the first stage's output can have 0 and 1 two values, $v_1 = \tau_k$ is associated with two input voltages $V_{in} = T_k$ and $T_{k+N/2}$ that are smaller and larger than v_{o1}, respectively, as marked with dash-dotted lines in Fig. 2. Substituting these relations into (2), we get

$$\tau_k = g_1(T_k - v_{n1}), \qquad d_1 = 0, \tag{3}$$

and

$$\tau_k = g_1(T_{k+N/2} - v_{p1}), \qquad d_1 = 1, \tag{4}$$

for k from 1 to N/2 – 1. Taking the inverse function of $g_1(\cdot)$ on above equations gives

$$g_1^{-1}(\tau_k) = T_k - v_{n1} = T_{k+N/2} - v_{p1}. \tag{5}$$

We can rewrite the second equality in (5) as

$$T_{k+N/2} - T_k = v_{p1} - v_{n1}. \tag{6}$$

It means that the difference between $T_{k+N/2}$ and T_k is a constant v_{p1}–v_{n1}.

Equation (6) is a general relationship between the upper half transition levels, T_k with $k > N/2$, and lower half transition levels, T_k with $k < N/2$, of a pipeline ADC. It is applicable to all k = 1, 2, …, N/2-1. This

result is not surprising because the residue amplification and quantization for input voltages smaller and larger than the offset v_{o1} are identical, except for the constant voltage shift v_{n1} and v_{p1}. Based on the above observation, we conclude that (6) is correct for other popular architectures such as cyclic ADCs and successive approximation register (SAR) ADCs with a binary-weighted internal DAC, whose transfer function are repeated for small and large input voltages. Therefore, the algorithm that will be developed in the following section is applicable to these types of ADCs as well.

3. ADC Test Using Nonlinear Stimulus

We are going to introduce an algorithm uses a nonlinear signal to test high-resolution ADCs with pipeline, cyclic or other similar architectures. The input nonlinearity will be first identified based on the ADC's inherent property. Linearity of the ADC itself will then be accurately estimated.

3.1. Input Signal Modeling and Histogram Test

We model the input signal $s(t)$ as a linear ramp plus a nonlinear term $F(t)$,

$$s(t) = t + F(t). \tag{7}$$

The amplitude and the offset of the input signal do not directly affect the linearity test results, so the linear component's coefficient is normalized to one and the offset assumed to be zero in (7). Testing the ADC with this input signal, we can get a set of histogram count H_k's for code k from 0 to $N-1$. The transition levels of the ADC can be estimated using the histogram counts as

$$\hat{T}_k = t_k + F(t_k) \quad (8.a)$$

$$= T_k + e_k, \quad (8.b)$$

where

$$t_k = \sum_{j=0}^{k-1} H_j \Big/ \sum_{j=0}^{N-1} H_j \tag{9}$$

in (8.a) is the measured time at which the output code's transition between $k-1$ and k happens, and (8.b) explicitly gives the estimation error e_k. However, the nonlinear component $F(t)$ is unknown, so (8.a) cannot give the value of T_k. If we would like to use a nonlinear signal in ADC testing, we have to accurately identify $F(t)$ first.

3.2. Test Using Single Nonlinear Signal

Based on our discussion in Section 2, we know that the difference between the true $T_{k+N/2}$ and T_k is a constant. So the difference between the corresponding estimated values of them should be a constant as well with some estimation error effects. Plugging (8.b) into (6) gives

$$\hat{T}_{k+N/2} - \hat{T}_k = v_{p1} - v_{n1} + e_{k+N/2} - e_k. \tag{10}$$

Substituting (8.a) into (10), we get

$$t_{k+N/2} - t_k = F(t_k) - F(t_{k+N/2}) + v_{p1} - v_{n1} + e_{k+N/2} - e_k. \tag{11}$$

If the difference between $t_{k+N/2}$ and t_k is not a constant, it is because of the input nonlinearity.

In [5], we have successfully shown that series expansion over a set of basis functions and the least squares (LS) method can be used to identify the input error in two identical nonlinear signals with a constant offset in between. We will use this technique again in this paper. $F(t)$ can be expanded as

$$F(t) = \sum_{j=1}^{M} \alpha_j F_j(t), \tag{12}$$

where $\{F_j(t),\ j = 1,\ 2,\ \ldots,\ M\}$ is a set of complete functions, and α_j's are unknown coefficients. This expansion can be used in (11), and we can get

$$\begin{aligned} & e_{k+N/2} - e_k \\ & = t_{k+N/2} - t_k + \sum_{j=1}^{M} \alpha_j [F_j(t_{k+N/2}) - F_j(t_k)] - \Delta v, \end{aligned} \tag{13}$$

where $\Delta v = v_{p1} - v_{n1}$. The left hand side of (13) contains only error terms. Ideally they should be zero. We have an abundant number of, $N/2 - 1$, equations like (13) for k from 1 to $N/2 - 1$, because N can be as large as tens of thousands for high-resolution ADCs. Usually the input nonlinearity can be concisely described by a reasonable small number of basis functions, i.e. M is much smaller than $N/2 - 1$. So we have plenty of equations, linear in a small number of variables. Therefore, the LS method can be used to estimate α_j's and Δv. If we are going to minimize the target function of the total energy of estimation errors, the corresponding estimated values are,

$$\begin{aligned} & \{\hat{\alpha}_j 's, \Delta\hat{v}\} = \arg\min\{ \\ & \sum_{k=1}^{N/2-1} \left(t_{k+N/2} - t_k + \sum_{j=1}^{M} \alpha_j [F_j(t_{k+N/2}) - F_j(t_k)] - \Delta v \right)^2 \}. \end{aligned} \tag{14}$$

Substituting these estimations into (8.a), we can now get the ADC transition levels as

$$\hat{T}_k = t_k + \sum_{j=1}^{M} \hat{\alpha}_j F_j(t_k), \tag{15}$$

for all k from 1 to $N-1$. Based on these estimated transition levels, we can calculate the linearity specifications of interest, such as INL and DNL, according to their definitions. Because the input nonlinearity is identified and removed, the linearity test result has very high accuracy.

4. Simulation Results

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A behavioral level model of pipeline ADCs was built in simulation for validating the performance of the proposed algorithm. The model includes the gain error, mismatch errors, amplifier nonlinearity, and other common nonideal effects in a real integrated circuit. 16-bit ADCs generated with this model have about 4 LSB INL. A noise with 2-LSB standard deviation was added to the test signals in simulation. This is sufficient to represent the noise in a typical test environment. The total number of samples is equivalent to about 16 samples per code on average.

4.1. Single ADC Testing

True INL_k of a simulated 16-bit ADC is plotted on the top of Fig. 3. It was measured with an ideal clean ramp signal without any noise. The true INL is 3.41 LSB. The simulated ADC was then tested with a 6-bit linear ramp signal. Low-order even and odd nonlinear components are synthesized for the input ramp. The stimulus signal has more than 1000 LSB errors at the 16-bit level, as shown in Fig. 5. This is an exaggerated nonlinearity for validating the performance the proposed strategy. Signals with much better linearity can be easily generated in reality. The nonlinear error of the test signal was first characterized using the parameterization and LS algorithm introduced in Section 3. The INL_k of the ADC was then calculated and plotted on the bottom of Fig. 3. The estimated INL is 3.62 LSB, which is very close to the true value. The true and tested INL_k curves match very well to each other and the difference between them is given in Fig. 4. All the INL_k test errors are less than 1 LSB at the 16 bit level. This confirms that proposed algorithm can accurately estimate and remove the input error and test 16-bit ADCs performance using a nonlinear signal.

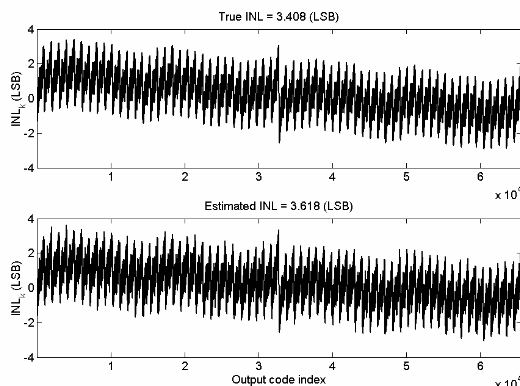

Fig. 3. True and estimated *INL*$_k$.

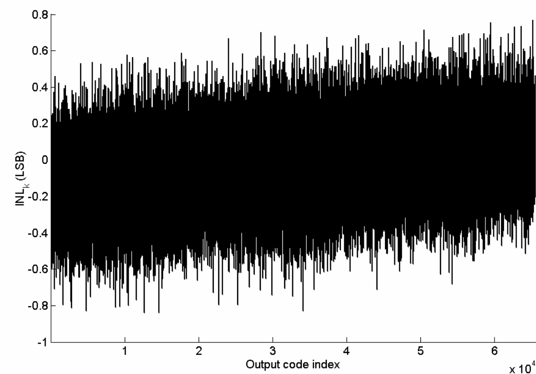

Fig. 4. Difference between *INL*$_k$ measurement results using ideal and nonlinear ramps.

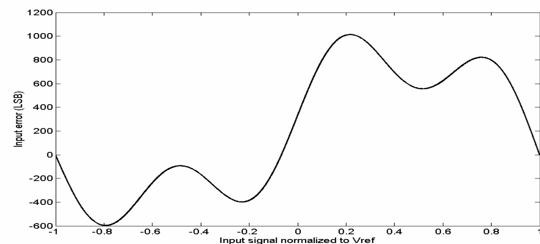

Fig. 5. Input error of the nonlinear ramp signal.

4.2. Multiple ADC Testing

The simulation was repeated more times to statistically characterize the performance of the algorithm. For saving simulation time, 14-bit pipelined ADCs were used as the device under test in these runs. Additive noise has a standard deviation of 2 LSB at the 14-bit level. The estimated INL using the single 6-bit linear signal are plotted with respect to the true values in Fig. 6. It can be observed that pairs of measured and true INL values are very well distributed along the 45 degree line in the figure. That means the estimated INL values accurately track the true values for ADCs with different linearity performance. The residue INL estimation errors are given in Fig. 7. All of the errors are less than 0.5 LSB. These data show that the proposed algorithm can consistently test high-resolution ADCs using one low-linearity signal and is robust to different ADC performance levels.

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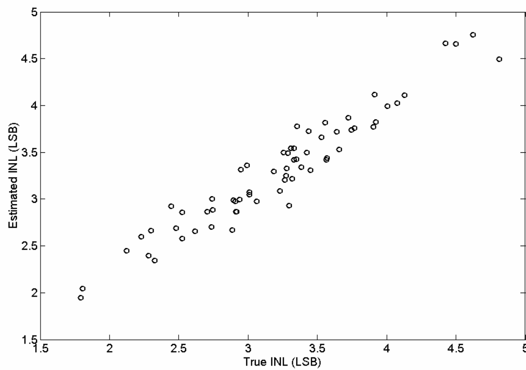

Fig. 6. Measured INL vs. True INL.

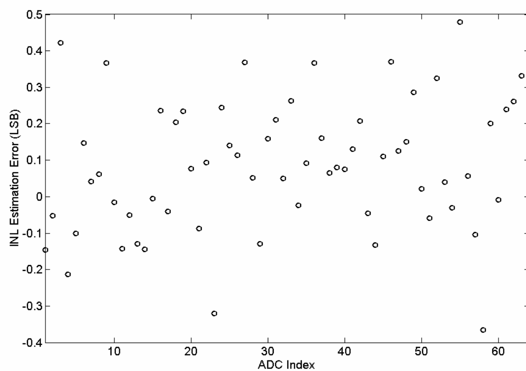

Fig. 7. Residue INL estimation errors.

5. Experimental Results

Data on 16-bit commercial ADCs collected at Texas Instruments are presented below. The ADCs under test have about 1 to 2 LSB INL, which is a known testing challenge. 32 samples per code on average are taken. The INL_k of the ADC was first tested with a linear ramp signal generated by a 20-bit sigma-delta DAC using the conventional histogram algorithm. The measured result is plotted on the top of Fig. 8. This result will be used as an accurate reference in the following comparison.

A nonlinear signal was generated by programming the input to the precision DAC. The input nonlinearity is plotted in Fig. 9. This signal has more than 300 LSB errors at the 16-bit level, so it is about 7-bit linear. This signal was used to test the same ADC again, and the measured INL_k is plotted on the bottom of Fig. 8. To assure the robustness of the proposed methodology, the detailed experimental setup was unknown to the test program and the input error was independently identified by the proposed algorithm. Using a 7-bit linear stimulus signal to test 16-bit ADCs is an extreme example. Our purpose is to sufficiently validate the capability of the proposed algorithm. Signals with much better linearity can always be generated and used in real-world practices.

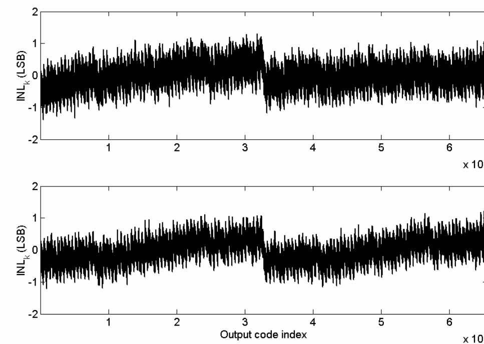

Fig. 8. Measured INL_k. Top: from 20-bit linear signal. Bottom: from 7-bit linear signal.

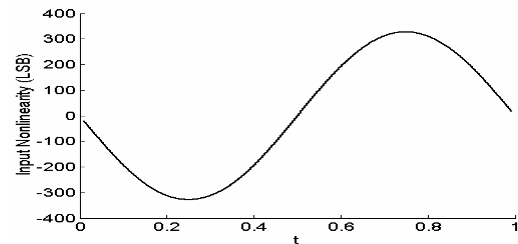

Fig. 9. Input Nonlinearity.

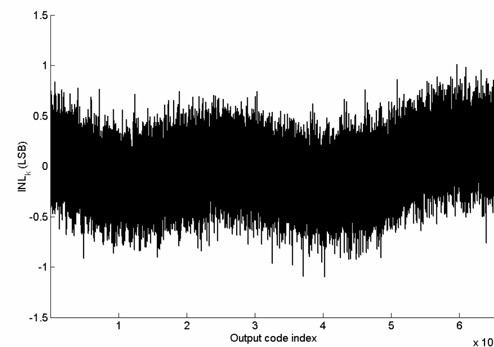

Fig. 10. Difference between INL_k measurement results using linear and nonlinear signals.

The two INL_k plots measured with the 20-bit linear signal and the 7-bit linear signal are very close to each other. The estimated INLs are 1.39 and 1.21 LSB, respectively. The difference between the two INL_k curves is plotted in Fig. 10. At different codes, the difference is almost always smaller than 1 LSB, and a significant portion of it comes from the noise in the measurement system, which can be reduced by increasing the total number of samples.

The experiment was repeated on a different ADC. The INL_k curves measured with the same linear and nonlinear signals are plotted on the top and bottom of Fig. 11, respectively, and the INL is measured as 1.66 and 1.45 LSB. Difference of estimation for the 2nd ADC is given in Fig. 12. All the errors are less than 1

LSB at the 16-bit level. This further confirms the capability of the proposed algorithm for testing high-resolution ADCs with single nonlinear signal.

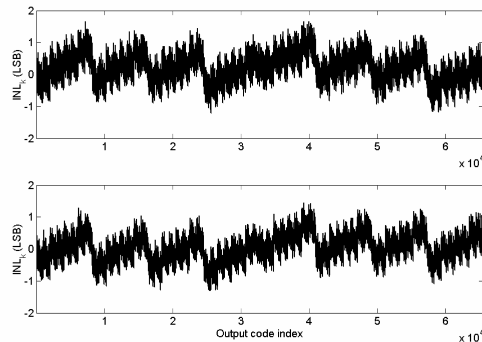

Fig. 11. Measured INL_k. Top: from 20-bit linear signal. Bottom: from 7-bit linear signal.

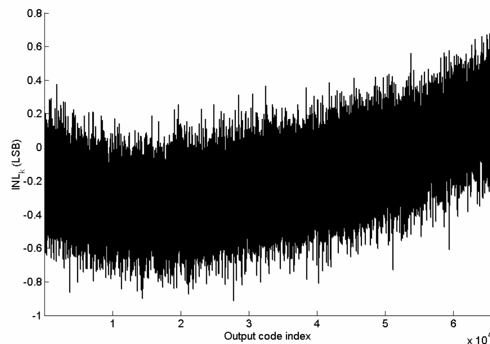

Fig. 12. Difference between INL_k measurement results using linear and nonlinear signals.

6. Conclusions

A histogram-based ADC linearity testing approach using a single nonlinear stimulus signal is introduced. This approach is applicable to some widely used architectures, such as cyclic and pipelined ADCs. The proposed algorithm exploits the ADC architecture information in data processing. It first identifies and removes the input errors using the series expansion and least squares method, and then accurately measures the ADC's linearity. Simulation and experimental results show that 16-bit ADCs can be tested to 1-LSB accuracy by using a 7-bit linear signal. This approach provides a promising solution to both the production and on-chip testing problems of high-resolution ADCs, since it does not require high-linearity stimulus signals. The proposed idea can be extended to develop similar algorithms for other AMS circuits testing.

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