A Fully Digital-Compatible BIST Strategy for ADC Linearity Testing

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Abstract

Digital testing is much easier and cheaper than analog and mixed-signal testing because of the straightforward connections and the low-cost testers. This paper presents a fully digital-compatible built-in self-test strategy for ADC linearity testing using all digital testing environments. On-chip, low-accuracy DACs, which are area efficient and simple to design, are implemented as the stimulus generator. ADCs' nonlinearities are tested using a histogram-based method under the control of a logic block. The described strategy is capable of characterizing ADC transition levels one by one with small hardware overhead. Simulation and experimental results show that the proposed circuitry and BIST strategy can test the INL_k error of 12-bit ADCs to ±0.2LSB accuracy level using only 7-bit linear DACs.

1. Introduction

The integration level of CMOS circuits is continuously evolving along with the technology scaling. As an example, today's new 65nm Pentium D CPU carries 376 millions transistors, which is about 50 times as many as the Pentium II in 350nm process nine years ago. High-level integration enables explosive growth in many new applications as well as the technologies of system-on-a-chip (SOC) and system-in-package (SIP). Consequently, analog and mixed-signal (AMS) circuits in more and more electronic systems are deeply embedded with other core semiconductor technologies, such as logic, memory, I/O and RF. Meanwhile, performances of AMS circuits keep improving to satisfy the demands of the new applications. Then, testing of these circuits becomes increasingly difficult and costly.

Data converters are the most extensively used mixed-signal circuitries. The performance of ADCs and DACs significantly affects the performance of many integrated circuits and systems [1]. In particular, sufficient linearity performance of ADCs is critically important to many applications in signal processing, communications, instrumentation and other areas. Therefore, accurate testing of linearity is indispensable for almost all ADCs to validate the design and to reduce wasted parts

In the production test, the most important issue is cost. Reducing the testing cost directly increases the profit of the products. Thus, much effort has been dedicated to developing cost-saving testing solutions with equivalent testing accuracy. There are several possible solutions for verifying AMS blocks. The first is designing a specific testing system for particular devices under test. In this case, the testing system includes a specific interface for connection, high-performance analog blocks for stimulus source generation and analog signal acquisition, memory for data storage, and a digital part for digital acquisition and analysis. This approach saves the cost of using automated test equipments (ATE). However, designing a testing system for high-performance DUTs is not a trivial task. The system has to be good enough to make sure that the test failure is from the DUT but not the testing system itself. The difficulties in designing those systems could increase the time to market of the product and then reduce the profit.

The second solution is using a general-purpose analog and mixed-signal ATE tester, like Teradyne A575. A device interface board (DIB) needs to be carefully designed for each type of DUT according to their unique electrical and mechanical testing requirements. DIBs in AMS testing are much more complicated than those in digital testing. With a good DIB design, the testing cost here is mainly determined by the AMS ATE, which is selected to provide necessary testing performance for DUTs. A high-performance ATE is far more expensive than a low-performance one. For that reason, testing high-performance DUTs is usually costly and the testing time for each DUT has to be as short as possible.

The third solution is making use of a digital ATE tester with a complex DIB [2]. By adding more functionality on the DIB, requirements on the tester are dramatically reduced and existing low-cost digital testers can be reused for analog and mixed-signal testing. Cost savings produced by the tester are substantial. However, all the analog processing blocks are integrated in the DIBs. Designing such a DIB is quite elaborate and time consuming.

The fourth possible solution for AMS testing is using a digital tester with a built-in self-test (BIST) technique. BIST circuits offer the stimulus and response verification capabilities for testing on-chip. Digital DIBs are used to simply provide point-to-point connectivity between the DUT pins and the tester, so that the testing cost can be further reduced. Compared with previous solutions, the BIST method shows an ideal way of sending the stimulus in and extracting the analog signal out of the DUT with excellent signal integrity. This advantage is more obvious

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for testing SOC and SIP systems. In addition, BIST could reduce the number of connections for testing. Therefore, more parts can be tested in parallel to reduce total testing time. In this work, we will focus on the BIST solution.

Built-in self-test has been proposed for a long time as a solution that will lower testing cost and improve testing accuracy. However, unlike the widely used digital BIST, "analog/mixed-signal BIST techniques are lagging. No proven alternative to performance-based analog testing exists and more research in this area is needed [1]." The reason is that, although BIST simplifies the testing setup and lowers the testing cost, it increases the circuit complexity and silicon area. Then, small on-chip testing circuits with minimum design effort become a prerequisite to a successful BIST strategy. Unfortunately, those circuits usually are not able to offer satisfactory testing performance for analog and mixed-signal blocks.

In this paper, we will present a BIST strategy for measuring ADCs' linearity performance. This strategy is fully compatible with digital testing environments using only digital testers and straightforward connections. On-chip circuitry for testing is able to provide high testing performance with small silicon area and minimal design effort. The rest of the paper is organized as follows. The second part briefly discusses ADCs' linearity specifications and the needs of implementing BIST for ADCs' linearity testing. Part 3 describes the structure and the performance of the proposed on-chip source generator. In Part 4, the proposed test structure and BIST strategy are presented. Simulation and experimental results are shown in Part 5 and Part 6 respectively. Finally, Part 7 concludes the paper.

2. ADCs' Linearity Characterization and BIST

2.1 ADC Linearity Specifications

The nonlinearity errors in an ADC are usually characterized by the differential non-linearity (*DNL*) and the integral non-linearity (*INL*) of its transition levels. *DNL* is the maximum deviation in the code bin widths from the ideal code bin width, 1*LSB*. *INL* is the maximum deviation of the measured transition levels from the ideal ones. In this paper, the ideal transition levels are defined by an end-point fit line passing through the first and the last transition points in the transfer curve, T_1 and T_{N-1} respectively, where N is the ADC's resolution. For an ADC transition level T_k, we define

$$DNL(k) = \frac{T_k - T_{k-1}}{LSB} - 1, \quad (1)$$

$$INL(k) = \frac{T_k - T_1}{LSB} - (k-1), \quad (2)$$

where k is the index of transition levels and $k=2, 3, \ldots, N-2$. The least significant bit (*LSB*), which is the ideal code bin width, is defined as

$$LSB = \frac{T_{N-1} - T_1}{N-2}. \quad (3)$$

Then, the *INL* and *DNL* of the ADC are the maximum values of the magnitudes of *INL(k)s* and *DNL(k)s*, respectively. From the equations, we can clearly see that ADCs' linearity characteristics are calculated from ADCs' transition levels. Thus, the major task of testing is to accurately estimate each transition level of ADCs.

2.2 BIST of ADC Linearity

There are several common methods of measuring the transition levels of ADCs. The most ubiquitous approach is the histogram test [3] [4]. It involves the use of precise linear ramp signals or ultra-pure sine wave signals as stimulus input to the ADC under test. At the output of the ADC, the histogram counts for all the possible output codes stored. With enough samples, the distribution of the output codes approaches the known distribution of the input stimulus. Then, the equality of the two distributions can be utilized to estimate the transition levels and create the *INL* and *DNL* information about the ADC. Histogram tests provide a fast way of full-code testing. But, the accuracy of the test strongly depends on the linearity of the input stimulus. In addition, it needs 2^n-1 memory cells to save the histogram counts before any of the linearity information is characterized. Both of these two factors make histogram test unsuitable for BIST solutions. The best linear ramp generator is only at about 11-12 bits level, which is not even qualified to test an ADC with moderate resolution [5] [6]. The required memory cells will increase the cost of BIST and make it even unrealistic when high resolution ADCs are under test.

Another commonly used method is the servo-loop feedback method [7]. In this case, the ADC input is driven to a specific transition level by a feedback loop. This level is then measured by an additional precise digitizer. Therefore, this method is able to target only a small subset of the ADC transition levels. This feature is preferable when high-resolution ADCs are tested, and the reduced-code testing instead of the full code testing is applied to reduce the testing time. The drawback is that this technique is quite slow and significantly limits the total number of ADC output codes that can be tested. Because the on-chip precise digitizer extremely increases the circuit cost, this solution is not suitable for BIST either.

Compared with the traditional methods, a successful BIST implementation for ADC linearity testing tends to satisfy the following conditions. First, it includes a very low-cost on-chip stimulus generator, which is more accurate than the ADCs under test (usually 3-bit or more linear) and is able to provide stimulus signals for at-speed testing.

Second, the measurement of the transition levels can be achieved accurately by simple on-chip logic circuits. Third, the BIST strategy should be capable of characterizing the specific transition levels with small hardware overhead. Finally, the *INL* and *DNL* information can be obtained with simple and small logic blocks. Since the traditional high-accuracy source generators are either particularly area consuming or very slow, the first condition becomes the bottleneck of ADC linearity BIST. In fact, there is no widely accepted solution to building such source generators.

3. On-chip Source Generator

This section will address the issue of the on-chip, low-cost source generator. The structure will be described and the testing performance will be analyzed.

3.1 The Proposed Structure

As we have discussed, traditional high-accuracy circuits are too costly to be used in BIST applications. Some methods of using low-accuracy circuits with calibration have been investigated [6] [8]. In this work, the source generator is built of a reconfigurable low-accuracy segmented current steering (SCS) DAC. A so-called deterministic dynamic element matching (DDEM) technique is used to control the reconfiguration and improve the accuracy [6].

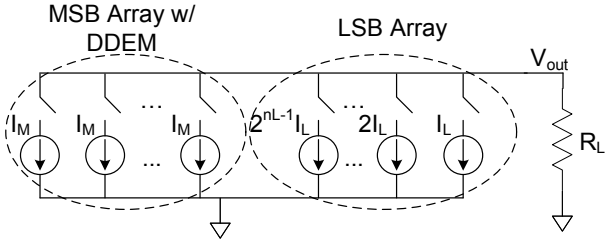
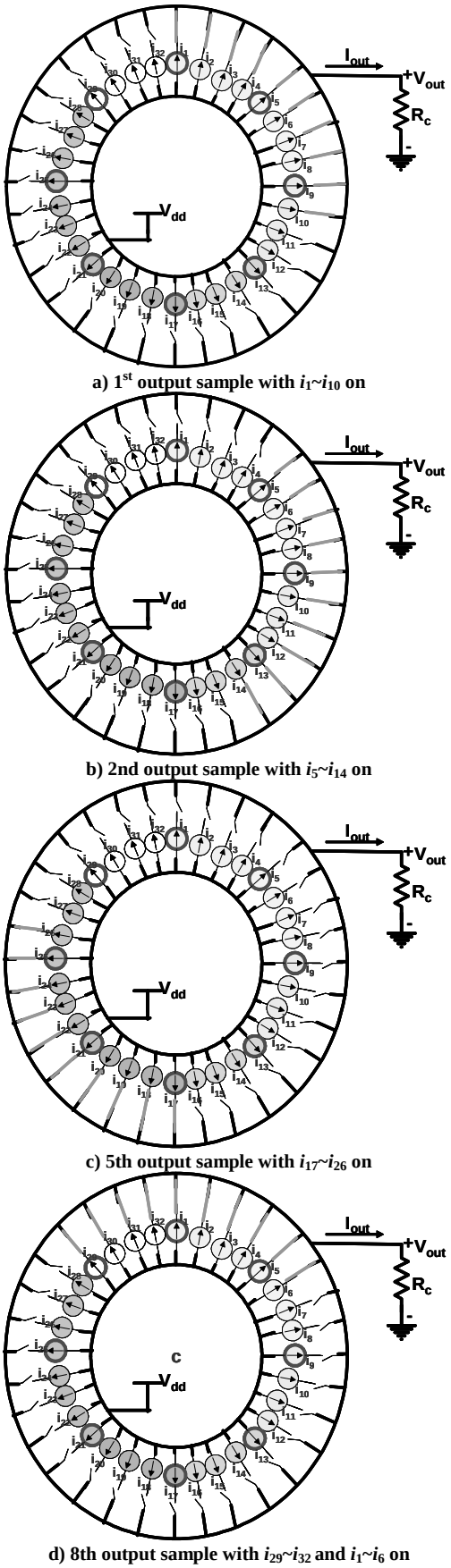


Figure 1 n-bit segmented current steering DAC

Segmented structure achieves a good combination of high resolution and small area. As shown in Figure 1, an n-bit segmented current steering DAC usually consists of an n_M-bit thermometer coded (TC) MSB array and an n_L-bit binary coded LSB array, where $n=n_M+n_L$. MSB array and LSB array generate currents according to their n_M-bit and n_L-bit input digital codes respectively. The total current generated is then forced to flow through a resistor to produce the output voltage. Assume the input codes for MSB array and LSB array are d_M and d_L respectively, the output voltage corresponds to the input code $d=2^{n_L}d_M+d_L$. Since MSB array's linearity dominates the whole DAC, it needs to meet the specification of the whole DAC in the normal case.

The deterministic dynamic element matching method is applied to the thermometer coded MSB array. It is able to increase the linearity performance of the MSB array by



a) 1st output sample with i_1~i_{10} on

b) 2nd output sample with i_5~i_{14} on

c) 5th output sample with i_{17}~i_{26} on

d) 8th output sample with i_{29}~i_{32} and i_1~i_6 on

Figure 2 5-bit DDEM DAC with P=8 and d_M=10

remapping the connections of the current cells with the input codes. The basic idea of DDEM is that instead of generating the desired signal with a costly high-performance MSB array DAC, we create a set of cheap and "poor" DACs by reconfiguration. Each of these DACs generates a series of low-resolution and low-accuracy output samples. However, if all these samples, which are distributed in a common range, follow a nearly uniform distribution, and the equivalent output linearity of the DAC is improved.

The DDEM DAC is capable of rearranging the connections of the current cells and getting different output characteristics from different configurations. Assume an n_M-bit DDEM DAC with $N_M=2^{n_M}$ current elements (i_1, i_2, ..., i_{NM}) is used as the MSB array. P is the number of different configurations generated by the DDEM control and is usually taken as a fraction of N_M. Conceptually, we put all the current elements on a circle clockwise from i_1 to i_{NM} then back to i_1, as shown in Figure 2. With an input code d_M, d_M different current elements should be connected to produce an output sample. For a normal TC current steering DAC, they could be d_M consecutive elements starting from a fixed element i_1 and going clockwise, as i_1, i_2, …, i_{dM} shown in Figure 2.a (d_M=10). For a DDEM DAC, it produces P different output samples for the input code by simply choosing P different current elements, which are evenly distributed on the circle, as start points. A simple 5-bit DDEM DAC example with P = 8 and d_M = 10 is illustrated in Figure 2. The eight start points selected are i_1, i_5, i_9, i_{13}, i_{17}, i_{21}, i_{25}, and i_{29}. Figures 2.a, 2.b, 2.c, and 2.d show the cases that the selected 10 current cells start from i_1, i_5, i_{17}, and i_{29} respectively. Therefore, to generate a stimulus sample for the ADC under test, there are three digital codes for the segmented current steering DAC, which are an n_M-bit input code for MSB array, an n_L-bit input code for LSB array, and a $\log_2 P$-bit DDEM control code for MSB array. Note that the circle does not exist in the physical design and is here only for explaining the algorithm.

3.2 Performance Analysis

In this part, we will first analyze the effect of the DDEM on the MSB array, and then we will obtain the effective testing performance of the whole SCS DAC.

Assume a separate DDEM DAC is used to measure a specific ADC transition level T_k. The measuring procedure is that under each DDEM configuration (for example the j^{th} configuration, j=1, 2, …, P), we search for a input code d_j so that the outputs of the DDEM DAC associated with input codes d_j and d_j+1, $V(d_j)$ and $V(d_j+1)$, satisfy $V(d_j)<T_k<V(d_j+1)$. Then, we can express the measurement of T_k by averaging all the d_j over j and the equivalent measured transition level is presented by

$$\hat{T}_k = \frac{1}{P}\sum_{j=1}^{P}\left(\frac{d_j}{N_M}\times\left(V_{ref+}-V_{ref-}\right)+V_{ref-}\right)=\frac{1}{P}\sum_{j=1}^{P}V_{d_j}^{id}, \quad (4)$$

where N_M is the resolution of the DDEM DAC, V_{ref+} and V_{ref-} are the reference voltages of the DAC, and $V_{d_j}^{id}$ is the output voltage of an ideal n_M-bit DAC for input code d_j. Thus, the error in measurement is

$$\begin{aligned} e_k &= \hat{T}_k - T_k \\ &= \frac{1}{P}\sum_{j=1}^{P}V_{d_j}^{id} - T_k \end{aligned}. \quad (5)$$

From the definition of d_j, we can express the true transition level T_k by

$$T_k = V_{d_j}^{j} + r_k^{j},\ j=1,2,\cdots,P, \quad (6)$$

where r_k^j is denoted as the residue voltage between the transition level and the DAC's output at code d_j. Substitute equation (6) into equation (5), and we can get the expression of the measuring error as

$$e_k = \frac{1}{P}\sum_{j=1}^{P}r_j^i - \frac{1}{P}\sum_{j=1}^{P}\left(V_{d_j}^{i} - V_{d_j}^{id}\right). \quad (7)$$

It is noticed that the term in the parentheses is actually the integral nonlinearity of the j^{th} DAC at code d_j, denoted as $INL^j(d_j)$. The definitions of DACs' $INL(k)$s and $DNL(k)$s provide the following relationships:

$$INL(k) = \sum_{i=1}^{k} DNL(i) \quad (8)$$

$$\sum_{i=1}^{N_M} DNL(i) = 0 \quad (9)$$

In DDEM reconfiguration, the differential nonlinearity errors are cyclically shifted with the unit cells. Then, equation (9) can be rewritten in another way as

$$\sum_{j=1}^{P}\sum_{t=1}^{s*q} DNL_j(t) = s\times\sum_{i=1}^{N_M} DNL_1(i) = 0, \quad (10)$$

where $q=N_M/P$ and s is a number in 1, 2, …, P. Assume s satisfies $d_j-sq \geqq 0$ for $j=1, 2, \ldots, P$. We can further express the measuring error as

$$e_k = e_1 + e_2, \quad (11)$$

$$e_1 = \frac{1}{P}\sum_{j=1}^{P} r_j^i, \quad (12)$$

$$e_2 = -\frac{LSB_M}{P}\sum_{j=1}^{P}\sum_{t=1}^{d_j-sq} DNL^j(t), \quad (13)$$

where LSB_M is the least significant bit of an ideal n_M-bit DAC. Now let us look at the variations of e_1 and e_2 for all the possible ADC transition levels since only the variation of the measuring error will affect the $INL(k)$ and $DNL(k)$

testing. First, consider the residue voltages in e_1. They are nearly in the range of one LSB_M. If an ideal n_M-bit DAC is used, the error e_1 changes from 0 to $1LSB_M$ periodically over all the ADC transition levels. The equivalent test performance of the source is at n_{DAC} bits. In this work, DDEM is applied to a very low-accuracy DAC so that the residue voltages for T_k are randomized in about one LSB_M range. Assume those residue voltages are uncorrelated. Then it can be show that the variance of e_1 is reduced by P times. Thus, the standard deviation of e_1 is expressed by

$$\sigma_{e_1} \approx \frac{\sigma_0}{\sqrt{P}}, \tag{14}$$

where σ_0 is the standard deviation of the measuring error using an ideal DAC and represents n_M-bit accuracy level. As a result, the error level of e_1 with DDEM is reduced to $n_M+0.5log_2P$ bits. The second error e_2 is induced by the nonlinearity of the original DAC. As in equation (13), e_2 with DDEM is simplified to the summation of a set of non-repeating *DNL(k)*s, the maximum value of which should be comparable to the *INL* of the original DAC, INL_M. Therefore, e_2 could vary in the range of

$$\left(-\frac{1}{P}|INL_M|, \frac{1}{P}|INL_M|\right). \tag{15}$$

Thus, the nonlinearity of the original DAC is reduced by $\log_2 P$ bits. On the whole, the equivalent testing performance of the n_M-bit DDEM DAC is expressed by

$$n_{eq} \approx \min\{n_M + 0.5\log_2 P, ENOB_M + \log_2 P\}, \tag{16}$$

where the original DAC's effective number of bits is defined as $ENOB_M=n_M-log_2INL_M-1$. It is noticed that at the ends of the DDEM DAC's output range the error e_1 is not effectively reduced by reconfiguration since the residue voltages will not be well spread. Thus, when using the DDEM structure as the source generator, the output range of the source generator should be a little larger than the input range of ADCs under test.

Now consider the segmented structure. For the j^{th} configuration of the MSB array, we can do the same code search for LSB array to get a LSB array output approaching the residue voltage r_k^j. The corresponding LSB array input code is added into the measurement of T_k. Then, as the LSB array increases the resolution of the DAC, the new residue voltage is limited by LSB_{DAC}, which is the least significant bit of the segmented DAC. The error e_1 now is lowered based on the resolution of the segmented DAC. Because the LSB array does not affect the nonlinearity of the MSB array, the error e_2 will not change with it. So for the whole segmented DDEM DAC, the equivalent testing performance is

$$n_{eq} \approx \min\{n_{DAC} + 0.5\log_2 P, ENOB_M + \log_2 P\}. \tag{17}$$

From the analysis, it is noted that the DDEM DAC can accommodate considerable nonlinearity in the circuit. In fact, the nonlinear error helps increase the effective resolution of the DDEM DAC as we have shown. Therefore, the DDEM DAC can be designed easily and with small transistors. In the latest fabrication, the current cells in the DDEM DAC are all built of the minimal-size transistors and the effectiveness of DDEM is still significant.

The target of this work is testing linearity performance of ADCs with middle or high resolution. The low-accuracy segmented DDEM DAC is built on-chip to generate stimulus input to the ADC under test. Considering the number of current cells and the complexity of the digital control block, we still want to decrease the resolution of the MSB array. In this case, although e_1 in (12) can be taken care of by the LSB array, error e_2 in (13) from the nonlinearity of the MSB array will probably limit the test performance. The reason is that when MSB array is low resolution, the number of DDEM DAC configurations, P, has to be small.

A solution to this problem is incorporating another DAC to generate extra linear dither steps at the output. As shown in Figure 3, these small dithers are added to the outputs of the DDEM DAC. Each output of the DDEM DAC is spread by N_d dither levels, where N_d is the resolution of the dither DAC. The output range of the dither DAC is equal to $q=N_M/P$ LSBs of the MSB array. From equation (12), it can be seen that the error e_2 has a repeating form with a period of q LSBs. Therefore, linearly spreading the error distribution over one period range and getting the average error distribution will effectively reduce the error variation and improve the test performance. Adding this dither DAC also increases the number of residue voltages averaged in the expression of e_1 so that it will also help reduce the error from the resolution limitation. It can be shown that the effect of the dither DAC is very similar to the way in which DDEM affects the test performance. The equivalent test performance in bits of the segmented DDEM DAC with dithering can be expressed by

$$n_{eq} \approx \min\{n_{DAC} + 0.5(\log_2 P + n_d), ENOB_{DAC} + \log_2 P + n_d\}, \tag{18}$$

where n_d is the resolution of the dither DAC in bits, n_{DAC} is the resolution of the segmented DAC and $ENOB_{DAC}$ is its effective number of bits. Here, we assume the nonlinear errors of LSB array and dither DAC is much smaller than that of MSB array. This assumption usually holds since the full ranges of the LSB array and the dither DACs are also much smaller than the DAC's output range. For effective implementation, the parameters, like n_M, n_L, P, and n_d, needs to be optimized so that both errors are reduced the same level.

As shown in Figure 3, the whole on-chip source generator consists of one low-resolution, low-accuracy thermometer MSB array with DDEM control, a binary-coded, low-

resolution LSB array, and another binary-coded, low-resolution dither DAC. Design of those circuits is quite straight forward and area saving because of the low requirement on the device matching. And the performance is not sensitive to different technologies.

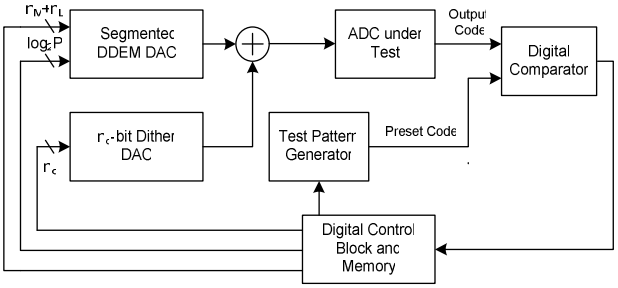


Figure 3 Proposed ADC BIST structure

4. Test Structure and BIST Strategy

This part will first discuss the details of the test structure and procedure. Then, the BIST strategy will be proposed.

4.1 Test Structure

The proposed test structure is illustrated in Figure 3. Stimulus signals to the ADC under test are generated by adding the dither DAC outputs to the outputs of the segmented DDEM DAC. Several digital codes, which include the input codes of the MSB array and the LSB array, the control code for DDEM configuration, and the input code of the dither DAC, are generated from a digital control block. This block simply consists of a state machine and some memory cells. A preset code k is set by a test-pattern generator for measuring the ADCs' k^{th} transition level T_k. The digital comparator will compare the ADC output code with the preset code k and send the result back to the control block. In addition, the comparator, with the control block, forms a digital feedback loop. During measurement, under each DDEM configuration and dither output, the feedback loop will help find the desired input codes, d_M and d_L, for the MSB array and LSB array. These codes generate the stimulus sample that is the closest to but less than the transition level T_k. The codes will be recorded to get the measurement of T_k. Binary search is applied to find those codes with fewer iteration cycles. The detailed procedure for measuring transition level T_k with the proposed structure is as follows.

1. Select a control code pair (i, j) for DDEM configuration and the dither DAC input, where $i=1, 2, \ldots, P$ and $j=1, 2, \ldots, N_D$.
2. Set k as the preset code for comparison. Do binary search for the input codes d_M and d_L, with following steps:

$set\ d_M = 0,\ d_L = 0$
$for\ v = n_M : 1$
$\quad a_M = d_M + 2\text{^}(v-1)$
$\quad a_L = d_L$
$\quad Set\ a_M\ and\ a_L\ as\ input\ codes\ for\ SCS\ DAC$
$\quad if\ ADC's\ output < k$
$\quad\quad d_M = a_M$
$\quad end$
end
$for\ u = n_L : 1$
$\quad a_L = d_L + 2\text{^}(u-1)$
$\quad a_M = d_M$
$\quad Set\ a_M\ and\ a_L\ as\ input\ codes\ for\ SCS\ DAC$
$\quad if\ ADC's\ output < k$
$\quad\quad d_L = a_L$
$\quad end$
end
$d = d_M \times 2^{n_L} + d_L$

3. Add the obtained code d into a register. Go back to step 1 if there is an unused code pair left.

After we finish the binary search for all the control code pairs, we use the summation or average of the obtained codes as the measurement of T_k and save it in a memory cell. Therefore, only one register is used to get the measurement of one transition level. The total number of register cells then is determined by how many transition levels we need to record for testing at one time. The testing time will be of great concern when high test performance is desired since the total number of binary searches is N_DP.

In the implementation of the DDEM DAC, we introduce one bit overlapping between the MSB array and the LSB array to compensate for the considerable *DNL* errors in the MSB part and make sure that all the residue voltages in equation (12) are covered by the LSB array. In this case, we will have the DAC's resolution as $n_{DAC}=n_M+n_L-1$ and the equivalent input code as $d=d_M*2\text{^}(n_L-1)+d_L$. A little change needs to be made in the second step of the above procedure.

4.2 BIST procedure

There are several levels of testing for verifying ADCs' linearity performance. Usually, the full-code INL_k testing is preferable for complete performance identifications. However, for high-resolution ADCs (which are typically slow), the data acquisition time may be prohibitively long. To cut down the test time, sometimes reduced-code testing is used. In this case, only a small subset of the ADC output codes are guaranteed. On the other hand, for production tests, we may only need to know whether an ADC meets the specification or not. This is noted as pass/fail testing. That means as long as we can find a transition level that is out of the error bound, the test is finished and characteristics of other transition levels are not important

anymore. Based on the test procedure described in the previous subsection, we are able to develop different BIST strategies for different kinds of ADC testing.

The flow chart of a pass/fail BIST procedure for ADC linearity testing is shown in Figure 4. The procedure starts after a testing enable signal is received from the digital tester. The digital control block in Figure 3 controls the testing by a state machine. The first step of the testing is characterizing the end-point fit line of the ADC under test. Transition levels, T_1 and T_{N-1}, will be measured by setting the preset code k equal to 1 and N-1 respectively. The measuring process for each transition level is described in the previous subsection. The measurements then are recorded in the memory cells as references for an ideal transfer curve. For any preset code k between 1 and N-1, the measurement of T_k can be obtained and compared with the ideal transfer curve to get the information about INL_k. The calculation is simple and can be done in digital blocks. This INL_k then is compared with the specification. If it does not meet the specification, the ADC fails the test. Otherwise, the next transition level is tested. If all the codes that need to be tested meet the specification, the ADC passes the testing. After the test is finished, a notification signal and the testing results will be sent back to the digital tester.

A test pattern generator is built on-chip to create a list of codes for testing. A simple and general way of doing that is using a counter. After measuring the fit line, the codes are tested in order from 2 to N-2. However, that is not an efficient way in terms of reducing test time if we have some extra information about the ADCs under test. Assume we can find some codes that are more possible to have large INL_k errors than others. Then, it makes sense to put those codes at the front of the list to reduce the average testing time for bad parts. Usually that information can be achieved according to the structure of ADCs.

As an example, assume n-bit pipeline ADCs using 1bit/stage structure are tested. The gain error and the comparator offset error of each stage will cause nonlinearity. It can be shown that for a good design the largest INL_k error happens the most probably around the position where the code has the MSB bit just change from 0 to 1, which is at code 2^{n-1} in decimal form. Thus, in the testing, several codes around 2^{n-1} can be tested first to get a local maximal INL_k. If it is within the error bound, the next code should be at the transition of the next MSB bit, which happens at two positions, 2^{n-2} and $2^{n-1}+2^{n-2}$, and so on. The code list according to these comments can then be generated by a state machine. For other ADCs like SAR ADCs, cyclic ADCs, and pipeline ADCs using other structures, some modifications need to be made corresponding to their own characteristics.

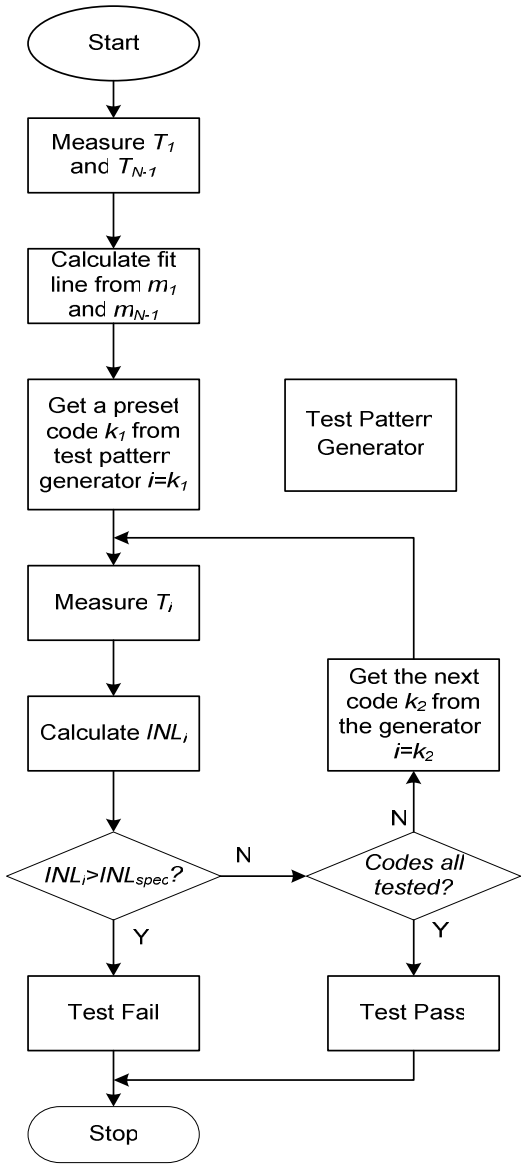


Figure 4 Flow chart of a pass/fail BIST procedure

It is noted that with some modifications to the test structure, the whole BIST strategy can also be applied to DAC testing. In this case, the ADC and the digital comparator will be replaced by the DAC under test and an analog comparator. The source generator and the comparator then form a high performance SAR ADC.

5. Simulation Results

Some simulations have been done to validate the testing performance of the stimulus generator and the proposed testing procedure. In the simulation, the segmented DDEM DAC has a 7-bit MSB array and a 6-bit LSB array. The full-scale range of the LSB array is equivalent to 2*LSB*s of the MSB part for error compensation. The parameter P is 16. So, we have a 4-bit DDEM control for configuration selection. The dither DAC has 4-bit resolution and its full

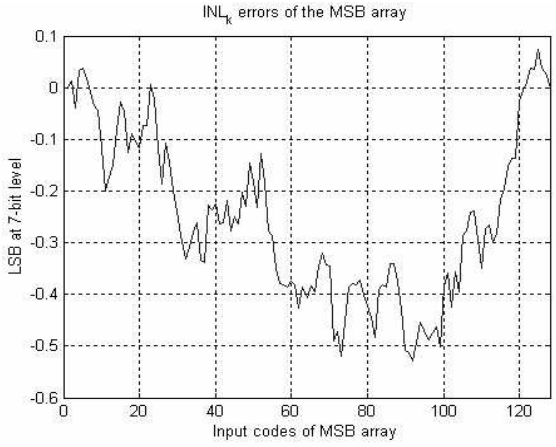


Figure 5 ***INL_k* error of the MSB array**

scale range is 8*LSB*s of the MSB array. Figure 5 shows the linearity performance of the original MSB array. The *INL* is about 0.52*LSB* and then the linearity of the MSB array is at only 7-bit level. The LSB array and the dither DAC in the simulation are both at about 6-bit level.

From the analysis of the testing performance, we can calculate the equivalent test performance in bits as

$$\begin{aligned} n_{eq} &\approx \min\{n_{DAC} + 0.5(\log_2 P + n_d), ENOB_{DAC} + \log_2 P + n_d\} \\ &\approx \min\{12 + 0.5\times(4+4), 7+4+4\} \\ &\approx \min\{16, 15\} = 15 bits \end{aligned} \quad . (19)$$

The equivalent testing performance of the stimulus generator has about 15-bit accuracy. In the simulation, a 12-bit ADC is under test. A white-noise signal is added to the input samples of the ADC to create the noise effect of a practical ADC. The standard deviation of the additive noise is set to be 0.25*LSB* at 12-bit level. The measurement of the transition levels follows the test procedure described in section 4.1. The INL_k information of each transition level is then calculated from the measurements. Figure 6 shows the true and estimated INL_k errors of the ADC under test along with the estimation errors, which is the difference between the first two plots. From the simulation, the INL_k estimation errors are bounded by about ±0.15*LSB*. Therefore, the testing performance of the stimulus source is evaluated to be at about 15-bit level, which verifies the theoretical analysis in equation (19).

To validate the robustness of the test, 100 different 12-bit ADCs are tested by 100 different implementations of the proposed test structure. The system parameters, such as *P* and the resolutions of the MSB array, the LSB array, and the dither DAC, are the same as in the previous simulation. The results are shown in Figure 7. Each dot in the figure represents one testing results. The true INL and the estimated INL of the testing are shown as the coordinates of the dot. The results show that the INL of the 100 ADCs varies from 1.5*LSB* to 5.5*LSB* and the INL estimation errors are from -0.118*LSB* to 0.139*LSB*. The testing

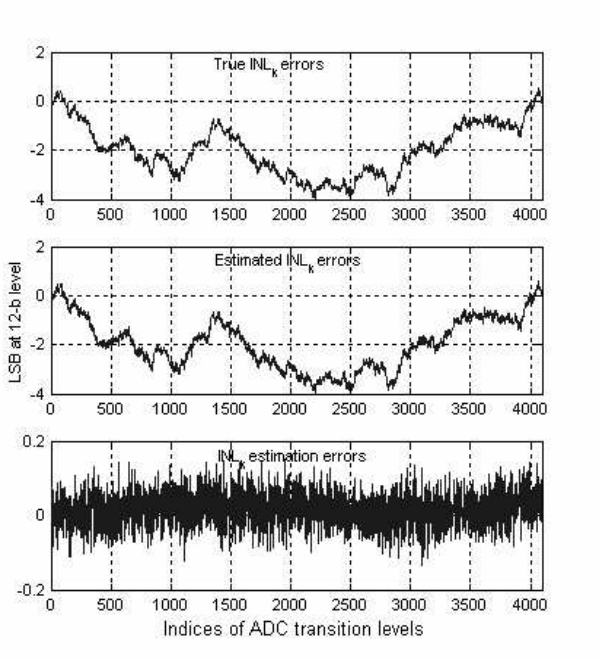


Figure 6 ***INL_k* estimation errors of ADC under test**

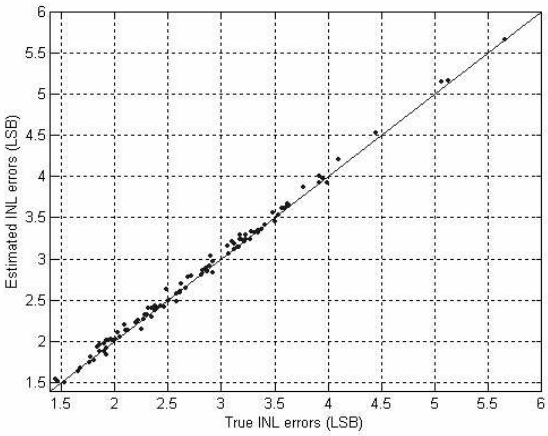


Figure 7 Estimated and True INL errors of 100 12-b ADCs

performance is very robust to the different implementations.

Analysis shows that the test performance can be improved by increasing several parameters, such as the number of configurations *P* and the resolution of the dither DAC n_d. In this simulation, *P* is increased while all the other system setups are kept. The same MSB array as shown in Figure 5 is used. Figure 8 illustrates the INL_k estimation errors of a 14-bit ADC with different values of *P*. The standard deviation of the noise in this simulation is set to be 0.25*LSB* at 14-bit level. When *P* is increased, the test performance is improved along with the cost of testing time.

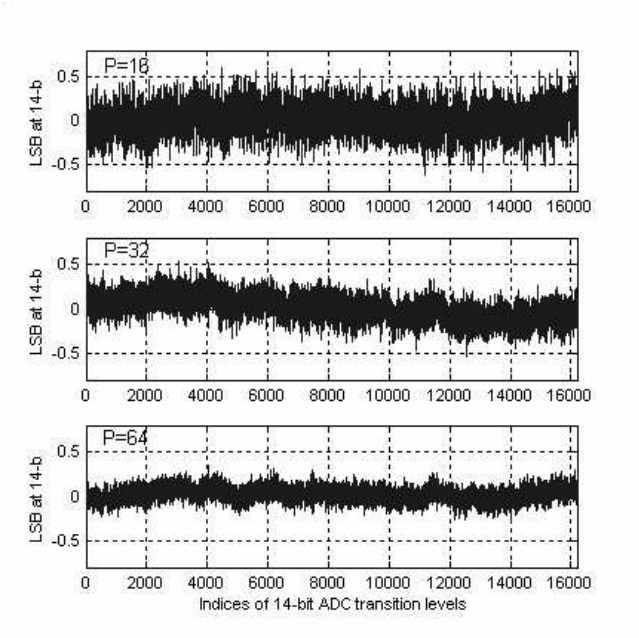


Figure 8 ***INL$_k$*** **estimation errors of a 14-b ADC with P=16, 32 and 64**

6. Experimental Results

The experimental results shown in this section are measured from the latest fabricated DDEM DAC in 0.5um CMOS process [9]. The chip includes 4096 unit current cells designed with all minimal-size transistors. The DDEM control parameter *P* can be up to 512. The differential outputs of a 7-bit DDEM MSB array with *P*=16 are measured as shown in Figure 9. Each ramp in the figure shows the output characteristics of the MSB array under one specific DDEM control code. Linearity of the original MSB array is at about 9-bit level as shown in Figure 10.

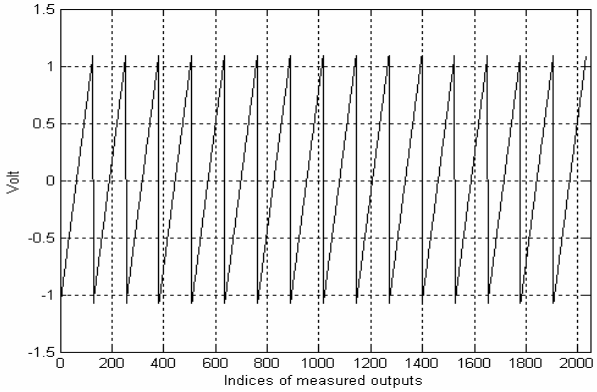


Figure 9 **Measured differential outputs of the DDEM MSB array**

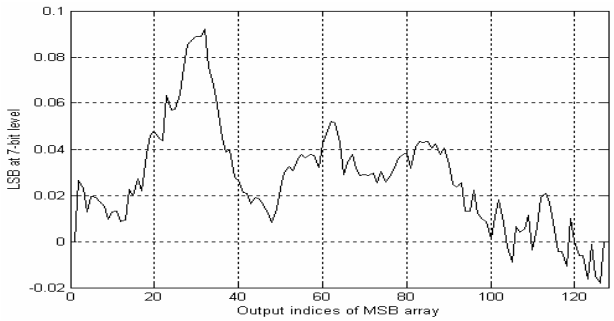


Figure 10 **Measured *INL$_k$* errors of the DDEM MSB array**

Similarly, output levels of the 6-bit LSB array and the 4-bit dither DAC are measured from the chip. Both of them are tested to be less than 8-bit linear. A simulated 12-bit ADC is tested using the measurements of the DACs to verify the testing performance of the measured data. Figure 11 shows the true and the estimated INL_k errors along with the estimation errors. The results prove the testing performance of the proposed source generator and the testing procedure. It is noted that although the linearity of the MSB array is 2-bit better than in the simulation section, the testing performance is still at 15~16 bits level because of the error coming from the resolution limitation as in equation (18).

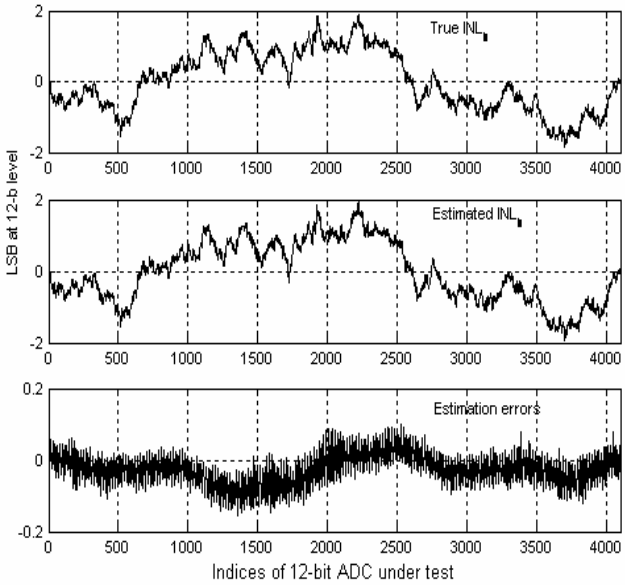


Figure 11 **Testing results of the simulated 12-b ADC using measured data**

7. Conclusions

Using a digital tester with BIST for analog and mixed-signal testing is an ideal way of reducing the test cost and improving the test quality. However, the traditional high performance circuits and testing solutions are too costly and complicated to be built on-chip just for testing. In this paper, the authors propose a BIST strategy for ADC

linearity testing, which is fully compatible with digital test environments using a low-cost digital tester and a simple digital DIB. Low-resolution and low-accuracy DACs (which are cost efficient) are built on-chip as source generators. The testing performance is guaranteed by the DDEM reconfiguration technique and the testing procedure. Design of the on-chip testing circuits could be as easy as digital design because of the low accuracy requirements on the analog blocks. Simulation and experimental results demonstrate that the proposed strategy is able to test the INL_k error of 12-bit ADCs to ±0.2*LSB* accuracy level using very low-accuracy DACs. In addition, the BIST strategy can be easily adopted for DAC testing with a little modification.

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