SEIR Linearity Testing of Precision A/D Converters in Nonstationary Environments With Center-Symmetric Interleaving

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***Abstract*—This paper describes an approach for analog-to-digital converter (ADC) linearity testing that can tolerate environmental nonstationarity and use low-precision test signals. The effects of stimulus errors on ADC testing results will be identified and removed by exploiting the functional relationship of input signals. The effects of environmental nonstationarity will be suppressed by interleaving input signals with a center-symmetric pattern. This approach can be applied to testing of ADCs of very high performance, such as 16-bit or higher resolution and more than 1 MSPS sampling rates, to which there is hardly a well-established solution for full-code testing. Simulation and experimental results show that a 16-bit ADC can be tested to one-least-significant-bit accuracy by using input signals of seven-bit linearity in an environment with more than 100-ppm/min nonstationarity. The proposed method can help control the cost of ADC production tests, extend the test coverage of current solutions, and enable built-in self-tests and test-based self-calibrations.**

***Index Terms*—Analog-to-digital converter (ADC), center-symmetric interleaving (CSI), differential nonlinearity (DNL), integral nonlinearity (INL), linearity test, nonlinear stimulus signal, nonstationary test environment, stimulus error identification and removal (SEIR) algorithm.**

I. Introduction

THE ANALOG-to-digital converter (ADC) is one of the world's largest volume analog and mixed-signal (AMS) integrated circuit products and is viewed as one of the system drivers for the AMS chip design [1]. Linearity testing of high-performance ADCs is a well-known important and challenging problem, and the testing cost has an essential meaning to the manufacturers because of the high volume. In a previous paper, the authors introduced an ADC test algorithm that uses nonlinear signals with stimulus error identification and removal (SEIR) [2]. The authors also developed a signal generation strategy that can eliminate the effect of environment nonstationarity on the test results [3]. The combination of the two methods will provide a solution to production tests of high-performance ADCs, utilizing low-linearity stimuli in a non-stationary environment. Simulation and experimental results show that the proposed technique can accurately test 16-bit ADCs using seven-bit linear signals in an environment with more than 100-ppm/min nonstationarity. Since the combined strategy allows the use of nonlinear but fast signals in tests, it is applicable to ADCs with 16-bit or higher resolution and a sampling rate of more than 1 MSPS, which do not have a practical solution for full-code testing because of the prohibitively long test time that conventional methods require. It can also work in a test environment with stability that is worse than that of the application environment but still provides accurate test results. Additionally, this approach can help reduce the test cost if combined with current solutions and enable testing of a wider range of specifications at a manageable cost.

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II. ADC Linearity Testing With SEIR

This section will briefly review the method, requirement, and bottleneck of the ADC linearity test and the SEIR algorithm as a solution for testing high-resolution ADCs.

A. Linearity Testing of High-Performance ADCs

The quasi-static linearity of ADCs is conventionally tested with the histogram approach by using a ramp or sine-wave input signal with linearity at least one decade better than the specified resolution of the ADC under test [4]–[6]. The test of high-resolution ADCs is an increasingly challenging problem since the resolution of ADCs is continuously going up, along with the emerging demand for high-performance applications in communications, imaging, and industrial controls [7], [8]. The ADC testing capability is mainly determined by the following three enabling technologies: 1) fast data capture; 2) precision clock timing; and 3) linear stimulus generation [9]. The bottleneck of testing next-generation high-performance ADCs lies in the linear signal generation, as present state-of-the-art technologies on clock timing and data capture can handle the upcoming ADCs.

A full-code histogram test for a high-resolution ADC requires a large number of samples, which implies a long and expensive test time [10]. In some linearity testing practices, only a reduced set of codes is tested to control the test cost. Due to the long test time, the nonstationarity of the test environment will cause errors in linearity testing; it will also become a problem when the resolution of ADCs under test increases. A highly linear signal source does not necessarily have good stationarity and vice versa [2]. Although the industry has spent a lot of effort on designing and maintaining a stationary test environment, few discussions about the stationarity issue can

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be found in the literature. Because of these facts, there is lack of widely adopted cost-effective approaches for testing high-performance ADCs that are pushing the edge of current technologies. A precision linearity test can help validate the design of a high-performance ADC, reduce the number of wasted parts, and enable calibration; therefore, it is necessary to develop methods to accurately characterize linearity of high-resolution high-speed ADCs.

B. SEIR Algorithm

The SEIR algorithm that was proposed in [2] uses the following two ramp signals with a constant offset α to test an ADC:

$$x_1(t) = t + F(t) = t + \sum_{j=1}^{M} a_j F_j(t) \quad (1)$$

and

$$x_2(t) = x_1(t) - \alpha \quad (2)$$

where $F_j(t)$'s are basis functions that are used to parameterize the input nonlinearity $F(t)$ with coefficients a_j's. Feeding the two ramps into an ADC under test, we collect two sets of histogram data $H_{k,1}$'s and $H_{k,2}$'s and get two estimates for a transition level T_k, respectively, as follows:

$$\hat{T}_{k,1} = \hat{t}_{k,1} + \sum_{j=1}^{M} a_j F_j(\hat{t}_{k,1}) = T_k + e_{k,1} \quad (3)$$

and

$$\hat{T}_{k,2} = \hat{t}_{k,2} + \sum_{j=1}^{M} a_j F_j(\hat{t}_{k,2}) - \alpha = T_k + e_{k,2} \quad (4)$$

where $e_{k,1}$ and $e_{k,2}$ are estimation errors, and transition times are estimated from the histogram data $H_{k,1}$'s and $H_{k,2}$'s as $\hat{t}_{k,1} = \sum_{i=0}^{k} H_{i,1} / \sum_{i=0}^{N-1} H_{i,1}$ and $\hat{t}_{k,2} = \sum_{i=0}^{k} H_{i,2} / \sum_{i=0}^{N-1} H_{i,2}$. Taking the difference between (3) and (4) gives

$$e_{k,1} - e_{k,2} = \hat{t}_{k,1} - \hat{t}_{k,2} + \sum_{j=1}^{M} a_j \left[F_j(\hat{t}_{k,1}) - F_j(\hat{t}_{k,2})\right] + \alpha. \quad (5)$$

There are $N-1$ equations for k that take different values in (5), and these equations are linear in $M+1$ unknown variables: a_j's and α. Therefore, we can robustly estimate the unknowns by using the least squares (LS) method to minimize the error energy as

$$\{\hat{a}_j' s, \hat{\alpha}\} = \arg\min \left\{ \sum_{k=0}^{N-2} \left[\hat{t}_{k,1} - \hat{t}_{k,2} + \sum_{j=1}^{M} a_j \left[F_j(\hat{t}_{k,1}) - F_j(\hat{t}_{k,2})\right] + \alpha\right]^2 \right\}. \quad (6)$$

With the knowledge of ramp nonlinearity a_j's, we can remove their effects on the histogram data and accurately identify ADC transition levels as

$$\hat{T}_k = \hat{t}_{k,1} + \sum_{j=1}^{M} \hat{a}_j F_j(\hat{t}_{k,1}). \quad (7)$$

Thus, the ADC's linearity performance can be estimated. The SEIR algorithm can use nonlinear signals for testing ADCs, with testing accuracy that is comparable to that of conventional methods using highly linear signals [2]. Therefore, it is promising for cost-effective production tests and built-in self-tests of precision ADCs.

C. Implementation Issues of SEIR Algorithm

One straightforward way to generate testing signals for the SEIR algorithm is to repeat the ramp signal $x_1(t)$ twice and add an offset α to the second one. There are two critical requirements on the test environment for using the SEIR algorithm.

1) The same signal can be exactly repeated twice.
2) The offset needs to be constant.

Violating any of the two requirements will introduce errors in the test results. Test errors due to a mismatch between the two signals and due to nonconstancy of the offset will be mathematically modeled and theoretically analyzed in this paper, whereas other types of errors that are related to the total number of samples, noise in the test environment, and quantization errors were discussed in [2].

III. NONSTATIONARY TEST ENVIRONMENT

Although the test signals can be highly nonlinear in the SEIR algorithm, it is required to have two identical test signals and a constant offset. For high-precision ADC testing, changes in the test environment may cause errors that are not in agreement with the two critical requirements and will significantly degrade the testing accuracy. Causes of test environment nonstationarity include the following: changes in temperature, humidity, and other physical environment parameters introduced by cycles of heating, ventilating and air conditioning systems, turning on and off of instruments, and people walking by; changes due to aging of testing instruments; and power supply changes. It is expensive and difficult to maintain a stable environment for testing high-performance ADCs with 16-bit or higher resolution. For the purpose of testing, the "common mode" nonstationarity that affects both the testing circuitry and the ADC does not introduce errors in linearity test results. Only the relative "differential" nonstationary effects among the signal generator, the offset generator, the adder, and the ADC will cause errors. Typical examples of these effects in a test system include temperature difference between different functional blocks and errors that are introduced by internal voltage distribution networks.

A nonstationary test environment can cause errors in the two requirements and affect the test accuracy of the SEIR algorithm by changing circuit electrical variables. The following are some examples. Any increase in the temperature can change the

reference voltage of the signal generator, which will result in different test signals $x_1(t)$ and $x_1'(t)$. If, ideally, the signal generator can give out linear ramps but its output is scaled by a steadily increasing reference, the true test signals are $x_1(t) = t(1 + \Delta \cdot t) = t + \Delta \cdot t^2$ and $x_1'(t) = t(1 + \Delta \cdot t_0 + \Delta \cdot t) = t + \Delta \cdot t^2 + \Delta \cdot t_0 \cdot t$, where the reference voltage is normalized to 1 at the beginning of $x_1(t)$, Δ is the slope of reference drift, and $x_1'(t)$ starts later than $x_1(t)$ by t_0, which causes the reference voltage of $x_1'(t)$ to be larger than that of $x_1(t)$ by $\Delta \cdot t_0$. This leads to a nonconstant difference between two signals: $\Delta \cdot t_0 \cdot t$. We will use $N_1(t) = x_1(t) - x_1'(t)$ to represent the general difference between test signals. Periodical power supply fluctuation can produce a nonconstant offset $\alpha' = \alpha + \varepsilon \sin(\omega t)$, where ε is the amplitude of the power-supply-induced error, and ω is its frequency, which is usually equal to the frequency of power supply change. We will use $N_2(t) = \alpha' - \alpha$ to represent the general nonconstant part in the offset.

By shifting $x_1'(t)$ down by α', we get the true second test signal as

$$x_2(t) = x_1(t) - \alpha - N(t) \tag{8}$$

where $N(t) = N_1(t) + N_2(t)$ is a general error term in the SEIR test introduced by environment nonstationarity that violates the two critical requirements. With $N(t)$, (3) and (4) should be rewritten as

$$\begin{aligned}\hat{T}_{k,1} &= \hat{t}_{k,1} + \sum_{j=1}^{M} a_j F_j(\hat{t}_{k,1}) \\ &= T_k + e_{k,1}\end{aligned} \tag{9}$$

and

$$\begin{aligned}\hat{T}_{k,2} &= \hat{t}_{k,2} + \sum_{j=1}^{M} a_j F_j(\hat{t}_{k,2}) - \alpha - N(\hat{t}_{k,2}) \\ &= T_k + e_{k,2}.\end{aligned} \tag{10}$$

In this case, if we neglect $N(t)$ and apply the LS method as in (6), we get another estimate, which is given as follows:

$$\begin{aligned}\{\hat{a}_j^* s, \hat{\alpha}^*\} = \arg\min \Bigg\{ \sum_{k=0}^{N-2} \Big[&\hat{t}_{k,1} - \hat{t}_{k,2} \\ &+ \sum_{j=1}^{M} a_j \left[F_j(\hat{t}_{k,1}) - F_j(\hat{t}_{k,2})\right] + \alpha \Big]^2 \Bigg\}.\end{aligned} \tag{11}$$

However, the estimates with "$*$" in (11) are not equal to their true values because $N(t)$ introduces errors in input identification, which can be seen from the following analysis:

$$\begin{aligned}&\sum_{j=1}^{M} \hat{a}_j^* \left[F_j(\hat{t}_{k,1}) - F_j(\hat{t}_{k,2})\right] + \hat{\alpha}^* \\ &\quad\approx \hat{t}_{k,2} - \hat{t}_{k,1} \\ &\quad\approx \sum_{j=1}^{M} a_j \left[F_j(\hat{t}_{k,1}) - F_j(\hat{t}_{k,2})\right] + \alpha + N(\hat{t}_{k,2})\end{aligned} \tag{12}$$

where the first equality comes from (11), and the second comes from (9) and (10). The estimation errors $e_{k,1}$ and $e_{k,2}$ are neglected because they are very small with an appropriate number of samples. The estimated coefficients can be broken down into two terms, i.e., the true value a_j and the error δ_j contributed by $N(t)$, as

$$\hat{a}_j^* = a_j + \delta_j. \tag{13}$$

By substituting (13) into (12) and canceling identical terms on both sides, we get

$$\sum_{j=1}^{M} \delta_j \left[F_j(\hat{t}_{k,1}) - F_j(\hat{t}_{k,2})\right] \approx N(\hat{t}_{k,2}). \tag{14}$$

By applying series expansion to basis functions, we can simplify (14) into the following form:

$$\begin{aligned}&\sum_{j=1}^{M} \delta_j \left[F_j(\hat{t}_{k,1}) - F_j(\hat{t}_{k,2})\right] \\ &\quad\approx \sum_{j=1}^{M} \delta_j (\hat{t}_{k,1} - \hat{t}_{k,2}) \frac{d}{dt} F_j(t) \Big|_{t=\hat{t}_{k,2}} \\ &\quad\approx -\sum_{j=1}^{M} \delta_j \alpha \frac{d}{dt} F_j(t) \Big|_{t=\hat{t}_{k,2}} \\ &\quad\approx N(\hat{t}_{k,2}).\end{aligned} \tag{15}$$

Equation (15) is an approximation when the offset α is much smaller than the input range of the ADC so that $\hat{t}_{k,2} - \hat{t}_{k,1} \approx \alpha$. Integrating (15) gives the input identification error as

$$\begin{aligned}F_\delta(t) &= \sum_{j=1}^{M} \delta_j F_j(t) \\ &\approx -\frac{1}{\alpha} \int_0^t N(\tau) d\tau.\end{aligned} \tag{16}$$

This error will finally become the transition level estimation error. If the estimates from (11) are used in (7) to calculate transition levels, we get

$$\begin{aligned}\hat{T}_k &= \hat{t}_{k,1} + \sum_{j=1}^{M} \hat{a}_j^* F_j(\hat{t}_{k,1}) \\ &= \hat{t}_{k,1} + F(\hat{t}_{k,1}) + F_\delta(\hat{t}_{k,1}) \\ &= T_k + F_\delta(\hat{t}_{k,1}).\end{aligned} \tag{17}$$

For instance, if $N(t) = \Delta(t - 0.5)$, the test error will be

$$\begin{aligned}F_\delta(t) &= -\frac{1}{\alpha} \int_0^t \Delta(\tau - 0.5) d\tau \\ &= -\frac{\Delta}{2\alpha}(t^2 - t).\end{aligned} \tag{18}$$

It gives a "bell"-shaped INL_k test error with a maximum absolute value that occurs at the middle of the ADC input range. The input identification error, as well as the ADC transition

level estimation error, is proportional to the relative error $N(t)$ with respect to α. Therefore, even if the absolute error is very small as compared to the input signal range, it can still seriously hurt the final linearity test accuracy. When designing an SEIR test, appropriately increasing the value of α can reduce the effect of $N(t)$.

IV. Center-Symmetric Interleaving (CSI) of Test Signals

To deal with environment nonstationarity and meet the two critical requirements of the SEIR algorithm, we propose the use of an interleaving strategy in signal generation for testing high-performance ADCs. This means that instead of repeating a signal twice and adding an offset to the second one, we will generate many copies of the same signal and add an offset to some of them according to a given pattern. In a low-stationarity test environment, this approach can significantly reduce the negative effects of environment changes on test signals and equivalently generate two identical signals and a constant offset.

A. *Concept of Interleaving*

Interleaving has been historically used in the design and testing of electrical circuits. For designing matching-sensitive circuits that are susceptible to gradient effects, such as amplifier input stages, precision gain stages, and feedback networks, the common-centroid layout technique and extensions of this idea are ubiquitously adopted to get two or more matched electrical quantities [11], [12]. The basic idea of these approaches is to divide circuit components into many small unit cells and evenly place them on a piece of silicon such that gradient effects on the electrical parameters of these components are averaged out. They can be viewed as interleaving in a 2-D space, and it is practically proven that these approaches can significantly improve the circuit performance. As a widely adopted practice, the ramp-based histogram test for ADC linearity is usually implemented by using a periodic triangular wave as the input. One of the major reasons for taking this approach is that with the presence of environment nonstationarity, it is easier to guarantee the linearity of each individual short fast ramp, which could have different slopes from one to another but give an overall linear ramp, as compared to a long slow ramp. This method can effectively guarantee the accuracy of ADC linearity testing. The implementation of a ramp test signal as many short triangles prompts the use of interleaved signals in the SEIR test.

Both of the two test signals that were used in the SEIR algorithm are generated as triangular waves. Assume that a single period of triangular wave takes the following form:

$$x_T(t) = \begin{cases} 2t + F_T(t), & 0 \leq t < 0.5 \\ 2(1-t) + F_T(t), & 0.5 \leq t < 1 \end{cases} \tag{19}$$

where $2t$ and $2(1-t)$ are the normalized desired output of the triangular wave generator for $t < 0.5$ and $0.5 < t$, respectively, and $F_T(t)$ is a general nonlinear component in the triangular wave. If we assume that the input nonlinearity is a function of the desired output voltage, which is true for most generators that are used in quasi-static testing, the nonlinear component in (19) has the following property:

$$F_T(t) = F_T(1-t). \tag{20}$$

For ADC linearity testing, a ramp signal in (1) is equivalent to a triangle signal in (19) if

$$F_T(t) = F(2t), \quad 0 \leq t \leq 0.5. \tag{21}$$

Let us look at the equivalence between triangle and ramp signals with the help of Fig. 1. The top left part of Fig. 1(a) shows an ideal triangle signal in dashed lines and a nonlinear triangle signal in solid lines, which can be described by (19) and whose nonlinearity follows (20). For ADC testing, the triangle signal will be sampled at evenly spaced time instances, with samples being represented by small circles. If we reorder these samples with respect to their voltage magnitudes (the vertical axis) and plot them with even spaces in time (the horizontal axis), then we get a ramp signal, as the top right part of Fig. 1(a) shows, whereas the nonlinearity between the triangle and ramp signals is related by (21). The horizontal arrows in Fig. 1 indicate the reordering process. Since only the sampled voltages determine the ADC output codes and the timing order of samples are not important in ADC linearity testing, the triangle and ramp signals are equivalent in the sense that they give out the same histogram test result. The bottom part of Fig. 1(a) shows the equivalence between a periodical triangle signal and a ramp signal in ADC linearity testing. Sometimes, the reordering process is also called an unfolding process, and the ramp signal is called an unfolded signal, whereas the periodical signal is referred as a folded signal. If the time spacing is fixed during the unfolding process, the duration of the unfolded ramp is the same as that of the folded signal: 4 in the bottom part of Fig. 1(a). As we mentioned that timing information is not critical to histogram testing, we can normalize the time axis and make the bottom ramp the same as the top one without affecting the ADC quasi-static test result. Therefore, the two ramp signals on the right side of Fig. 1(a) will give the same test result, and subsequently, the periodical triangle signal will be equivalent to the normalized ramp in the sense of testing.

The SEIR test method requires two ramp signals, with one shifted from the other by a constant offset. The two signals cannot be simultaneously generated and quantized by an ADC. Generally speaking, the two desired input signals are generated as triangular waves and interleaved with each other in the time domain. The interleaved signals can be represented as

$$s(t) = \sum_{j=0}^{2N_s-1} \left[x_T(t-j) - \alpha \cdot I_\Lambda(j) g(t-j)\right] \tag{22}$$

where $I_\Lambda(j)$ is a characteristic function on an index set Λ that equals 1 if j is an element of Λ and 0 otherwise, and $g(t)$ is a gate function that equals 1 inside [0, 1] and vanishes outside the interval. The index set Λ specifies the time windows that correspond to the second signal, during which the offset will be applied. When the ADC under test is converting the signal

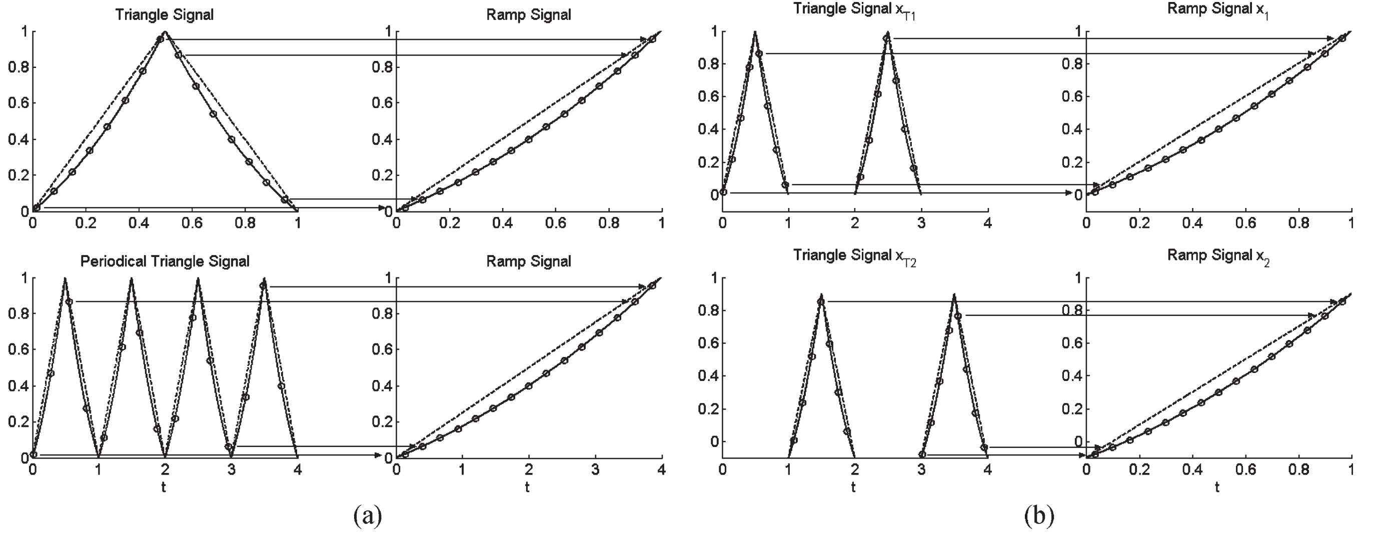

Fig. 1. (a) Equivalent triangle, periodical triangle, and ramp signals. (b) Two nonlinear triangle signals with a constant offset in between and their ramp equivalence.

$s(t)$, output codes generated during the time windows that are associated with j's outside Λ will be counted into $H_{k,1}$, and codes associated with j's in Λ will be counted into $H_{k,2}$. Based on the discussion above, the two desired test signals are

$$x_{d1}(t) = \sum_{j \notin \Lambda}^{2N_s-1} x_T(t-j) \tag{23}$$

and

$$x_{d2}(t) = \sum_{j \in \Lambda}^{2N_s-1} \left[x_T(t-j) - \alpha \cdot g(t-j)\right] \tag{24}$$

which are equivalent to (1) and (2) because samples on the two interleaved triangle signals can be unfolded and give two normalized ramp signals, as shown in Fig. 1(b). If two triangle signals are the same, two unfolded ramp signals will be the same as well, and the offset between the two ramps will be constant and equal to the offset between the original triangular waves.

B. CSI in a Nonstationary Environment

Test environment nonstationarity will inevitably introduce errors in (22). Two identical signals and a constant offset as in (23) and (24) are practically impossible to achieve. Various types of nonstationary effects exist, including deterministic and stochastic time-dependent drifting, as well as random noise. Random noise usually does not degrade test performance in an unrecoverable way since they are uncorrelated from each other, and their effects can be averaged out by a reasonable number of measurements. We will focus on the nonstationary effects that have a strong correlation during a test window of about tens of seconds to several minutes. These error terms can be modeled as deterministic slowly changing functions of time in a specific test window. We assume that these errors affect the test signal through a scaling effect in our ensuing analysis, whereas additive errors can be treated in a similar style. Based on the assumptions above, the two real test signals with nonstationary effects are

$$x_{r1}(t) = \sum_{j \notin \Lambda}^{2N_s-1} x_T(t-j)\left[1+e(t)\right] \tag{25}$$

and

$$x_{r2}(t) = \sum_{j \in \Lambda}^{2N_s-1} \left[x_T(t-j) - \alpha \cdot g(t-j)\right]\left[1+e(t)\right] \tag{26}$$

where

$$e(t) = \sum_{i=1}^{L} b_i t^i + n(t) \tag{27}$$

represents the effects of environment nonstationarity. b_j's are major coefficients of low-order polynomial error terms. $n(t)$ includes noise and high-order errors that are neglected in our discussion since we assume that the nonstationarity slowly changes in a test.

To meet the two critical requirements of the SEIR algorithm in nonstationary environments, we introduce a CSI strategy to cancel out the low-order error terms shown in (25) and (26). We first give the property of CSI, which is to determine the size and elements of the set Λ, and then explain a procedure to get such a set. The set Λ that can cancel up to the Lth-order nonstationary effects should have the property that up to the Lth moment of j's in Λ should be equal to that of j's outside Λ, which can be mathematically expressed as

$$\sum_{j \notin \Lambda}^{2N_s-1} j^l - \sum_{j \in \Lambda}^{2N_s-1} j^l = 0, \qquad l = 0, 1, \ldots, L. \tag{28}$$

One procedure to get Λ is shown as follows. It starts from a pattern of one single element [0], which will be extended to

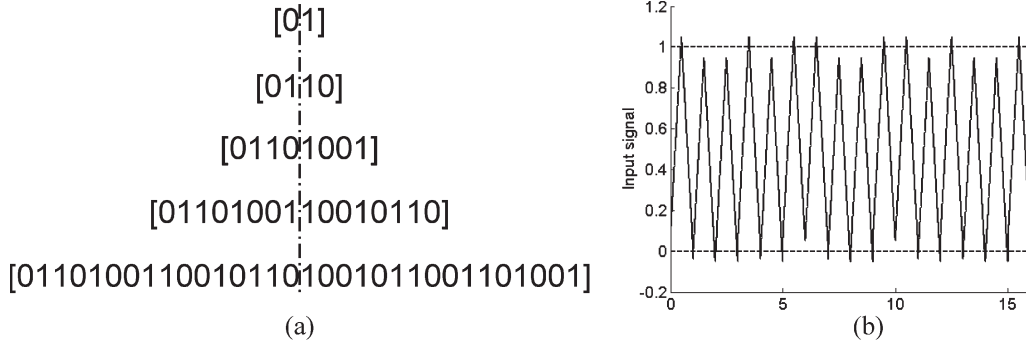

Fig. 2. (a) First five patterns for Λ generating. (b) Signal generated using the fifth pattern.

generate the elements of Λ. Extension of the pattern takes the following steps.

1) Start from the beginning of the current level pattern.
2) If a "0" is met in the current level pattern, append "01" to the next level pattern.
3) If a "1" is met in the current level pattern, append "10" to the next level pattern.
4) Finish at the end of the current level pattern.
5) Repeat the steps above with the next level pattern until the length of the pattern is equal to $2N_s = 2 \cdot 2^L$, where L is the level of the pattern.

The first five patterns are listed in Fig. 2(a). We name them the zeroth- to the fourth-level interleaving patterns. It can be observed that these patterns are symmetric or antisymmetric with respect to the center as the dash-dotted line indicated, and when dividing a pattern into two in the middle, the two subpatterns are symmetric or antisymmetric with respect to their own centers as well. That is why we call them CSI patterns, and this symmetric property leads to the capability of canceling nonstationary effects. The final pattern has a length of $2N_s$, because $2N_s$ periods of triangular waves are used in an SEIR test for two signals. Index the pattern from 0 to $2N_s - 1$. The set Λ contains the indices of "1" elements in the generating pattern. The signal generated by using the third interleaving pattern is plotted in Fig. 2(b), where a negative offset is added at j in $\Lambda = \{1, 2, 4, 7, 8, 11, 13, 14\}$. It can be verified that by using the Lth-level interleaving pattern, the lth moments of j's inside and outside Λ are equal to each other for l up to L, which is required in (28).

C. Test Signals With CSI

We now show that the two test signals that were generated with CSI are nearly identical, and the offset is nearly constant, as required by the SEIR algorithm. For investigating the effect of interleaving on test signal generation, we first set $\alpha = 0$ and then take the average of triangular wave periods for the first and second signals, respectively. The two averaged signals are

$$x_1(t) = \frac{x_T(t)}{N_s} \sum_{j \notin \Lambda}^{2N_s - 1} [1 + e(t+j)]\, g(t) \tag{29}$$

and

$$x_1'(t) = \frac{x_T(t)}{N_s} \sum_{j \in \Lambda}^{2N_s - 1} [1 + e(t+j)]\, g(t). \tag{30}$$

The difference between the averaged signals can represent the mismatch between the test signals as follows:

$$\begin{aligned} N_1(t) &= x_1(t) - x_1'(t) \\ &= \frac{x_T(t)}{N_s} \left[\sum_{j \notin \Lambda}^{2N_s - 1} e(t+j) - \sum_{j \in \Lambda}^{2N_s - 1} e(t+j) \right] g(t). \end{aligned} \tag{31}$$

From (27), we get

$$\begin{aligned} &\sum_{j \notin \Lambda}^{2N_s - 1} e(t+j) - \sum_{j \in \Lambda}^{2N_s - 1} e(t+j) \\ &= \sum_{i=1}^{L} b_i \left[\sum_{j \notin \Lambda}^{2N_s - 1} (t+j)^i - \sum_{j \in \Lambda}^{2N_s - 1} (t+j)^i \right] \\ &= \sum_{i=1}^{L} b_i \sum_{l=0}^{i} \binom{l}{i} t^{i-l} \left(\sum_{j \notin \Lambda}^{2N_s - 1} j^l - \sum_{j \in \Lambda}^{2N_s - 1} j^l \right) \end{aligned} \tag{32}$$

where the binomial coefficient of i choose l is used, and noise and high-order terms are neglected. If the Lth-order CSI is used, we know that $N_1(t) = 0$, based on (28) and (32). This means that the CSI strategy cancels the signal mismatch that is caused by up to the Lth-order nonstationary effects and makes two test signals nearly identical.

To study the constancy of the offset, we set the signal to 0 in (26) and take the average of the real offset during the time windows of the second signal as

$$\alpha' = \frac{\alpha}{N_s} \sum_{j \in \Lambda}^{2N_s - 1} [1 + e(t+j)]\, g(t). \tag{33}$$

The difference between the averaged offset and the nominal offset is

$$\begin{aligned} N_2(t) &= \alpha' - \alpha \\ &= \frac{\alpha}{N_s} \sum_{j \in \Lambda}^{2N_s - 1} e(t+j) g(t). \end{aligned} \tag{34}$$

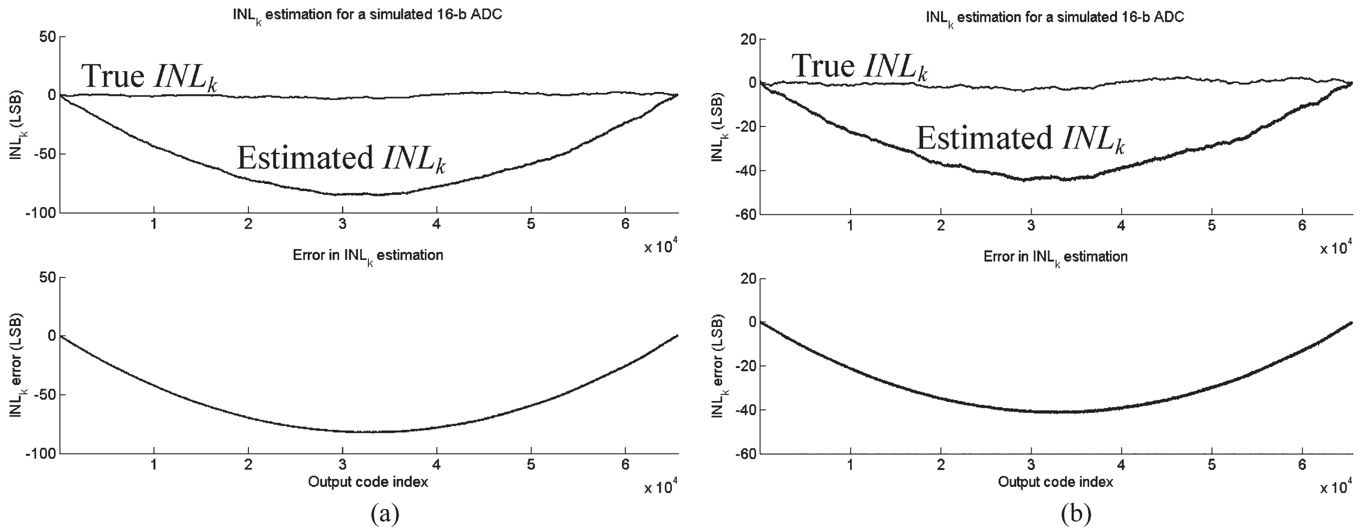

Fig. 3. INL$_k$ estimation. (a) $\alpha = 0.5\%$, 100-ppm drifting. (b) $\alpha = 1\%$, 100-ppm drifting.

Although $e(t)$ is unknown, its effect on the offset is attenuated by approximately $2N_s = 2 \cdot 2^L$ times if the Lth-level CSI is used, since each triangle only experiences a small, i.e., $1/(2N_s)$, portion of the total error. Assuming that each signal consists of $N_s = 32$ triangles and that the signal source has 1000 ppm of dominantly linear drifting error in its reference voltage during a test, it will introduce a relative error of about 16 ppm in the offset. Based on (18) and the discussion thereafter, this will introduce about 2 ppm error in ADC linearity testing, which is much smaller than one least significant bit (LSB) at the 16-bit resolution level (16 ppm). In reality, most of the existing testing circuitry can maintain better than 1000-ppm stability during a test time of several minutes or shorter. Therefore, with CSI, the offset can be sufficiently maintained constant under a changing environment.

Based on the discussions above, we can see that the CSI strategy can help generate identical test signals and a constant offset—two critical components that the SEIR algorithm requires—under a nonstationary environment. Some conclusions are summarized as follows.

1) Two interleaved periodical triangle signals are equivalent to two unfolded ramp signals with the same nonlinearity, i.e., if the original triangle signals are of the same shape.
2) Offset values between unfolded ramps are constant, if interleaved triangle signals are shifted from each other by a constant value.
3) Identical test signals can be generated by CSI. With the Lth-level CSI, effects of environmental nonstationarity on unfolded ramps can be cancelled to the Lth order.
4) A constant offset can be achieved with CSI. With the Lth-level interleaving, offset errors that are introduced by a changing environment can be reduced by about 2^L times.
5) By using the SEIR algorithm and Lth-level CSI, the residue nonstationary error is limited to be of $(L+1)$th or higher order and in a given bound when an appropriate L is picked, if the system can be described by a well-behaved low-order function.

V. Simulation and Experimental Results

Simulations and experiments were run to validate the conclusions that were made earlier. They are all in agreement with the analysis on the CSI strategy and support its effectiveness.

A. Simulation Results

The ADC under test was modeled by a 16-bit flash structure with a resistance mismatch in the simulation. The SEIR test algorithm is not sensitive to the ADC architecture. We choose the flash structure because it has a large number of independent error sources, which we can use to validate the performance of the proposed method under challenging situations. To save on simulation time, the number of average samples per code was set to 8, whereas it could take more than 50 samples per code in real production test applications for high-precision ADCs. In the simulation, the additive noise at the ADC input had a standard deviation of 0.5 LSB. The input signals were composed of triangular waves of seven-bit linearity. Sixteen sinusoidal basis functions were used in the SEIR algorithm to identify the input nonlinearity.

First, we checked the correctness of (16). We chose $N_s = 8$. The reference voltage had 100-ppm linear drifting during the test and was multiplied to the interleaved signal. To have a visible effect of the nonconstant offset, the second signal was generated after the first signal was completed. This means that $\Lambda = \{8, 9, 10, \ldots, 15\}$. The INL$_k$ estimation results, using the SEIR method for the same ADC, are plotted in Fig. 3 for offset values of 0.5% and 1% of the total ADC input range, respectively. We can see that the INL$_k$ estimation error (Fig. 3(a) and (b), bottom part) has a "bell" shape and that the maximum error happens at the middle of the ADC input range. The maximum error is inversely proportional to offset α and is reduced by half when α is doubled. All of these observations are in agreement with (18). Calculations show that the equivalent error in the offset is approximately a linear drift of 50 ppm, which is in agreement with the simulation setup, since the 100-ppm drift was applied to two test signals.

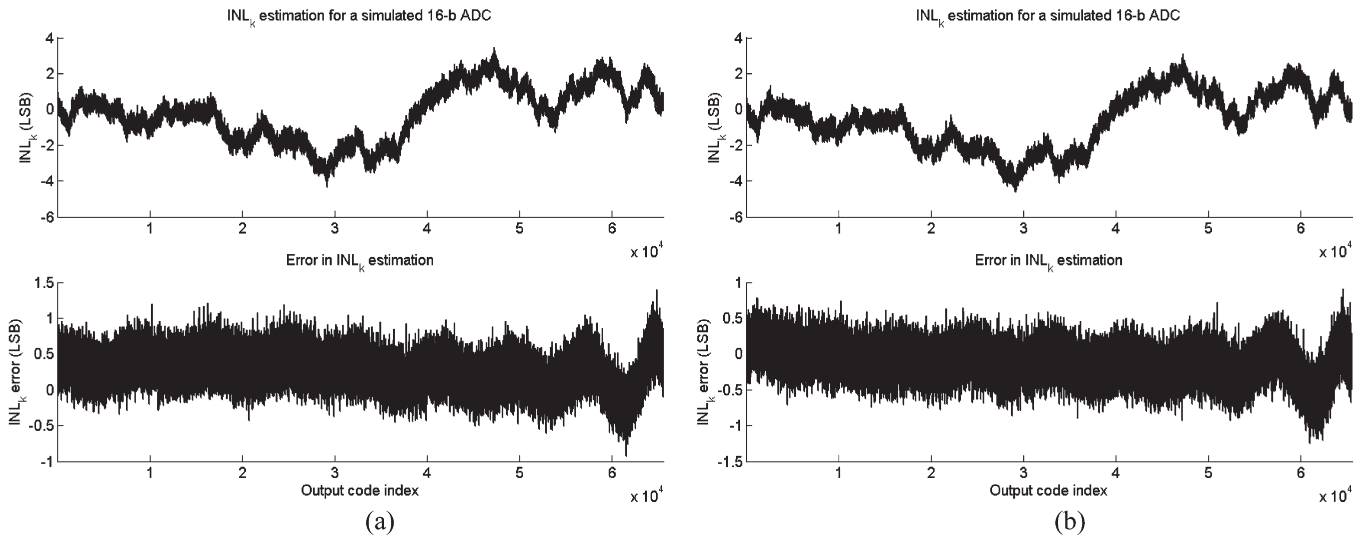

Fig. 4. INL$_k$ estimation. (a) $\alpha = 0.5\%$, 100-ppm drifting. (b) $\alpha = 0.5\%$, 500-ppm drifting.

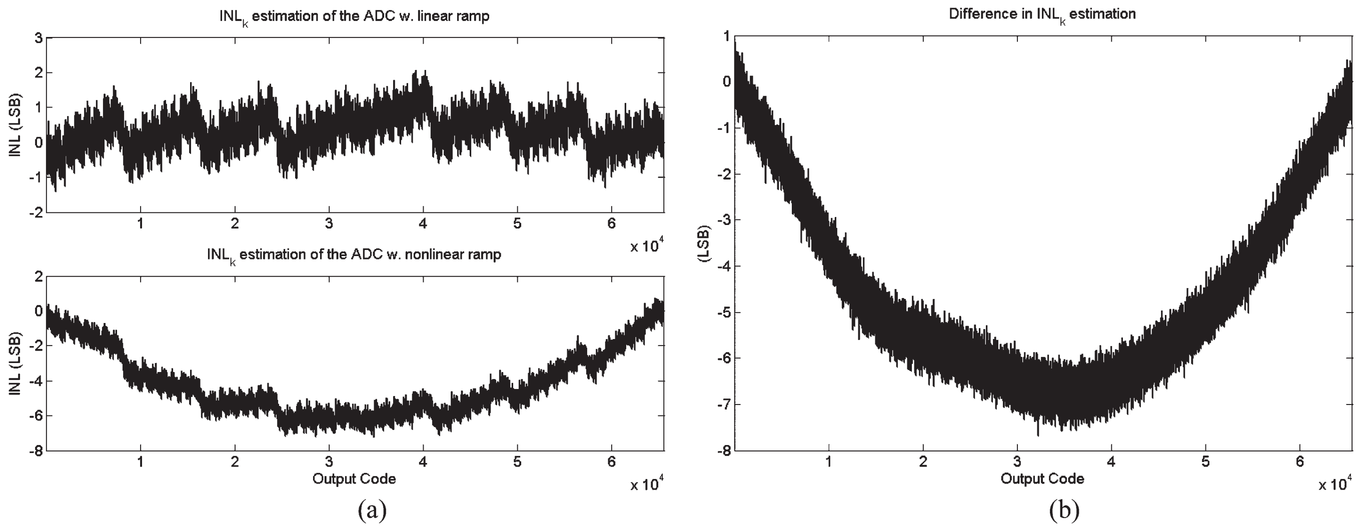

Fig. 5. INL$_k$ measurement. (a) Top: Test results with a 20-bit linear signal. Bottom: Test results with seven-bit linear signals $\alpha = 0.1\%$. (b) Difference between results.

Then, we checked the effectiveness of CSI under the same test condition. The offset between two signals was 0.5% of the overall ADC input range. The third-level CSI as in Fig. 2(b) was used. The top part of Fig. 4(a) contains two curves: the true INL$_k$ and the INL$_k$ estimated using SEIR and CSI. The two curves match very well. The difference between them can hardly be seen and is plotted on the bottom part of Fig. 4(a). The estimation error is dramatically reduced from more than 80 LSBs in Fig. 3(a) to 1 LSB. The residue errors mainly come from the noise effect due to the small number of samples. We run another simulation with 500-ppm linear drift to represent a worse test environment, and the results are shown in Fig. 4(b). The estimation errors remain at about the same level, which are not increasing, even with bigger reference voltage drifting, and are mainly due to noise.

B. Experimental Results

Commercially available ADCs were tested to verify the performance of the proposed method, which combines the SEIR algorithm and the CSI strategy. The device under test was a laser-trimmed 16-bit successive-approximation register ADC with typical INL of about 1.5 LSBs, which is a known test challenge. The INL$_k$ of the ADC was tested by both the traditional method and the proposed method, with 32 samples per code on the average. The proposed method used ten basis functions in input identification.

The first experiment was done without carefully arranging the two signals, simply generating the second signal after the first one. The offset was set as 0.1%. To do a comparison, the ADC was first tested by using the conventional histogram method with a 20-bit linear signal, and the tested INL$_k$ is plotted on the top part of Fig. 5(a). This INL$_k$ is used as a reference to determine the performance of the proposed test. The SEIR algorithm tested the ADC with the seven-bit linear signals, and the tested INL$_k$ is plotted on the bottom part of Fig. 5(a). The difference between the two tested INL$_k$ is plotted in Fig. 5(b). As can be seen from the plot, SEIR test results have errors shaped like a "bell" and a maximum value

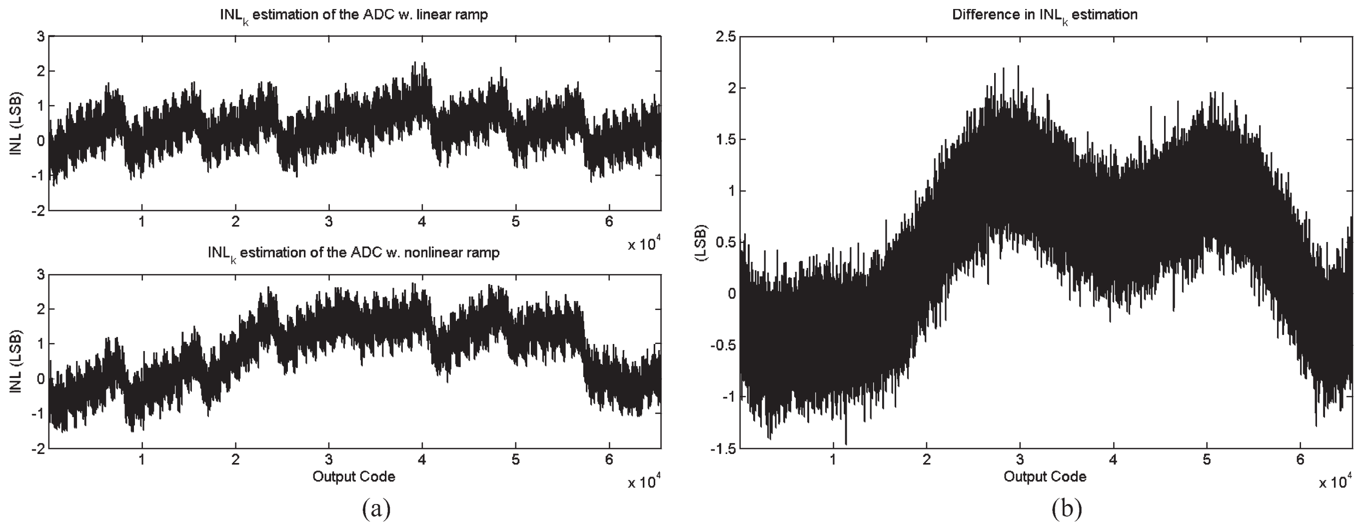

Fig. 6. INL_k measurement. (a) Top: Test results with a 20-bit linear signal. Bottom: Test results with seven-bit linear signals $\alpha = 0.1\%$. (b) Difference between results.

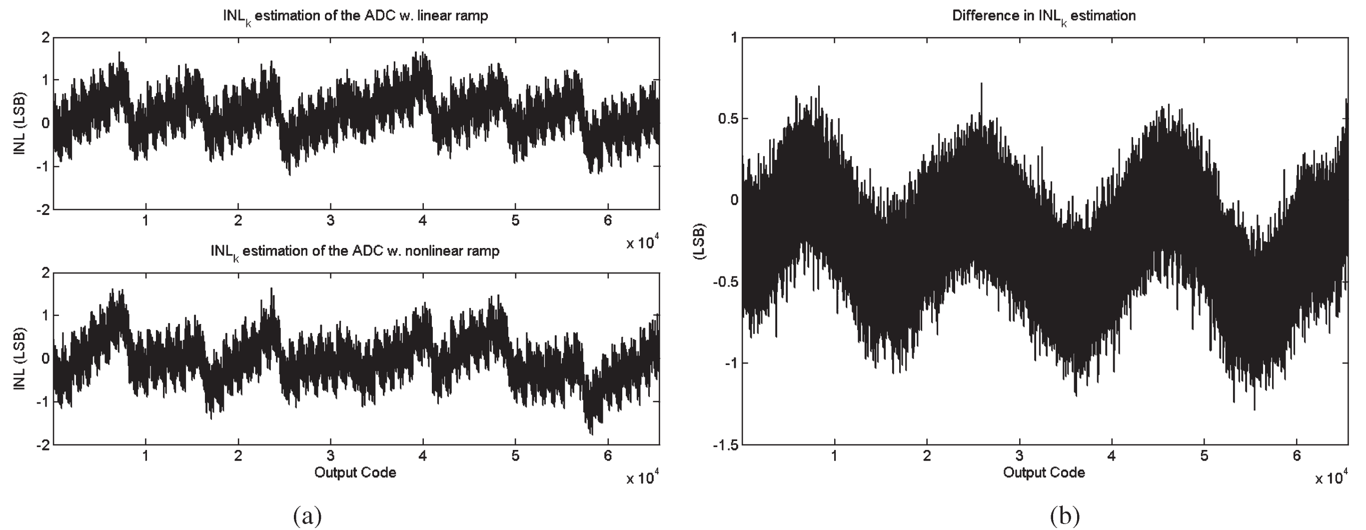

Fig. 7. INL_k measurement. (a) Top: Test results with a 20-bit linear signal. Bottom: Test results with seven-bit linear signals $\alpha = 0.05\%$. (b) Difference between results.

of more than seven LSBs. This error is expected because there is nonstationarity existing in the test system.

Next, the ADC was tested with an improved arrangement of signals, whereas all the other setups are unchanged. Instead of letting the second signal go after the first one, the triangular waves of the two signals were evenly interleaved, which means that $\Lambda = \{1, 3, 5, \ldots\}$. Fig. 6 gives the results. The INL_k that was tested with a 20-bit linear signal is used as a benchmark and plotted on the top part of Fig. 6(a). The SEIR result is plotted on the bottom part. This time, test errors of the SEIR algorithm with seven-bit linear signals were reduced to about the two-LSB level and did not have a "bell" shape. This means that two evenly interleaving signals can reduce the nonstationary effects, but it is still not good enough for testing the 16-bit part.

Finally, the CSI method that was developed in this paper was used. This time, the dc offset was set to a smaller value, i.e., 0.05%, which may lead to larger test errors, as compared to the 0.1% offset. N_s was set to 32, and $\Lambda = \{1, 2, 4, 7, 8, 11, 13, 14, 16, 19, 21, 22, 25, 26, 28, 31, 32, 35, 37, 38, 41, 42, 44, 47, 49, 50, 52, 55, 56, 59, 61, 62\}$ was used to cancel up to the fifth-order reference drifting errors. The test results are plotted in Fig. 7. As our old convention, the ADC was first tested by using a highly linear signal with the results plotted on the top part of Fig. 7(a). The corresponding measured INL is 1.66 LSBs. Then, histogram data were obtained with the seven-bit linear input signals and analyzed using the SEIR algorithm with ten basis functions. The estimated INL_k is plotted on the bottom part of Fig. 7(a). The estimated INL with nonlinear signals is 1.77 LSBs. We can see that when using the proposed CSI method, the INL_k that is estimated using linear and nonlinear signals are really close. The difference between the INL_k estimates is shown in Fig. 7(b), and they are mostly less than one LSB. This means that the proposed approach can effectively make the offset between two signals constant in nonstationary environments and is an acceptable solution as far as 16-bit converters are concerned.

In Fig. 7(b), the difference between the testing results mainly come from two sources. First, the high-frequency errors were

introduced by the additive noise, which gives a band of about ±0.5 LSB. Second, the low-frequency error component was contributed by the residue of nonconstant errors in the offset, which are not completely cancelled by the signal arrangement approach. Based on (16), this kind of error is inversely proportional to the offset amount. Since the offset value is only 0.05% in the last test, we can increase the offset amount to further reduce test errors to well below the noise error level.

The simulation and experimental results that are presented in this section show that combining the SEIR algorithm with the CSI technique can eliminate the effect of test environment nonstationarity and give out accurate linearity test results for high-resolution ADCs.

VI. Conclusion

In this paper, a test strategy that can eliminate the effects of input nonlinearity and environment nonstability errors on the test results of high-resolution ADCs has been introduced. Using the SEIR algorithm along with the proposed CSI technique, 16-bit ADCs were accurately tested using input signals with only seven-bit linearity in an environment with more than 100-ppm nonstationarity in the test window. This has been a promising strategy for solving test problems that are very challenging, such as full characterization of ADC linearity at 16-bit or higher resolution levels, since both the signal linearity and environment stability are no longer required to be better than ADC specifications. This strategy can also help control the cost of existing test solutions by allowing the use of cheap instruments. Furthermore, the strategy has the potential to be used in an on-chip test environment, where accurate test devices may not be available.

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