A Simple and Accurate Method to Predict Offset Voltage in Dynamic Comparators

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***Abstract*—In a dynamic comparator, it's always challenging to analytically predict the input offset voltage due to the existence of the internal positive feedback and transient process. In this paper, a simple method is presented to accurately estimate input offset voltages caused by process variations in dynamic comparators. The "Lewis-Gray" comparator implemented in TSMC0.25µm process is applied as an example to verify the effectiveness of the analytical method. Based on the SPICE level 1 model, the method shows good agreements with Monte Carlo transient simulation based on the sophisticated BSIM3v3 model. The analytical results allow the circuit designers to fully explore the tradeoffs in comparator design, such as offset voltage, area and speed. To illustrate the potential, the analytical method was used to re-size the "Lewis-Gray" structure to reduce its random offset while maintaining a constant total area. After the optimization, input offset voltage has been reduced by 41% compared with its original sizing.**

I. INTRODUCTION

Comparators have a crucial influence on the overall performance in high-speed analog-to-digital converters (ADCs) [1]. The comparator's accuracy, which is often defined by its input offset voltage, is essential for high performance ADCs. Dynamic comparators are widely used in the high speed ADCs due to its low power consumption and fast speed. However, there is a lack of thorough and accurate analysis in the literature on how to evaluate the input offset voltages analytically. Although there exist various offset cancellation circuits and digital calibration techniques [2] [3], to apply such additional circuits to cancel offset voltages increases the power consumption, silicon area and lowers the overall speed. When the transistor feature size is scaled down, random offsets impact the yield of ADCs more severely [4]. Different from the offset caused by mismatch from the gradient effect, random offset cannot be relieved by any layout strategy [5]. In order to achieve an optimum dynamic comparator design, it is essential to have analytical methods to accurately predict offset voltages, especially random offset voltages.

When a traditional comparator is built by an operational amplifier, the calculation of offset voltage is straightforward since the operation regions of all transistors are well defined.

The previous authors try to analyze the input offset voltage in a dynamic comparator the same way as in the traditional comparator [6][7][8]. However, the authors fail to clearly state how to accurately determine trans-conductance g_m and output conductance g_o of the transistors. As a matter of fact, in a dynamic comparator with an internal positive feedback, the previous method is not applicable since g_m and g_o of any transistor are time dependent and not well defined.

To overcome the difficulties in determining the operation regions and bias conditions of transistors in a dynamic comparator when the mismatch exists, we propose a balanced method to calculate the input offset voltage. In this method, a voltage equal to the input offset voltage is virtually applied to one of the inputs of the comparator to cancel the mismatch effects and make the comparator with mismatch to reach a balanced status. Under this balanced condition, the currents in the two branches are symmetric at any time. So the bias voltage and current for any transistor in the comparator are ready to be solved at any time point. The input referred offset voltage can thus be derived analytically.

In section II, the procedure to derive the input offset voltage is demonstrated by using the "Lewis-Gray" dynamic comparator as an example. In section III, our analytical results are compared with the more accurate but time consuming Monte Carlo transient simulations. A good agreement is reached. In section IV, the analytical results are applied to reduce random offset voltage by 41% in the "Lewis-Gary" comparator by re-sizing the transistors while maintaining a constant total area.

II. RANDOM OFFSET VOLTAGE IN A DYNAMIC COMPARATOR

A fully differential dynamic comparator reaches a balanced state if no mismatch exists in the circuit. As shown in Fig. 1, balanced state means that currents I_1 and I_2 in both branches are identical at all the time during the transient process and $V_{out+}=V_{out-}$. The balanced state can be described by a space Φ_b comprised of power supplies, external bias voltage V_{latch} and comparison threshold or reference voltages V_{ref+} and V_{ref-} and transistor node voltages, which is written as

Φ_b = {V_{DD}, V_{latch}, V_{ref+}, V_{ref-}, V_{s5} or V_{s6}, V_{d5} or V_{d6}, V_{out+} or V_{out-}}, in which the subscript s and d mean source and drain voltage of transistor, respectively. When some mismatch occurs, the circuit will lose its balance so $I_1 \neq I_2$. A voltage ΔV_{in} can be applied to compensate the mismatch effect and make I_1 equal to I_2. This compensation voltage ΔV_{in} is the input offset voltage. The new balanced state Φ_{bn} is the same as Φ_b since under the new balanced condition, mismatch and ΔV_{in} is a small disturbance that won't change the bias condition of the comparator.

In order to calculate ΔV_{in}, node voltages at balanced state Φ_b need to be found and then are treated as the desired state when ΔV_{in} is applied to compensate mismatch. The chosen time point to calculate Φ_b is not important since under balanced condition node voltages for both branches are always symmetrical all the time. In this paper, the time point when the control signal V_{latch} reaches V_{DD} is chosen. Therefore, the operation regions of all of the transistors are well defined. Transistors of M_1-M_4 connecting to the input and reference voltages are in the triode region and act like voltage controlled resistors. M_{10} and M_{11} have equal drain and gate voltage, which makes them work at saturation region. M_7 and M_8 work as switches embedded in cross-coupled inverter pairs including M_5M_{10} and M_6M_{11}. They are turned on during comparison stage and working in the triode region because of its high gate voltage $V_{g7,8} = V_{DD}$. The drain voltage of M_5 and M_6 is pulled up closed to V_{out+} or V_{out-} and works in saturation because switches M_7 and M_8 are in the triode region. M_9 and M_{12} are both turned off because control signal V_{latch} is V_{DD}, which indicates that mismatch effects in M_9 and M_{12} is negligible. If time point for Φ_b is chosen when V_{latch} is half of the V_{DD}, the operation region of M_7 and M_8 becomes unclear. Thus their operation regions need to be assumed first, and then verified by solving each node voltages under the balanced condition. Iteration may be necessary to find the operation region of M_7 and M_8. Once the operation regions for each transistor is known, combining with known power supply voltages, input voltages and process parameters, each node voltage in the dynamic comparator at balanced state can be readily solved.

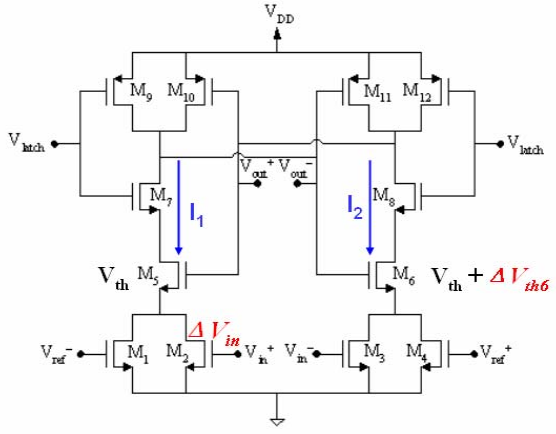

Figure 1. "Lewis-Gray" structure

In this paper, mismatch in current factor $\beta=\mu C_{ox}W/L$ and threshold voltage V_{th} are assumed to be the dominant offset factors caused by process variation. Since β is the product of μ, C_{ox} and W/L, the combined variation can be regarded as the only variation in mobility μ for the convenience of calculation. First mismatch between M_5 and M_6 is considered and other pairs are assumed to be perfectly matched. At the input a compensation voltage $\Delta V_{in} = V_{os\_M5M6}$ will be required to make the comparator work at balanced condition Φ_b. The offset voltage is calculated as

$$V_{os\_M5M6} = \frac{(\mu_n+\mu_{5R})(W_5/W_1)(V_{out+}-V_{s5}-V_{tn}-V_{t5R})^2}{2\cdot\mu_n\cdot V_{s5}} - \frac{(\mu_n+\mu_{6R})(W_6/W_1)(V_{out-}-V_{s6}-V_{tn}-V_{t6R})^2}{2\cdot\mu_n\cdot V_{s6}} \quad (1)$$

where V_{out+}, V_{out-}, V_{s5}, V_{s6} are solved node voltages at balanced state Φ_b. μ_n and V_{tn} are the nominal values of NMOS mobility and threshold voltage, respectively. μ_{5R} and μ_{6R} are the random mobility variations for M_5 and M_6. V_{t5R} and V_{t6R} are the random variations for threshold voltages of M_5 and M_6, respectively.

If variables μ and threshold voltage V_{th} are assumed to be two uncorrelated random variables with Gaussian distribution, input random offset voltage caused by mismatch between M_5 and M_6 can be derived from the variance of (1).

$$\sigma^2_{V_{os\_M5M6}} = \frac{(V_{out+}-V_{s5}-V_{tn})^2\sigma^2_{Vt5R}+(V_{out-}-V_{s6}-V_{tn})^2\sigma^2_{Vt6R}}{{V_{s5}}^2}\cdot(W_5/W_1)^2 + \frac{(V_{out+}-V_{s5}-V_{tn})^4\sigma^2_{\mu5R/\mu n}+(V_{out-}-V_{s6}-V_{tn})^4\sigma^2_{\mu6R/\mu n}}{4{V_{s5}}^2}\cdot(W_6/W_1)^2 \quad (2)$$

Similarly, input random offset voltages caused by mismatch of the other pairs can also be found as follows:

$$\sigma^2_{V_{os\_M1M4}} = \sigma^2_{V_{t1R}}+\sigma^2_{V_{t4R}} + (V_{ref+}-V_{tn})^2\sigma^2_{\mu_{4R}/\mu_n}+(V_{ref-}-V_{tn})^2\sigma^2_{\mu_{1R}/\mu_n} \quad (3)$$

$$\sigma^2_{V_{os\_M2M3}} = \sigma^2_{V_{t2R}}+\sigma^2_{V_{t3R}} + (V_{ref+}-V_{tn})^2\sigma^2_{\mu_{2R}/\mu_n}+(V_{ref-}-V_{tn})^2{\sigma_{\mu_{3R}/\mu_n}}^2 \quad (4)$$

$$\sigma^2_{V_{os\_M10M11}} = \frac{(V_{dd}-V_{out+}-V_{tp})^2}{9\cdot{V_{s5}}^2}\sigma^2_{V_{t10R}}+\frac{(V_{dd}-V_{out+}-V_{tp})^2}{9\cdot{V_{s6}}^2}\sigma^2_{V_{t11R}} + \frac{(V_{dd}-V_{out+}-V_{tp})^4}{9\cdot4{V_{s5}}^2}\sigma^2_{\mu_{10R}/\mu_p}+\frac{(V_{dd}-V_{out+}-V_{tp})^4}{9\cdot4{V_{s6}}^2}\sigma^2_{\mu_{11R}/\mu_p} \quad (5)$$

$$\sigma^2_{Vos\_M7M8} = (\frac{W_7}{W_2}\cdot\frac{V_{ds7}}{V_{s5}})^2\sigma^2_{V_{t7R}}+(\frac{W_8}{W_2}\cdot\frac{V_{ds8}}{V_{s5}})^2\sigma^2_{V_{t8R}} + (\frac{W_7}{W_2}\cdot\frac{V_{ds7}}{V_{s5}})^2(V_{latch}-V_{d5}-V_{tn}-\frac{V_{ds7}}{2})^2\sigma^2_{\mu_{7R}/\mu_n} + (\frac{W_8}{W_2}\cdot\frac{V_{ds8}}{V_{s5}})^2(V_{latch}-V_{d6}-V_{tn}-\frac{V_{ds8}}{2})^2\sigma^2_{\mu_{8R}/\mu_n} \quad (6)$$

where ${\sigma_{VtiR}}^2$, ${\sigma_{\mu iR/\mu n}}^2$ and ${\sigma_{\mu iR/\mu p}}^2$ (i=1,2..11) characterizes random mismatch in threshold voltage and mobility in NMOS and PMOS transistors, which can be modeled as follows[4],

$$\sigma^2_{V_{tR}} = \frac{A^2_{V_t}}{W \cdot L} + S^2_{V_{T0}} D^2 \quad (7)$$

$$\sigma^2_{\mu_R/\mu_n} = \frac{A_\mu{}^2}{W \cdot L} + S_\mu{}^2 D^2 \quad (8)$$

where W and L are the width and length of transistor pair. D is the distance on chip between the matching transistors, which will be neglected because of its minor contribution to the overall mismatch.

If the random mismatches in each pair are uncorrelated or nearly uncorrelated, the overall random offset voltage σ_{Vos} in the dynamic comparator can be described as follows:

$$\sigma_{Vos} = \sqrt{\sigma^2_{Vos\_M5M6} + \sigma^2_{Vos\_M1M4} + \sigma^2_{Vos\_M2M3} + \sigma^2_{Vos\_M7M8} + \sigma^2_{Vos\_M10M11}} \quad (9)$$

Random offset resulting from mismatch between M_9 and M_{12} are neglected in the calculation, because they work as switch during the reset state to pull up differential output to V_{DD}, and then are turned off during the comparison stage.

From (2) to (6), it can be concluded that: 1) Random offset voltages caused by mismatch in transistors pairs of M_1 and M_4, M_2 and M_3 can be reduced by increasing the size of those transistors, because $\sigma_{VtR}{}^2$ and $\sigma_{\mu R/\mu N}{}^2$ are inversely proportional to the product of W and L; 2) Random offset voltages caused by mismatch in transistors pairs of M_5 and M_6, M_7 and M_8 can not be guaranteed to be reduced when the size of the transistors are increased since the widths also appear in the numerator of the (2) and (6). A particular aspect ratio W/L can be found to make an optimum tradeoff between random offset voltage and transistor size denoted by the product of W and L.

III. An Numerical Example and Monte Carlo Simulation

The "Lewis-Gray" comparator is implemented in a TSMC 0.25µm process. The key values are listed in Table I. The channel length L=0.45µm is chosen for all the transistors for matching purpose. First, all node voltages are solved when no mismatch is presented to determine ideal state Φ_b at balanced condition. In this example, it can be calculated that: $V_{out+}=V_{out-}=0.601V$, $V_{d5}=V_{d6}=0.585V$, $V_{s5}=V_{s6}=0.0089V$. Then the calculated node voltages are applied to equation (2)-(6) to find numerical value for random offset caused by mismatch due to process variation in each pair. A_{vt} and A_μ in σ_{VtR} and $\sigma_{\mu R/\mu n}$ are process dependent parameters, whose values for different processes are listed as a reference in Table II [4].

Monte Carlo transient simulation is performed by using BSIM3v3 model. In this model, the mobility μ_n and threshold voltage V_{th} are defined as Gaussian distributed variables with a standard deviation modeled by equation (7) and (8). One hundred iterations are done for each pair while assuming no mismatch exists in other pair to find out σ_{Vos_M1M4}, σ_{Vos_M2M3}, σ_{Vos_M5M6}, σ_{Vos_M7M8}, σ_{Vos_M10M11} and σ_{Vos_M9M10}. In Fig.2, the random offset voltage calculated by the analytical method from section II shows a good agreement with the Monte Carlo simulation results.

IV. One Application of the Random Offset Analytical Model

Without any offset cancellation technique, a dynamic comparator will not easily achieve input offset voltage less than several tens of milli-volts. Mismatch caused by random variations cannot be relieved from any layout strategy. Without increasing the total area of the comparator, the analytical model in (2)-(6) can be utilized to effectively reduce the random offset voltage by proper sizing.

The following procedures are applied to find the proper sizes to achieve small random offset voltage given a fixed total area.

1) Based on the analytical results in (2)-(6), the input random offset voltage due to each transistor pair can be calculated. Then all the transistor pairs are divided into several

TABLE I. Key Values for the Dynamic Comparator

Process	TSMC 0.25µm
Power supply	Vdd=1.5V, Vss=0V
Transistor sizing	(W/L)1,2,3,4=(1.5u/0.45u)x4
	(W/L)5,6,7,8=(3.5u/0.45u)x4
	(W/L)10,11=(1.5u/0.45u)x4
Vref	Vref+=1.6V, Vref-=1.2V
Clock signal Vlatch	High=1.5V;Low=0V
	Rise and fall time = 10ps
	Pulse width=20ns;Period=100n
Switch (PMOS)	(W/L)9,12=1.5u/0.45u

TABLE II. Mismatch Parameter for Several CMOS Technologies

Technology	Type	A_{vt}(mV·µm)	A_β(%·µm)
2.5 µm	NMOS	30	2.3
	PMOS	35	3.2
1.2 µm	NMOS	21	1.8
	PMOS	25	4.2
0.7 µm	NMOS	13	1.9
	PMOS	22	2.8
0.5 µm	NMOS	11	1.8
	PMOS	13	2.3
0.35 µm	NMOS	9	1.9
	PMOS	9	2.25
0.25 µm	NMOS	6	1.85
	PMOS	6	1.85

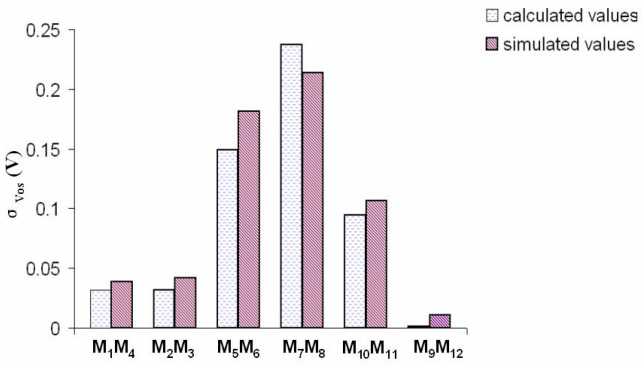

Figure 2. Comparison of input random offset voltage between analytical results and Monte Carlo simulation for each pair

groups following the rule that in each group there contains both a critical matching pair and uncritical pairs. All of the groups have the same silicon area.

2) Consider the mismatch in one group and assume there is no mismatch in the other groups. Based on the conclusion from section II, a minimum random offset voltage can be found by properly adjusting the size of the transistor pairs depending on their contributions to the offset voltages. Apply the same procedure to the remaining groups to achieve minimum random offset in each group.

Based on the calculated offset voltage from each transistor pair, six pairs in the dynamic comparator in Fig.1 are divided into two groups. Group 1 is composed of bottom four uncritical matching transistor pairs M_1-M_4 and critical matching transistor pairs M_7M_8. Group 2 includes the four uncritical matching PMOS transistors M_9-M_{12} and critical matching NMOS pairs M_5M_6.

First the lengths of all the transistors are fixed as 0.45µm for layout matching purpose in TSMC0.25µm process. First group 1 is optimized. The area margin is moved from M_1-M_4 to M_7M_8 by increasing width of M_7M_8 at a step size 0.5um while the total area in the group is maintained as a constant. The simulated random offset voltage versus ΔW in M_7M_8 is shown in Fig. 3. It is shown that when ΔW_ M_7M_8 is equal to 2µm, which means the widths of M_7M_8 are equal to 5.5µm and widths of M_1-M_4 are 0.5µm. The random offset voltage reaches the minimum value 78.3mV. The similar area allocation procedure is applied to group 2. The simulated random offset versus ΔW of M_5M_6 is shown in Fig. 4. Finally, the aspect ratios $(W/L)_{1,2,3,4}$=0.5/0.45, $(W/L)_{7,8}$=5.5/0.45, $(W/L)_{5,6}$=2.5/0.45, $(W/L)_{9,10,11,12}$=2/0.45 are determined.

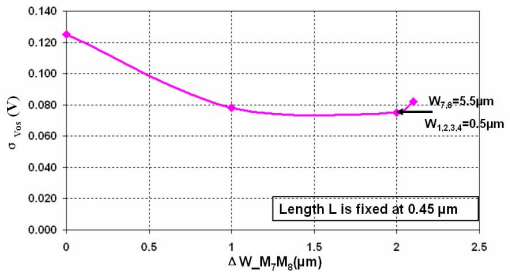

Figure 3. Random offset vs. ΔW of matching critical pair M_7M_8

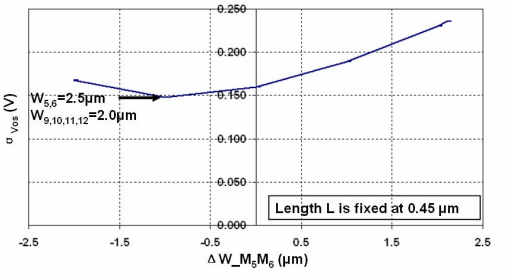

Figure 4. Random offset vs. ΔW of matching critical pair M_5M_6

After this optimization, Monte Carlo simulation is applied with mismatch presented in all the pairs, and the overall random offset voltage is 150 mV, which is reduced by 41% compared with 254 mV in the original sizing.

V. CONCLUSION

A simple and accurate way called the balanced method to predict random offset in dynamic comparators using internal positive feedback has been presented. The method solves the problem that the operation regions and bias conditions of transistors in dynamic comparators with fast transient process are difficult to be accurately determined. Analytical expressions for random offset voltage caused by mismatch in each pair in "Lewis-Gray" structure are derived as an example. The analytical results have very good agreement with Monte Carlo transient simulations. One application of the method to optimize the comparator design between offset and area is listed to demonstrate its effectiveness.

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