Testing of Precision DAC Using Low-Resolution ADC With Wobbling

Le Jin, *Member, IEEE*, Hosam Haggag, Randall L. Geiger, *Fellow, IEEE*, and Degang Chen, *Senior Member, IEEE*

***Abstract*—Testing of high-resolution, digital-to-analog converters (DACs) with gigahertz clock rates is a challenging problem. The bottleneck is fast and accurate output measurement. This paper presents a novel high-performance DAC testing approach that uses a flash analog-to-digital converter (ADC) to achieve high-speed data acquisition, adopts the wobbling technique to provide a sufficient resolution, and processes the data with a sophisticated algorithm to guarantee high test accuracy. Simulation results show that, by using a 6-bit ADC and wobbling, the static linearity of 14-bit DACs can be tested to better than 1-LSB accuracy. The experimental results that are included in the paper also affirm the performance of the algorithm. This method provides a solution to both the production and on-chip testing problems of high-performance DACs.**

***Index Terms*—Analog-to-digital converter (ADC), digital-to-analog converter (DAC), precision test, wobbling.**

I. Introduction

BECAUSE of the explosive growth in the consumer-electronics market during the past few decades, the integrated circuit (IC) industry is shifting from personal computer-centric to consumer-electronics-centric. Not only digital but also mixed-signal and RF functions are required to be integrated in a single device, such as cell phones, personal digital assistants, portable multimedia players, digital cameras, and video recorders. System-on-a-chip (SoC) design and built-in self-test (BIST) for mixed-signal circuits are two enabling technologies that are behind the integration of these functions and are of great interest to the industry and academia. While digital testing has been studied for a long time, testing of analog and mixed-signal (AMS) circuits is still in its development stage. Existing solutions for testing AMS circuits have several major problems. First, the test cost is high. This has become a strategic problem to many large circuit manufacturers and has led to serious discussions. Second, it is more and more challenging to improve the test capability of existing methods to keep up with the performance of the fast-evolving mixed-signal products. Furthermore, there is a lack of effective methods for on-chip test of mixed-signal integrated systems. The International Technology Roadmap for Semiconductors (ITRS) identified mixed-signal testing as one of the most daunting SoC challenges [1].

The digital-to-analog converter (DAC) serves as the interface between the digital processing functions and analog signals. As the SoC design style is getting increasingly popular and as the requirements for high-quality AMS circuitries are continuously going up, the demand for high-performance DACs is rapidly growing. In addition, in the ITRS, is it indicated that "... digital-to-analog conversion performance becomes increasingly important as it opens the door to new high-volume but low-cost applications." The world's leading IC companies are manufacturing high-speed, high-resolution DACs for applications such as wireless communications and digital signal processing. Current state-of-the-art products have 16-bit resolutions and more than 500-MSPS update rates. The next-generation products with better performance are under development and will be on the market very soon. Along with the advancement in DAC performance, there are, consequently, new needs in DAC design and testing.

This paper is targeting at the high-performance DAC testing problem. Techniques such as dithering and wobbling have been adopted to improve test performance of analog-to-digital converters (ADCs) in terms of accuracy and stability (see [2] and its references). Wobbling has several advantages over dithering [2]. One of them is that it applies deterministic signals during testing, and the effect can be corrected during data processing. We exploited the idea of wobbling and extended it to DAC testing in this paper. We came up with a novel method of testing high-performance DACs using low-resolution ADCs with wobbling. A high-speed measurement is achieved with a flash ADC in our method, a sufficient resolution is provided by wobbling, and a high test accuracy is guaranteed by a proposed data processing algorithm. Because of the availability of very high-speed flash ADCs, this approach provides a practical solution to testing high-speed, high-resolution DACs.

II. Review of DAC Testing

Testing has important roles in the design, characterization, and production of an IC. An efficient testing method with high accuracy, short test time, and low cost is very appealing to manufacturers. This section provides background information on some common linearity tests that are applied to a DAC and limitations of the conventional test solutions.

A. Specifications of DACs

Integral nonlinearity (INL) and differential nonlinearity (DNL) are widely used in characterizing a DAC's static

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L. Jin is with National Semiconductor Corporation, Santa Clara, CA 95052 USA.

H. Haggag was with National Semiconductor Corporation, Santa Clara, CA 95052 USA.

R. L. Geiger and D. Chen are with the Department of Electrical and Computer Engineering, Iowa State University, Ames, IA 50011 USA.

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linearity. Various definitions for INL and DNL exist. We use the definition based on a fit line connecting a DAC's smallest and largest output voltages. By this definition, an n-bit DAC's INL at code k can be written as

$$\text{INL}_k = (N-1)\frac{v_k - v_0}{v_{N-1} - v_0} - k\,(\text{LSB}), \qquad k = 0, 1, \ldots, N-1 \tag{1}$$

where $N = 2^n$, and v_k is the output voltage that is associated with k. The unit LSB, which means least significant bit, is the averaged voltage increment

$$1\ \text{LSB} = \frac{v_{N-1} - v_0}{N-1}. \tag{2}$$

The expression for INL is

$$\text{INL} = \max_k \{|\text{INL}_k|\}. \tag{3}$$

Definitions of codewise and overall DNL are

$$\text{DNL}_k = (N-1)\frac{v_k - v_{k-1}}{v_{N-1} - v_0} - 1\,(\text{LSB}), \qquad k = 1 \ldots N-1 \tag{4}$$

$$\text{DNL} = \max_k \{|\text{DNL}_k|\}. \tag{5}$$

B. Existing DAC Testing Methods

There are many widely adopted methods existing for bench and production test of DACs. Static linearity and dynamic performance of medium and low-speed DACs can be measured by using sigma–delta or dual-slope ADCs [3]. These types of ADCs have very high accuracy, but their speed is inherently limited by their architectures. Dynamic test of high-speed communication DACs is usually done by using spectrum analyzers. The spectrum analyzers' dynamic range is affected by their nonlinearity and distortion and is usually less than 90 dB or lower for some specific measurements. Notch filters are sometimes used to remove the dominant fundamental component to reduce the nonlinearity and distortion. Furthermore, spectrum analyzers need a long time to generate a complete spectrum over a wide frequency range with a small resolution bandwidth, and they do not provide any time-domain information about the measured signal.

Other DAC testing approaches have been studied and reported. An on-chip pass-or-fail testing approach for DACs using accurate reference voltages and a precision gain amplifier was presented by Arabi *et al.* [4]. An approach of using a DAC's static nonlinearity to characterize its intermodulation errors was introduced by Vargha *et al.* [5]. This approach is useful if the intermodulation errors are mainly from static nonlinearities, which is true at low frequencies. Rafeeque and Vasudevan [6] proposed an improved BIST scheme for DACs using an accurate sample-and-subtract circuit, a linear voltage-controlled oscillator, and a stable clock counter. An overall review of existing BIST approaches for DACs can also be found in [6].

In spite of these efforts, testing of high-speed precision DACs remains an open problem because it puts stringent requirements on the testing instruments. Linearity and stability of measurement devices should be better than the resolution of a DAC under test. It is also desirable to have a test structure that runs as fast as the DAC under test to conduct real-time testing and reduce the total test time. It is nontrivial to manufacture sufficiently fast and accurate instruments for testing the current and future high-performance DACs. The problem of on-chip DAC testing is also of interest and is still open. Calibration techniques can significantly improve a DAC's performance [7]. For effective calibration, an accurate characterization of the DAC is needed and is often times carried out by using precision instruments such as off-chip high-resolution ADCs [8], [9]. If a highly accurate and stable testing circuitry can be built on-chip, it will enable integrated self-calibration for DACs in an SoC design.

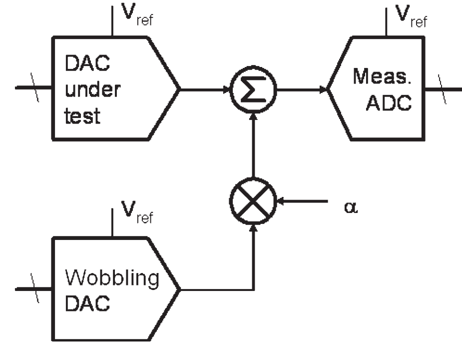


Fig. 1. Block diagram of the proposed method.

III. Precision DAC Testing Using Low-Resolution ADCs With Wobbling

This paper proposes a DAC testing approach with two goals: short test time and high accuracy. Flash ADCs have the fastest conversion rate among the data acquisition devices, so that it is used in our approach to quantize the output voltage of high-speed DACs. However, flash ADCs' resolutions are usually less than 8 bit because of their architecture limitation. The limitation of a low-resolution ADC is that it will introduce large quantization errors and that its transition levels are not accurate. A wobbling technique is developed in our paper to increase the resolution of the test, while the final accuracy of the test result will be guaranteed by an effective data processing algorithm that is applied to measurement results.

A. Test Setup and Data Capture

The proposed strategy uses a low-resolution measurement ADC (m-ADC) and a wobbling DAC (w-DAC) to test a high-performance DAC, which is usually called the device under test (DUT) (see the block diagram in Fig. 1). The output of the w-DAC will be scaled by a small factor α and will be added to the output of the DUT as a wobbling component. The wobbled output of the DUT will be quantized by the m-ADC.

In the test, the DUT will repeatedly generate a waveform of interest. During each period of the waveform, the w-DAC will provide a distinct but constant wobbling voltage. The m-ADC will quantize many periods of the waveform with

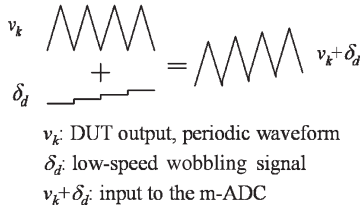


Fig. 2. DUT's output with wobbling.

different wobbling levels. Because of the different wobbling levels, the m-ADC's output codes that are associated with one output voltage of the DUT may slightly be different from one period to the next. See Fig. 2, where the DUT output waveform is triangular in this example.

The output codes of the m-ADC can be put into a 2-D structure, as shown in Table I, where N_w and N are the number of output levels of the w-DAC and the DUT, respectively. By assuming that a 6-bit ADC is used, the output code will be in the range 0–63. Each column in Table I is associated with one w-DAC input or, alternatively speaking, a wobbling level, and collected from one period of the waveform that is generated by the DUT, which is a ramp in this example. On the other hand, each row in the table comes from one DUT output voltage v_k with different wobbling levels. The scaling factor α is chosen so that the wobbled voltages that are associated with any one specific DUT output will cover at least one complete code bin of the m-ADC. A wobbling range of 3 LSB of the m-ADC is enough to guarantee this feature for a low-resolution ADC, for which the DNL is usually much less than 0.5 LSB. Given this property, the output codes of the m-ADC that are associated with any input codes to the DUT, which is a row in Table I, will always consist of at least three distinct codes. These output codes will be used to calibrate the m-ADC and to test the DUT.

B. DAC Test With Wobbling

Without wobbling, a DUT output voltage v_k will be quantized by the m-ADC as code j if $T_j < v_k <= T_{j+1}$ [see Fig. 3(a)]. T_j is the transition level of the m-ADC between code $j-1$ and j. Based on this output, we can only have a rough estimation of the DUT output as

$$\hat{v}_k = T_j = v_k + q_k \tag{6}$$

where q_k is the quantization error introduced by the m-ADC. Since the m-ADC's resolution is much lower than that of the DUT, q_k can be as large as hundreds of LSBs for the DUT. This is why low-resolution ADCs are not used to test precision DACs. In our approach, wobbling is used to increase the resolution and minimize the quantization error.

As in Fig. 2, the m-ADC will quantize many wobbled copies of the DUT output voltage $v_k + \delta_d$, where δ_d is the dth wobbling level. The associated output codes form a row in Table I. The quantized output may change as the wobbling voltage increases. At a specific wobbling level d_{kj}, the output code of the m-ADC changes from $j-1$ to j as the wobbled voltage changes from less than T_j to larger than T_j [see Fig. 3(b)]. In Fig. 3(b), we can derive a new estimate of the DUT output as

$$\hat{v}_{k,j} = T_j - \delta_{dkj} = v_k - e_k \tag{7}$$

where $\delta_{dkj} = d_{kj}/N_w - 1/2$ is the wobbling level. For linearity testing, the unit of the wobbling voltage does not affect the final accuracy, so we use their linearly code-dependent part and normalize it with N_w, and half is taken off for representing differential voltage wobbling. It is assumed in the discussion that the wobbled voltages that are associated with v_k are uniformly spaced over the whole wobbling range, which is a small interval around v_k. This is reasonable for a small scaling factor α because any nonideality in the w-DAC is dramatically scaled down and becomes negligible as compared to the errors of the DUT. Further discussions on this assumption will be provided later in the performance analysis section. e_k in Fig. 3(b) is the error between the estimate of v_k in (7) and its true value. In this case, e_k is limited by the step size of the wobbling voltages and can be made very small by a sufficient number of wobbling steps in a fixed range.

We have shown that wobbling can effectively increase the resolution of testing, but test accuracy is not guaranteed because we do not know the exact value of T_j in (7). If we appropriately set the wobbling range, there will be more than one transition in the m-ADC's output codes that are associated with v_k. In Fig. 3(b), the output code changes from j to $j+1$ at the wobbling level $\delta_{dk(j+1)}$. This gives us another estimate, which is given as

$$\hat{v}_{k,j+1} = T_{j+1} - \delta_{dk(j+1)} = v_k - e'_k \tag{8}$$

where $\delta_{dk(j+1)} = d_{k(j+1)}/N_w - 1/2$. For each v_k, we can have at least two equations, like (7) and (8). There are a total of 2^*N of such equations, for $k = 0, 1, 2, \ldots, N-1$, in N v_k and $N_{\mathrm{ADC}} - 1$ T_j variables. Since the m-ADC's resolution is lower than that of the DUT, $N_{\mathrm{ADC}} - 1$ is smaller than N. Therefore, the DUT's output voltages and m-ADC transition levels can simultaneously be solved from the $2N$ linear equations under the least squares sense when necessary.

The DUT's linearity specifications can be calculated from the estimated v_k's using the equations given in Section II. The estimation errors in (7) and (8) (e_k and e'_k) are bounded by the wobbling step size and can be reduced by applying a small wobbling increment between two consecutive wobbling levels. If we make this increment much smaller than 1 LSB of the DUT, the final test result that is based on the estimated values will have a very high accuracy.

C. Implementation of the Proposed Algorithm

It is inefficient to simultaneously solve $2N$ equations in (7) and (8), especially when N is large. By investigating the equations' structure, we find that v_k's and T_j's can be calculated from the equations by applying a series of simple arithmetic operations.

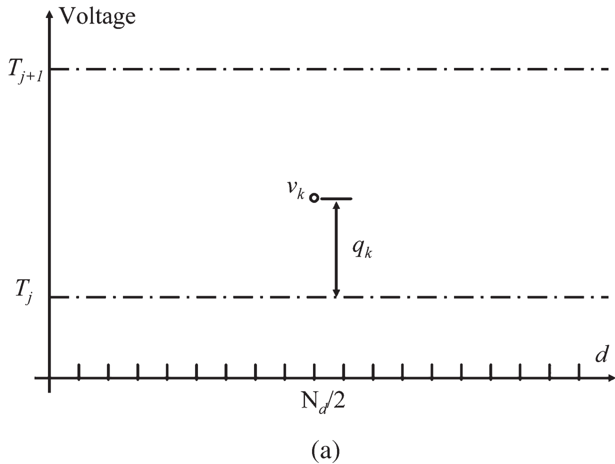
We can first calculate the m-ADC's jth code bin width $W_j = T_{j+1} - T_j$ from (7) and (8) as

$$\hat{W}_j^{(k)} = \delta_{dk(j+1)} - \delta_{dkj} \tag{9}$$

where errors e_k and e'_k are neglected. For different v_k's, we may have other estimates of W_j. The final estimate is the average

TABLE I
OUTPUT OF THE m-ADC VERSUS THE INPUT OF THE w-DAC

DUT output \ w-DAC input	0	1	2		d	…				N_w-1
v_0	2	2	2	3	3	3	3	4	4	4
v_1	2	2	3	3	3	3	3	4	4	4
v_2	2	2	3	3	3	3	4	4	4	4
…										
v_k	40	41	41	41	41	42	42	42	42	43
…										
v_{N-2}	60	60	60	61	61	61	61	61	62	62
v_{N-1}	60	60	61	61	61	61	61	62	62	62



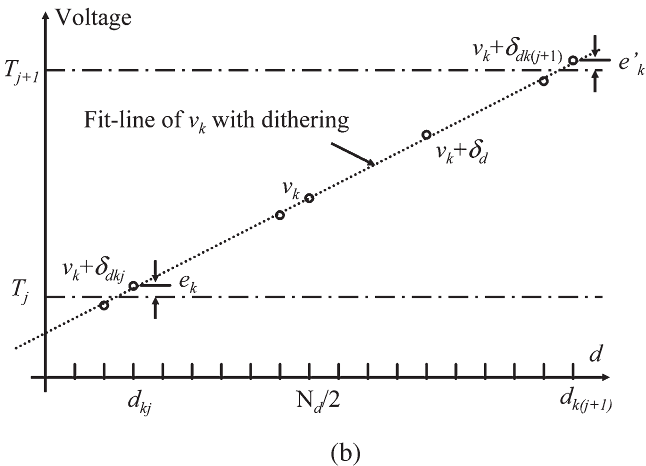


Fig. 3. DAC testing with wobbling.

over all of these values

$$\hat{W}_j = \operatorname*{mean}_k \left\{ \hat{W}_j^{(k)} \right\}. \tag{10}$$

Transition levels of the m-ADC can then be calculated by taking cumulative summations of these code bin widths as

$$\hat{T}_j = \sum_{i=0}^{j-1} \hat{W}_i. \tag{11}$$

The DUT output voltage can be calculated from (7) and (8) as

$$\hat{v}_k = \operatorname*{mean}_j \{\hat{T}_j - \delta_{dkj}\} \tag{12}$$

where the average is taken over all the T_j's covered by the wobbled copies of v_k.

The proposed DAC testing strategy can be summarized by the following steps.

1) The DAC under test generates a periodic waveform with different wobbling levels.
2) The flash ADC quantizes the wobbled waveform.
3) Estimate the ADC transition points using (9)–(11).
4) Calculate DAC output voltages using (12).
5) Characterize DAC performance based on the measured waveform.

IV. PERFORMANCE ANALYSIS AND OTHER ISSUES

This section provides performance analysis and implementation considerations of the proposed DAC testing strategy.

A. Performance Analysis

An intuitive observation of the proposed algorithm is that the test result will be more accurate if the m-ADC has a higher resolution or the w-DAC can provide more distinct wobbling levels with high resolution and linearity. Further analysis is in agreement with this observation, and the test accuracy of the proposed method can be described as

$$A_{\text{test}} = n_{\text{ADC}} + \text{ENOB}_w - \log_2 \alpha \tag{13}$$

where A_{test} is the desired test accuracy in bits, n_{ADC} is the m-ADC's resolution, ENOB_w represents the linearity of the w-DAC, and α is the scaling factor in m-ADC's LSB. The test accuracy is the m-ADC accuracy plus the effective accuracy of the w-DAC. Since the wobbling range covers α LSBs of the m-ADC, $\log_2 \alpha$ bits are subtracted out. In (13), we assume that the w-DAC has a sufficient resolution so that the error introduced by wobbling is dominantly dependent on w-DAC's linearity, and the effect of w-DAC's quantization noise is neglected. This assumption is reasonable as the resolution is comparatively easy to get, while the linearity of a DAC is

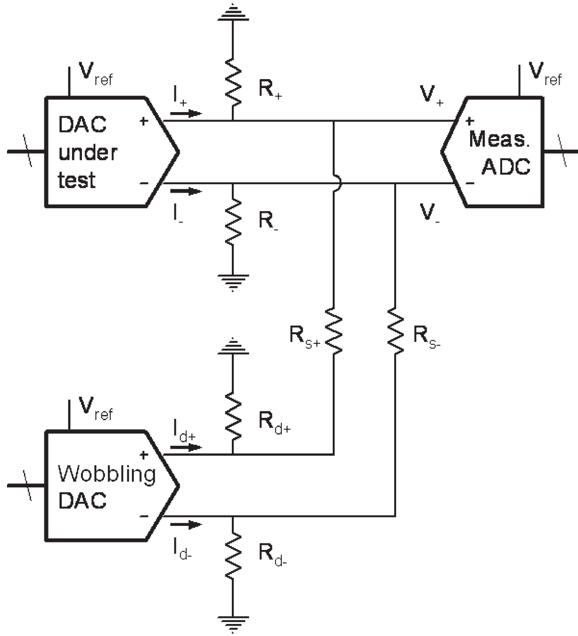


Fig. 4. Circuit implementation of the proposed test scheme.

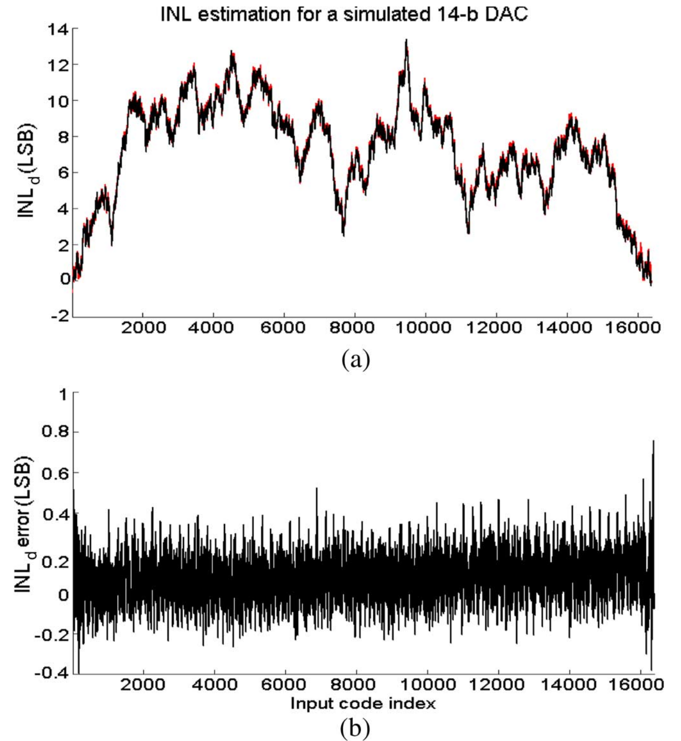


Fig. 5. INL_k estimation of a 14-bit DAC. (a) True and estimated INL_k's are plotted in black and red, respectively. (b) Estimation errors.

limited by the design and manufacturing technologies. In (7) and (8), we assume that the w-DAC is linear, even if it is actually not, so that the nonlinearity of the w-DAC will affect the final test accuracy. Therefore, the w-DAC can only provide an accuracy improvement that is equal to ENOB_w. However, if the w-DAC can accurately be characterized or calibrated, the w-DAC can improve the test accuracy even more.

By using the aforementioned equation, we can determine the requirement on the test devices for specific test accuracy. For example, if we have a 6-bit ADC and the wobbling range is 4 LSB at the 6-bit level, we need the following w-DAC linearity to achieve a 14-bit accuracy:

$$\mathrm{ENOB}_{\mathrm{dith}} = A_{\mathrm{test}} - n_{\mathrm{ADC}} + \log_2 \alpha = 14 - 6 + 2 = 10 \text{ (bit)}. \tag{14}$$

Equation (14) means that a 6-bit ADC can provide a 14-bit test accuracy if a 10-bit linear wobbling is available. As shown in Fig. 2, the w-DAC generates a waveform at a much lower speed than the main DAC under test. It is justifiable to use a medium-speed DAC in testing a high-speed DAC. The w-DAC can specifically be designed for testing purposes or can simply be another device from the same product family of the DUT.

B. Scaling and Summation Circuit

By assuming that the DUT and the w-DAC are fully differential current-steering DACs, a practical realization of the proposed test scheme is shown in Fig. 4. The scaling of the w-DAC's output and the wobbling summation can physically be implemented with the π networks of resistor ($R_{+/-}$, $R_{s+/-}$, and $R_{d+/-}$). If the w-DAC and the DUT are the same product, $R_{+/-}$ and $R_{d+/-}$ are also the same. To correctly match DACs' output impedance and to set the scaling factor, the resistance values need to be appropriately chosen such that

$$\begin{aligned} R_{+/-} \| (R_{s+/-} + R_{d+/-}) &= R_0 \\ R_{+/-} / (R_{s+/-} + R_{+/-}) &= \alpha \end{aligned} \tag{15}$$

where R_0 is the desired load resistance of the DACs. The aforementioned conditions can uniquely determine the nominal values of $R_{+/-}$, $R_{s+/-}$, and $R_{d+/-}$. The exact value of α is not critical to the linearity test as it will be normalized out in the final DNL and INL. We only need to guarantee that it is big enough to cover three code bins of the m-ADC. Since resistive networks are usually very linear, it will not introduce extra nonlinear errors in wobbling, which is necessary to guarantee the m-ADC characterization.

V. Simulation Results

The 14-bit DACs were tested in the simulations. The proposed algorithm is not dependent on the architecture of the DUT. We chose the thermometer-coded current-steering DAC as the DUT since it has the largest number of independent errors from each of the current sources, although it is not realistic.

A 6-bit flash ADC was used in the measurement. The INL of the m-ADC is about 0.3 LSB so that the m-ADC is 6 bit linear. Transition levels of the ADC were first measured, as discussed in Section III-C. The DUT has an INL of 14 LSB, and its true INL_k is plotted in black in Fig. 5(a). The DUT has about 10-bit linearity. Another 12-bit DAC of the same structure is used to provide 4096 wobbling levels. This w-DAC has about 10-bit linearity, with an INL of 3 LSB at the 12-bit level.

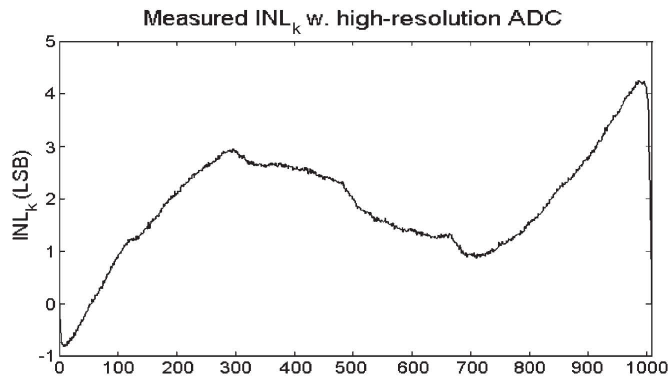


Fig. 6. INL_k measurement with a high-resolution ADC.

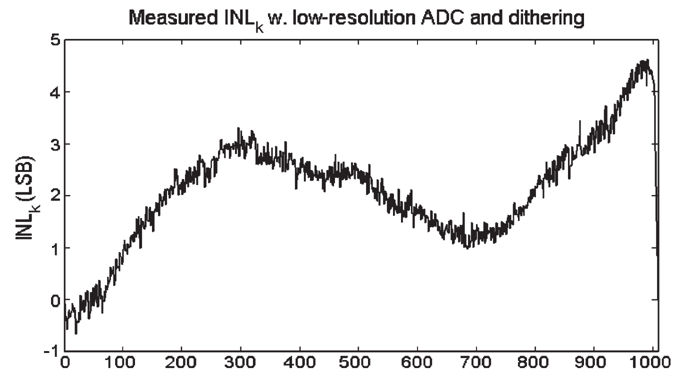


Fig. 7. INL_k measurement with a 6-bit ADC and a 9-bit wobbling.

In the simulation, the wobbling range was chosen to be 3.6 LSB of the m-ADC, and a noise is added to the input of the m-ADC, with a standard deviation that is equal to 0.25 LSB at the 14-bit level. This is the only noise of the input signal. The large quantization error of the m-ADC always exists and will be corrected by the proposed algorithm. Based from the calculation in Section V, a 6-bit ADC, a 10-bit linear wobbling, and the aforementioned wobbling range can provide a 14-bit test accuracy. The estimated INL_k of the DUT is plotted in red in Fig. 5(a). The estimated curve very well matches the true INL_k curve. The estimation errors for all codes are shown in Fig. 5(b). The INL_k of the DUT was tested to be better than 1-LSB accuracy at the 14-bit level.

VI. Experimental Results

Some experiments were done to validate the performance of the proposed DAC testing algorithm using low-resolution ADCs. We used a Conejo baseboard by innovative integration in our experiments. This board has four 16-bit DACs, four 14-bit ADCs, and a TI DSP on-chip. As the total number of samples for the wobbled measurement is limited by the data storage capability of the board, testing of very high-resolution DACs was not carried out, but we can show that the concept of the proposed method is working by the following results. Since there was no 6-bit ADC in our test setup, we used only the six most significant bits of the high-resolution ADC on the Conejo baseboard.

A pseudo-10-bit DAC was generated by using the 16-bit DAC on the Conejo baseboard for INL_k testing. An extra sinusoidal shape INL_k was purposely introduced. INL_k of the 10-bit DUT was measured by using a 14-bit ADC many times. The mean value of INL_k from different measurements, when the noise effect is averaged out, would be used as a reference in evaluating the performance of the proposed method. It is shown in Fig. 6. The 10-bit DAC was then tested by using the proposed algorithm with a 6-bit ADC, from truncation, and 512 level wobbling. The wobbling range is set to be about 5% of the m-ADC input range. The measured INL_k is shown in Fig. 7.

It can be calculated from (13) that a 6-bit ADC, plus a 9-bit wobbling and the wobbling range we used, can provide about 13-bit test accuracy. In Figs. 6 and 7, we can observe that the INL_k's that are measured by the 14-bit ADC and the proposed method are very close to each other. Therefore, the algorithm works and achieves the performance that we predicted.

VII. Conclusion

An effective DAC testing approach is presented in this paper. This approach uses high-speed flash ADCs and wobbling to test high-resolution DACs. The simulation results show that the INL_k of the 14-bit DACs can be tested to 1-LSB accuracy by using a 6-bit ADC and 12-bit wobbling. The experimental results also supported the effectiveness of the algorithm in DAC testing by using low-resolution ADCs. Because the proposed algorithm does not require high-precision test instruments, it provides a practical solution to the problem of production and on-chip testing of high-speed, high-resolution DACs.

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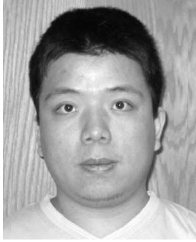

Le Jin (S'02–M'06) received the B.S. degree in electrical engineering from Shanghai Jiaotong University, Shanghai, China, in 2001 and the Ph.D. degree in electrical engineering from Iowa State University, Ames, in 2006.

He has been working with the Data Conversion Systems Group, National Semiconductor Corporation, Santa Clara, CA, since 2006. His research interests include cost-effective mixed-signal testing methodologies and design techniques.

Dr. Jin is a member of Tau Beta Pi.

Hosam Haggag received the B.Sc. and M.Sc. degrees in electrical engineering and solid-state physics from the University of California, Berkeley, in 1985 and 1987, respectively.

He was with Technology Transfer Associates and AMD. He was a Senior Engineering Manager with National Semiconductor Corporation, Santa Clara, CA.

Randall L. Geiger (S'75–M'77–SM'82–F'90) received the B.S. degree in electrical engineering and the M.S. degree in mathematics from the University of Nebraska, Lincoln, in 1972 and 1973, respectively, and the Ph.D. degree in electrical engineering from Colorado State University, Fort Collins, in 1977.

He was a Faculty Member with the Department of Electrical Engineering, Texas A&M University, College Station, from 1977 to 1990. Since 1991, he has been a member of the Faculty with the Department of Electrical and Computer Engineering, Iowa State University, Ames, where he is currently the Willard and Leitha Richardson Professor. His teaching and research interests are in the fields of analog and mixed-signal VLSI design, specifically in the areas of amplifier design, test and built-in self-test of mixed-signal circuits, data converter design, device modeling, and design for yield.

Dr. Geiger is a past member of the Board of Governors, a past Vice President of Publications, and a past President of the IEEE Circuits and Systems Society. He was a member of the IEEE Publications Board and the IEEE Periodicals Council and is a past Chair of the Transactions Committee of the Periodicals Council. He was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS PART II and the Circuits and Systems Society Editor of the *IEEE Circuits and Devices Magazine*. He has served in various capacities on the Technical Program Committees and Organizing Committees for the IEEE International Symposium on Circuits and Systems and the IEEE Midwest Symposium on Circuits and Systems. He received the Meritorious Service Award from the IEEE Circuits and Systems Society in 1996, the Golden Jubilee Medal from the IEEE Circuits and Systems Society in 2000, and the IEEE Millennium Medal in 2000.

Degang Chen (S'90–M'92–SM'02) received the B.S. degree in instrumentation and automation from Tsinghua University, Beijing, China, in 1984 and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of California, Santa Barbara, in 1988 and 1992, respectively.

From 1984 to 1986, he was with the Beijing Institute of Control Engineering which is a space industry R/D institute. From March to August 1992, he was the John R. Pierce Instructor of electrical engineering with the California Institute of Technology, Pasadena. After that, he joined Iowa State University, Ames, where he is currently an Associate Professor. He was with the Boeing Company, Chicago, IL, in summer 1999, where he became an A. D. Welliver Faculty Fellow and was with Dallas Semiconductor-Maxim, Dallas, TX, in summer 2001. His research experience includes particulate contamination in microelectronic processing systems, vacuum robotics in microelectronics, adaptive and nonlinear control of electromechanical systems, and dynamics and control of atomic force microscopes. His current teaching and research interests are in the area of analog and mixed-signal (AMS) VLSI integrated circuit design and testing. In particular, he is interested in low-cost high-accuracy test and built-in self-test of AMS and RF circuits and in self-calibration and adaptive reconfiguration/repair strategies for the enhancement of the performance and yield of such circuits.

Dr. Chen received the Best Paper Award at the 1990 IEEE Conference on Decision and Control and the Best Transaction Paper Award from the *ASME Journal of Dynamic Systems, Measurement, and Control* in 1995.