# On-Chip At-Speed Linearity Testing of High-resolution High-Speed DACs Using DDEM ADCs with Dithering

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***Abstract*—On-chip testing of high-resolution high-speed DACs is extremely challenging because of the stringent requirements on the accuracy, speed and cost of the measurement circuits. This work proposed a new on-chip strategy for DAC linearity testing applying the proposed deterministic dynamic element matching (DDEM) technique. Low-accuracy two-step flash ADCs are used as test devices. Speed advantage of flash structure enables at-speed testing, while its accuracy and resolution are improved by DDEM algorithm, the second stage and dithering. In this paper, the architecture of the DDEM flash ADC and DDEM algorithm are described. The design consideration of the major circuit blocks are talked about. The test performance is analyzed theoretically and verified by simulation. Simulation shows that a dithering incorporated two-step flash DDEM ADC, which consists of a 6-bit coarse DDEM stage, a 6-bit fine stage and a 5-bit dithering DAC, with linearity of all the blocks only at about 6-bit level, is capable of testing 14-bit DACs.**

**Key Words— On-chip, BIST, DAC linearity, DDEM**

## I. INTRODUCTION

The integration level of CMOS circuits is continuously evolving along with the technology scaling. Today's 65nm Pentium D CPU carries 376 millions transistors, which is about 50 times as many as the Pentium II in 350nm process nine years ago. Meanwhile, working 45nm CPU products using the new technology have been manufactured with doubled transistor density. High integration level enables explosive growth in the portable device applications as well as the technologies of system-on-a-chip (SOC) and system-in-package (SIP). Consequently, analog and mixed-signal (AMS) circuits, which are indispensable in most systems, are deeply embedded, and therefore it is becoming more challenging to make cost-saving and accurate testing of those circuits by using the traditional production test techniques. On-chip testing of AMS circuits is now getting more and more interesting to the industry and the academia.

As an interface between digital processing and the analog world, digital-to-analog converter (DAC) is one of the most widely used mixed-signal integrated circuits. In the recent years, along with the demands of new applications in wireless communications and multimedia signal processing, digital to analog conversion performance becomes increasingly important [1]. High-speed high-resolution DACs are widely manufactured and used. Some commercial parts, such as AD9771 from ADI and DAC5678 from TI, have 16-bit resolutions and more than 500MSPS update rates. Consequently, testing of those high-performance DACs becomes one of the most challenging problems in the area of AMS test.

On-chip built-in self-test (BIST) enables improvement in test efficiency and test speed. Meanwhile, it avoids high-cost using of external automatic test equipments (ATE). However, BIST needs additional circuitry, which sometimes is not a trivial to implement. This problem is more obvious when BIST is applied to the linearity test of high-speed and high-resolution DACs since it usually needs measurement circuits with much better linearity performance and faster speed than DACs under test. Measurement circuits with high performance but low cost have been regarded as the bottleneck of on-chip DAC testing.

This work provides a solution to high-performance DAC on-chip testing by using low-accuracy but high test performance circuits. Low-accuracy circuits are usually fast, easy to build and cost effective. In order to use them as measurement devices, we need improve their linearity/ resolution performance. A so-called deterministic dynamic element matching (DDEM) technique has been proposed for linearity improvement [2]. The idea has been applied to the design of current-steering DACs for on-chip stimulus generation [2] [3]. The latest experimental results show that a 12-bit thermometer-coded DAC with only 9-bit original linearity can equivalently generate 16-bit linear outputs by applying DDEM. In [4], the DDEM method incorporated with dithering technique is investigated for high-performance DAC testing with low-resolution flash ADCs. This work will extend the study on the algorithm, the test structure and the circuit implementation. The rest of the paper is organized as follows. Section II briefly discusses DACs' linearity specifications and testing of digital to analog converters. Section III describes the proposed BIST structure and

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DDEM test algorithm. Section VI theoretically evaluates the test performance. Section V talks about some design considerations of the DDEM ADC. Section IV shows the simulation results and Section IIV concludes the paper.

## II. Linearity Specifications of DACs

The nonlinearity errors in a DAC come from variations and mismatches in the conversion circuitry, and are usually characterized by the differential nonlinearity (*DNL*) and integral nonlinearity (*INL*). *DNL* is the maximum deviation in the output steps from the ideal step size. *INL* is the maximum deviation of the output transfer curve from an end-point fit line. For a DAC input code *k*, we define

$$DNL(k) = \frac{V_{k+1} - V_k}{LSB} - 1 \quad , \tag{1}$$

$$INL(k) = \frac{V_k - V_0}{LSB} - k \quad , \tag{2}$$

where $V_i$, $i$=0,1…$2^n$-1 are the outputs of an n-bit DAC at code $i$ and the least significant bit, *LSB*, is defined as

$$LSB = \frac{V_{2^n-1} - V_0}{2^n - 1} \quad . \tag{3}$$

Then the overall *INL* and *DNL* are the maximum values of the magnitudes of *INL(k)*s and *DNL(k)*s, respectively. From the equations, we can clearly see that DACs' linearity characteristics are calculated from DACs' output levels. Thus, the major task of testing is to accurately estimate each output of DACs. Usually, high-resolution and high-linearity analog to digital converters are used to quantize the DACs' outputs for calculation. As we have mentioned, these ADCs are very hard to build when DACs under test are high resolution and operate at high clock rate.

## III. DDEM Technique and Test Structure

In this section, we talks about how DDEM improves the linearity of low-accuracy circuits and make it suitable for on-chip testing.

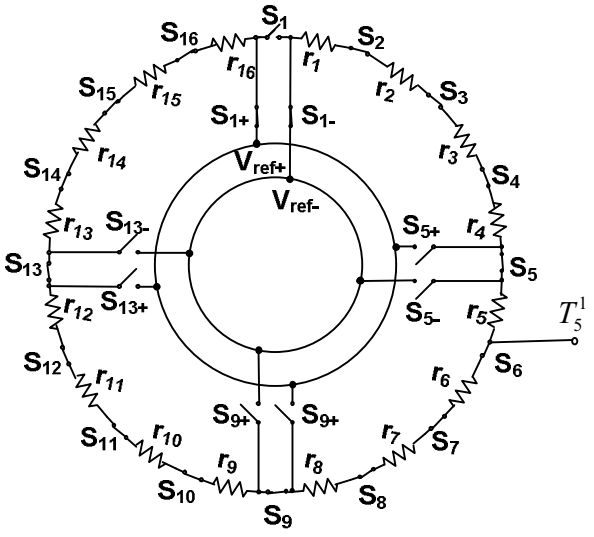


Figure 1. Resistor loop of a 4-bit DDEM flash ADC with $P = 4$

The basic idea of DDEM is that instead of building one high-performance ADC satisfying the resolution, linearity and speed requirements, we use DDEM to generate a set of ADCs with low resolution, low linearity, but fast speed, which are much easier to implement. Although the transition levels of each ADC are inaccurate, those of all the ADCs are distributed nearly evenly in their common input range. As a result, the overall resolution and linearity performances are greatly improved. Flash structure is adopted for this application because of its speed advantage. However, the resolution of single-stage flash ADCs is limited by their large number of comparators and usually no more than 8 bits. To reduce the quantization noise, we add a second stage and a dithering input DAC. The second stage also uses flash structure so that the speed performance is not degraded so much. The detailed ADC structure will be discussed in Section V.

DDEM technique is applied to the first-stage resistor string. As a 4-bit example shown in Fig. 1, 16 resistors are connected in a loop through switches. By opening one switch in the loop (e.g., $S_1$ off) and connecting the two broken ends to the reference voltages (e.g., $S_{1+}$ and $S_{1-}$ on), a resistor string is formed to generate transition voltages for coarse comparison. In DDEM, one of $P$ switches, which are uniformly distributed in the loop (e.g., $S_1$, $S_5$, $S_9$ and $S_{13}$ for $P=4$), can be turned off at one time to form a resistor string. $P$, denoted as the iteration parameter, represents the number of resistor strings we construct. $P$ is then also the number of digital outputs generated for one analog ADC input. Assume there are $N$ resistors in the loop. $P$ is selected to be one of the submultiples of $N$, i.e. $q=N/P$ is an integer. It can be shown that due to resistance mismatch, $P$ different sets of ADC transition levels form a nearly uniform distribution. The measurement of any analog input to the DDEM ADC can be represented by the average of the $P$ different digital outputs associated to that input. Then, *DNL*s and *INL*s of DACs under test can be calculated.

The structure of the whole BIST system is shown in Fig. 2. A dithering DAC is added at the input of the DDEM ADC to further reduce the nonlinear errors of the first stage and the quantization errors. In operation, the dithering DAC linearly shifts the outputs of the DAC under test in a small range to provide more configurations for testing. The full-scale output range of the dithering DAC is adjustable according to the value of $P$. It should be noted that the shifted DAC outputs need to be covered by the effective input range of DDEM ADC.

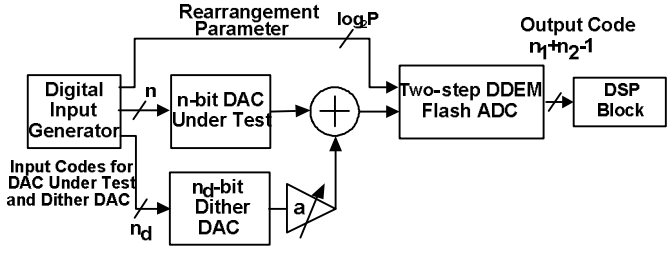


Figure 2. Block diagram of the proposed BIST scheme

## IV. Test Performance Evaluation of The Proposed DDEM ADC

In this section, we theoretically evaluate the linearity performance of the proposed scheme. We will look at the DDEM ADC itself firstly and then add on the effect of dithering.

For a specific input voltage without dithering, $V_{in}$, the test system generates $P$ digital outputs. The average of those $P$ digital outputs is used as the measurement of $V_{in}$, $m_{in}$, as expressed in

$$m_{in} = \frac{1}{P}\sum_{j=1}^{P} d_j \,. \tag{4}$$

Considering the two-step structure, we can further express $m_{in}$ as

$$m_{in} = \frac{1}{P}\sum_{j=1}^{P}\left(d_j^c + d_j^f\right) = \frac{1}{P}\sum_{j=1}^{P}\left(T_{id}\left(d_j^c\right) + r_j + \varepsilon_j\right), \tag{5}$$

where $d^c_j$ and $d^f_j$ are the first-stage (also known as the coarse stage) and second-stage (also known as the fine stage) outputs with proper scaling respectively. They can be equivalent represented by the ideal coarse-stage transition level at code $d^c_j$, which is $T_{id}(d^c_j)$, and the residue voltage, $r_j$, with quantization error $\varepsilon_j$ generated by the second stage. On the other hand, the input $V_{in}$ can be accurately expressed in multiple ways as

$$V_{in} = T_{id}(k) + r_{in} = T_j(d_j^c) + r_j, j = 1, \cdots, P, \tag{6}$$

where $T_{id}(k)$ is the nearest ideal coarse-stage transition level smaller than $V_{in}$, $r_{in}$ is the residue voltage calculated by subtracting $T_{id}(k)$ from $V_{in}$, $T_j(d^c_j)$ is the actual transition level at code $d^c_j$ under the $j^{th}$ switch configuration and $r_j$ is the residue voltage generated for the fine-stage quantization. By comparing the expressions of the measurement in (5) and the true input in (6) and using the equality in (6), we can express the estimation error $e_{in}$ as

$$e_{in} = m_{in} - V_{in} = -\frac{1}{P}\sum_{j=1}^{P} INL_j(d_j^c) + \frac{1}{P}\sum_{j=1}^{P}\varepsilon_j, \tag{7}$$

where $INL_j(d^c_j) = T_j(d^c_j) - T_{id}(d^c_j)$ is the coarse-stage integral nonlinearity error at code $d^c_j$ under the $j^{th}$ switch configuration. The definitions of the differential and integral nonlinearity errors provide the following relationships:

$$INL(k) = \sum_{i=1}^{k} DNL(i), \tag{8}$$

$$\sum_{i=1}^{N} DNL(i) = 0, \tag{9}$$

where $N$ is the number of resistors in the string. In DDEM algorithm, the differential nonlinearity errors are shifted by switching. Then, (9) can be rewritten in another way as

$$\sum_{j=1}^{P}\sum_{t=1}^{s*q} DNL_j(t) = s \times \sum_{i=1}^{N} DNL_1(i) = 0, \tag{10}$$

where $q=N/P$ and $s$ is a number in 1, 2, …, $P$ and satisfies $d^c_j - sq \geqq 0$ for all $j$=1, 2, …, $P$. With the three equations of $DNL$ and $INL$ above, the estimation error can be further expressed as

$$e_{in} = m_{in} - V_{in} = -\frac{1}{P}\sum_{j=1}^{P}\sum_{t=1}^{d_j^c - s*q} DNL_j(t) + \frac{1}{P}\sum_{j=1}^{P}\varepsilon_j, \tag{11}$$

It is noted that the first term in (11) is reduced to the summation of a set of non-repeating $DNL(k)$s, the value of which should be comparable to the $INL$ of the original coarse stage, $INL_C$. It is noticed that this term is approximately periodic over the ADC input range with a period of $q$ coarse-stage $LSB$s. Assume the quantization error part becomes negligible after fine-stage quantization. The estimation error becomes

$$e_{in} \approx -\frac{1}{P} INL_C \,. \tag{12}$$

Then the linearity of the coarse stage is improved by $\log_2 P$ bits.

Now the effect of the input dithering DAC is considered. Its full-scale input range is taken as one period of the estimation error, which is $q$ $LSB$s of the coarse stage, noted as $LSB_C$. The similar analysis to the DDEM part can show that this setup further reduces the nonlinear error after DDEM. The effect of the dithering is similar to that of the DDEM. And the estimation error with the dithering DAC can be finally expressed as

$$e_{tot} \approx \frac{1}{2^{n_d}}\frac{1}{P} INL_C, \tag{13}$$

where $n_d$ is the resolution in bit of the dithering DAC and the quantization error part is neglected. As a result, the test performance of the whole system can be calculated as

$$n_{test} \approx ENOB_C + \log_2 P + n_d, \tag{14}$$

where $ENOB_C = n_1 - \log_2 INL_C - 1$ is the effective number of bits of the coarse stage.

## V. Considerations of Circuit Implementation

In this section, we focus on the implementation of the two-step DDEM flash ADC, which is the main part of the whole system.

The structure of the two-step DDEM ADC is shown in Fig. 3. The DDEM ADC is composed of a 6-bit DDEM first stage, a residue amplifier and a 6-bit second stage flash ADC. Sample and hold stage is not necessary since DACs under test themselves will compensate for the time delay in the coarse and fine quantization. The first stage does the conversion for the first 6 MSB bits. After that, a residual voltage is created by subtracting the differential reference, which is the transition level of the coarse stage at code of the coarse-stage digital output, from the analog input. In order to avoid missing codes, the full-scale range of the second stage ADC is set to be equivalent to 2 $LSB$s of the first stage. To achieve that, the residue amplifier amplifies the generated residue voltage by a gain of 32.

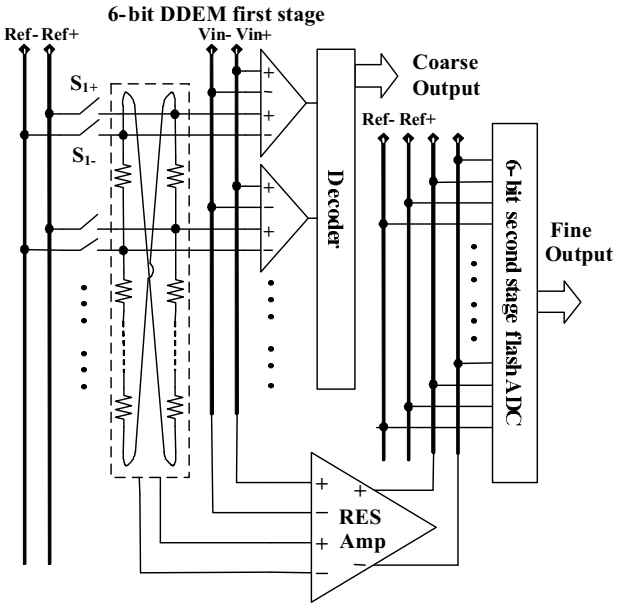


Figure 3. Structure of the proposed two-step DDEM ADC

Since the basic idea of our on-chip testing solution is to using low-accuracy circuits, the proposed scheme should be able to accommodate a considerable level of errors. In the rest of this section, three major circuit nonidealities, which include the on-resistance of switches, the offsets, and the gain error of the residue amplifier, will be discussed. Some of them will be approved by theoretical analysis to be non critical. Others will degrade the test performance and need to be taken care of.

### A. On-Resistance of the Switches in Resistor Loop

Switches in the resistor loop have there own resistance when conducting. As shown in Fig. 1, those resistances are added to the resistors in the loop and affect the transition levels. Unlike the resistors, which have only voltage-independent random mismatches, the resistances of MOS switches are voltage-dependent and vary with their positions in the R-string because of their different gate-source voltages. In DDEM algorithm, resistors in the R-string will be cyclically shifted to different voltage levels. For $P$ different configurations, there are $P$ different transition levels, $T_1(k)$, $T_2(k)$ … $T_P(k)$, generated for a specific digital output code $k$. In the ideal case, those transition levels are generated by resistances with only random mismatches so that the average of $T_1(k)$, $T_2(k)$ … $T_P(k)$ is close to the ideal transition level. However, if a voltage-dependent part is included in the resistance, all the transition level will exhibit the same level of error and so does their average. It can be shown that this error cannot be canceled out by DDEM algorithm.

To solve this problem, the switches need to be moved out of the resistor loop, while the shifting ability of DDEM remains. That can be achieved in fully differential structure. In Fig. 3, all the resistors are in a fixed loop. Switches are used to connect different nodes to the references. With one pair of switches on (like $S_{1+}$ and $S_{1-}$), there are two resistor strings formed and connected to $V_{ref+}$ and $V_{ref-}$. Differential transition levels can be generated for comparison. In this case, there are only two switches in the resistor strings and they are always connected to $V_{ref+}$ and $V_{ref-}$. Therefore, voltage-dependent resistance is removed.

### B. Offset Voltages

Two kinds of offset voltages are discussed in this subsection, which are comparator offset voltages and the residue amplifier offset voltage.

#### 1) Comparator Offset Voltages

Comparator offset voltages degrade the accuracy of flash ADCs since they directly sum to the reference voltages generated from the resistor strings. The offset voltages are random and characterized by the standard deviation. To design for high yield, the standard deviation is usually less than 0.2 *LSB* of the ADC. Large transistors or some offset cancellation techniques sometimes are necessary to reduce the offsets.

Two-step ADCs usually have extra input range in their second stage to compensate for the comparator offsets in the first stage. In the DDEM ADC described herein, the full-scale input range of the second stage is equivalent to 2*LSB* of the first stage. Thus, $\pm 0.5LSB$ of the first stage is available for error compensation. In addition, averaging effect of DDEM and dithering further relaxes the requirement on the first stage comparator offsets. Simulation results show that a 6-bit first stage can have comparator offsets voltages with a standard deviation of 0.3*LSB* of the first stage without degrading the test performance significantly. Thus, the first stage comparators can be very low-accuracy and area-efficient.

The second stage will not affect the linearity but the quantization error of the system. Therefore, the second stage comparator offsets are not critical as long as the quantization error is small enough. Small input transistors can be used in the second stage comparator to reduce the load capacitance of the residue amplifier and therefore improve the speed.

#### 2) The Offset Voltage of the Residue Amplifier

Offset voltage error of the residue amplifier changes the residue signal by a fixed value. For any analog input of the ADC, this error induces a constant offset in the final measurement. The good thing is the constant offset will not cause any error in *DNL* and *INL* estimation since they are calculated from not absolute DAC output levels but relative ones.

### C. Gain Error of the Residue Amplifier

The residue amplifier amplifies the difference between the input signal and the reference by a nominal gain of 32. Gain error of the amplifier will induce missing codes or cause the two-step ADC non-monotonic. In this subsection, we will analysis the effect of the gain error in DDEM algorithm. Gain error of the residue amplifier can be divided

into two parts: the gain difference error and the gain variation error. The gain difference is the static error between the nominal gain and the actual gain after fabrication. It does not change during the ADC operation. The gain variation error represents the dynamic error of the gain, which changes with the input common mode of the residue amplifier.

*1) The Gain Difference Error:*

In this design, open-loop low-gain amplifiers are used for residue amplification because of their high bandwidth. The whole amplifier consists of three gain stages. Each stage has a nominal gain of about 3.2 to achieve the desired gain of 32. However, the gain of the open-loop amplifiers can not be accurately controlled as a result of process variation. Assume we have an analog input $V_{in}$. The measurement of $V_{in}$ obtained from the dithering incorporated DDEM ADC is expressed as

$$m_{in} = \frac{1}{N_D P}\sum_{i=1}^{N_D}\sum_{j=1}^{P} C_{i,j}\,, \tag{15}$$

where $N_D$ is the number of available dither levels, $P$ is the iteration parameter and $C_{i,j}$ is the digital output of the DDEM ADC associated with the $i^{th}$ dither level and $j^{th}$ R-string configuration. Assume $m_{in0}$ is the measurement when the gain of the residue amplifier is exactly 32. It can be shown that with an actual gain of $32+\Delta G$ the measurement can be expressed as

$$m_{in,\Delta G} = m_{in,0} + \frac{\Delta G}{32}\cdot\frac{1}{N_D P}\sum_{i=1}^{N_D}\sum_{j=1}^{P} r_{i,j}\,, \tag{16}$$

where $r_{i,j}$ is the residue voltage for $i^{th}$ dither level and $j^{th}$ R-string configuration. The second item in the right part of (16) is the additional error induced by the gain difference. It is noted that the dithering DAC almost uniformly spreads the analog input in $q$ *LSB*s of the first stage. At the same time, DDEM algorithm also randomizes the residue voltages associated with a specific analog input uniformly into a 1-LSB range. Although each of the residue voltages associated with a specific input can not be accurately expressed, the average of them is nearly constant especially for a large $P$. Thus, the error term in (16) is almost constant for all the input signals and will not affect the estimation of *INL*. This fact greatly reduces the sensitivity of the testing accuracy with respect to the gain difference error.

*2) The Gain Variation Error*

The inputs of the residue amplifier are two differential signals. Their common mode signal depends on the input signal level and is different for different first-stage digital outputs. The disadvantage of this fact is that changing of the common mode will cause the gain of the amplifier to vary and make it input signal dependent. As described in the subsection V.A, this signal dependence generates test error that cannot be cancelled by DDEM and dithering since this error is almost constant for a specific analog input despite of DDEM and dithering, but different for different input levels. It is noticed from the analysis that the induced estimation error directly copies the gain variation. Therefore, it can be calibrated out if the gain variation is tested. This information can be obtained from the digital outputs of the second stage. The second stage quantizes the amplified residue voltages. For the same first-stage output code $k$, the largest of all the second-stage output codes shows the characteristics of the gain error as well as *DNL(k)* of the first stage. If ignore the quantization error, the maximum second-stage output at code $k$, $C^f_{Max,k}$, can be expressed as

$$C^f_{Max,k} = G\cdot(1+g_k)\cdot(1LSB_C + DNL(k)) \text{ 永永永永永永}$$

where $G$ is the static gain of the amplifier, $g_k$ is the normalized dynamic gain variation at code $k$. Considering DDEM algorithm, we have the maximum outputs under different configurations as $C^f_{Max,k,1}$, $C^f_{Max,k,2}$, …, $C^f_{Max,k,P}$. Then, the average can be calculated as

$$\bar{C}^f_{Max,k} = G\cdot(1+g_k)\cdot\left(1LSB_C + \frac{1}{P}\sum_{j=1}^{P} DNLj(k)\right), \tag{18}$$

where $DNL_j(k)$ represents the *DNL(k)* error under the $j^{th}$ DDEM configuration. It is easy to show that with $P=2^{n_1}$, where $n_1$ is the first-stage resolution in bits, we have

$$\frac{1}{P}\sum_{j=1}^{P} DNL_j(k) = 0\cdot \tag{19}$$

Thus the gain variation error can be accurately estimated from the second-stage output codes.

## VI. Simulation Results

The proposed DDEM algorithm and test scheme are verified by numerical simulation. In simulation, a 14-bit DAC is modeled as the device under test. Its *INL(k)*s are shown in the top plot of Fig. 4. The test system has a 6-bit DDEM first stage, a 6-bit second stage and a 5-bit dithering DAC. The linearity of the coarse stage is less than 7 bits with the INL of 0.38LSB. The fine stage and the dithering DAC are nearly 6-bit linear. The standard deviations of comparator offsets in two stages are *0.3LSB* of the first and second stages respectively. The gain of the residue amplifier is 32. A noise is added to the input of the DDEM ADC with a standard deviation equal to 1 *LSB* at the 14-bit level. With *P=32*, the quantization error is calculated to be less than 16-bit level. The test performance of the specified system is roughly equivalent to $n_{test}=6+5+5=16$ *bits*. Therefore, it should be

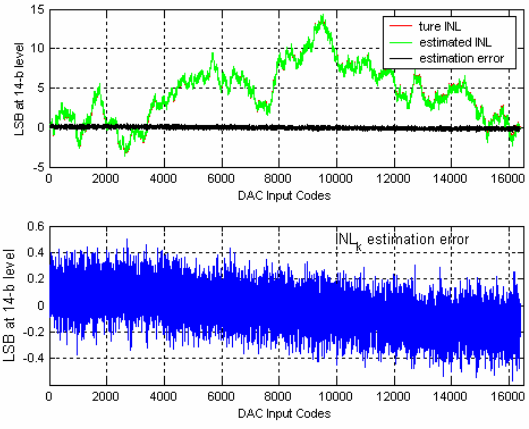


Figure 4. *INL(k)* estimation error with P=32 and 5-bit dithering DAC, 14 bits DAC under test

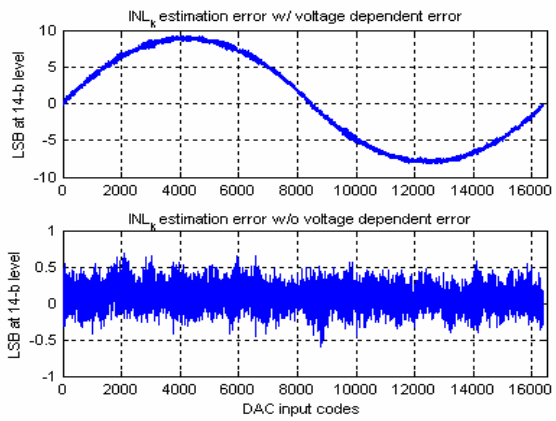


Figure 5. $INL_k$ estimation error w/ and w/o voltage-dependent errors

capable of testing a 14-bit DAC. Fig. 4 shows that with the above configuration the maximum *INL(k)* estimation error is about *0.5LSB* at 14-bit level and the *INL* estimation error is *0.0729LSB*.

The effect of voltage-dependent resistance is simulated. The same system parameters are used in the test of a 14-bit DAC. The estimation errors (difference between estimated *INL(k)* and true *INL(k)*) with and without voltage-dependent resistance are plotted in Fig. 5. The voltage-dependent resistance variation in the simulation is set to be 1% of the nominal value. Simulation result shows that voltage-dependent resistance in the first-stage R-string will cause considerable estimation error. Those resistances, such as switch on-resistance, need to be removed from the R-string.

Fig. 6 shows the *INL(k)* estimation errors in the cases of the actual gain of the residue amplifier equal to 32, 37 and 27 respectively. The system configurations are the same as the previous. Simulation results verify that the DDEM ADC can accurately test 14-bit DACs with a large gain difference error.

The calibration of the gain variation error is simulated. Fig. 7(a) shows the normalized gain variation against first-stage outputs simulated in Spectre. The induced test error is

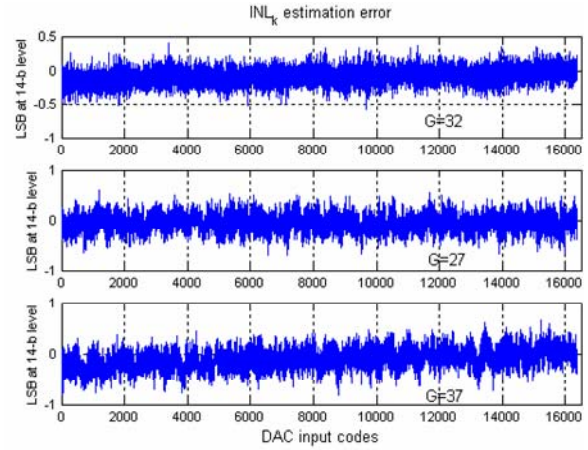


Figure 6. INLk estimation error when *G=32,27 and 37*

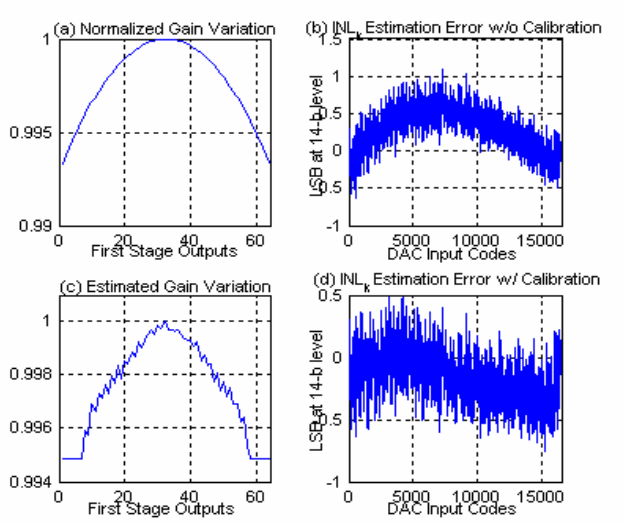


Figure 7. INLk estimation error when $\Delta G=0$, *5 and -5*

shown in Fig. 7(b). Set $P=2^{n_1}=64$ for the calibration. Fig. 7(c) shows the estimated gain variation and the estimation errors after calibration is shown in Fig. 7(d). Simulation shows that the system's test ability is not degraded by the variation error after calibration.

## VII. Conclusions

This paper describes an on-chip BIST method for the linearity testing of high-performance DACs. This method overcomes the difficulty of DACs' on-chip testing in requiring costly high-accuracy measurement devices. Low-accuracy but high-speed flash ADCs are used with the proposed DDEM algorithm. Both theoretical analysis and simulation show that this method is capable of providing high-resolution test results. In addition, it is also shown in the paper that the proposed algorithm and circuit structure can accommodate considerable circuit nonidealities. These characteristics make this method a promising solution to on-chip testing of high-precision DACs.

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