An Overview and Behavioral Modeling of Higher Order Multi-Bit ΣΔ A/D Converters

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Abstract— **This paper presents an overview of the developments made in the field of oversampling sigma-delta (ΣΔ) data converters. Further, an approach to model a 4th order multi-bit ΣΔ ADC using Simulink, Matlab is proposed. It is shown that behavioral modeling provides comparable accurate results, and is much faster in comparison to spectre based simulations.**

I. Introduction

Since its provenance in the early 1960's, Sigma Delta (ΣΔ) modulation methods have evolved through a number of generations to become one of the most attractive and popular technique for realizing high resolution, high performance analog-to-digital (ADC) and digital-to-analog (DAC) converters. Sigma Delta modulation exploits oversampling and digital signal filtering to produce a high resolution digitized output [1]. A typical oversampled A/D converter is shown in Fig. 1. First, the modulator samples and produces a single-bit or multi-bit pulse code modulated output. Then, using digital low pass filter high frequency noise components introduced by the quantizer is removed and the output is decimated, yielding a high resolution digital output [2]. In comparison to flash data converters, ΣΔ ADC provide high resolution without the need of component trimming and calibration. As a consequence ΣΔ ADC have reported resolution of 20 bit or higher that is far difficult to realize in CMOS component matching [3].

In recent years, research has shifted towards increasing the bandwidth of the ΣΔ ADC. One method has been to increase the order of the modulator. The basic modulator architecture used for an Nth order modulator is depicted in Fig 2. The number of integrator in the forward path depicts the order of the modulator. More aggressive noise shaping resulting in higher resolution can be achieved by increasing the order of the modulator. However, this improvement in resolution of the modulator comes at the cost of the stability of the single bit quantizer, because it is not possible to avoid overloading the 1-bit loop quantizer [4]. An obvious solution to this problem is to increase the number of levels in the quantizer. In addition to avoiding quantizer overload, multibit approach would also improve integral linearity, and also facilitate implementation of higher order loop filters as the low frequency oscillation observed in higher order modulators are caused by overloaded quantizers [5].

Another trend being observed in the area of ΣΔ ADC is the implementation of continuous time (CT) loop filters. In comparison to the earlier switched-capacitor circuits, CT ΣΔ ADC offer higher clock frequency and/or consume less power [6]. Inception of new architectures requires behavioral modeling of the system to validate its performance capabilities. This paper sheds light on the developments made in the area of ΣΔ ADC's and presents a behavioral modeling approach using Simulink, MATLAB, for the new developed architectures.

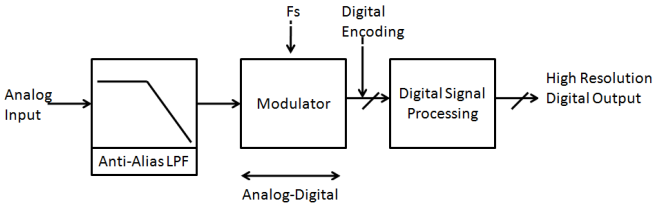


Figure 1 Block Diagram of Oversampling ADC

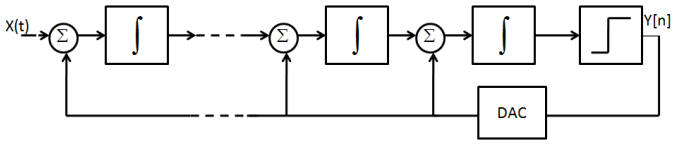


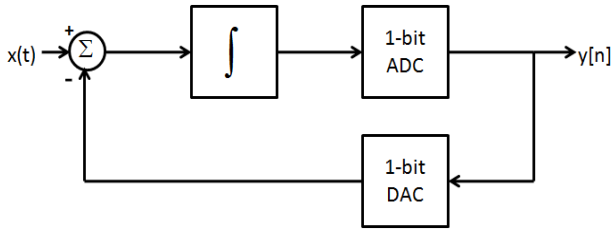
Figure 2 Nth Order Sigma Delta Modulator

II. ΣΔ Modulator Behavioral Model

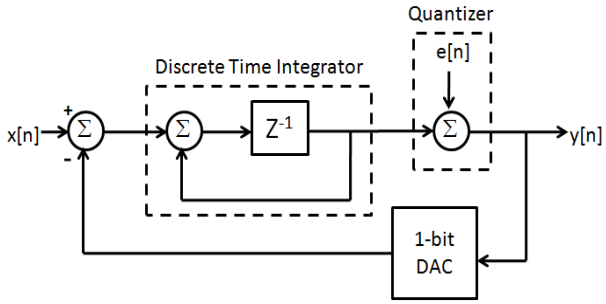
ΣΔ ADC is a non-linear system (due to the quantization effect of ADC) and also a dynamic system (due to the memory in the integrator) [7]. This section develops models for higher order modulators and multibit architectures. Using these techniques a fourth order four bit sigma delta modulator is designed and modeled in Simulink. A continuous time model is then derived using bi-linear transform techniques.

A. Sigma-Delta Modulators

Fig. 3a depicts the simplest form of an oversampled noise shaping sigma-delta modulator. The modulator consists of an integrator, an internal ADC or quantizer, and a DAC used in feedback path. The input to the quantizer is not x[n], but a filtered version of the input x(t) and the analog representation of the output y[n]. It is important to realize that ΣΔ modulators are highly nonlinear systems because of the quantizer [8]. To properly model and analyze the ΣΔ modulator the quantizer is generally replaced with an injected noise source as shown in Fig 3b. Further the integrator can be replaced by a discrete time integrator whose transfer function is $z^{-1}/(1-z^{-1})$.



(a)



(b)

Figure 3: First Order Sigma Delta Modulator, (a) block diagram and (b) equivalent linear model

If the single bit DAC is assumed to be ideal then it can be replaced by a unity gain transfer function and the modulator output can be expressed as:

$$y[z] = H_x(z)x[z] + H_e(z)e[z] \quad (1)$$

such that $H_x(z) = z^{-1}$ and $H_e(z) = (1\text{-}z^{-1})$. The output is thus a delayed version of the input plus quantization noise that has been shaped by a first order Z domain differentiator or high pass filter. For the first order modulator the SNR can be derived and expressed as:

$$SNR = 10\left[\log\left(\frac{\sigma_x^2}{\sigma_e^2}\right) - \log\left(\frac{\pi^2}{3}\right)\right] + 30\log\left(\frac{f_s}{2f_b}\right) \text{ (dB)} \quad (2)$$

Observing from Equation 2 that SNR for the system improves by 9dB, or equivalently the resolution improves by 1.5 bits for every doubling in oversampling ratio (OSR). However, many problems arise when implementing an ADC using a sigma-delta modulator.

B. Linear Model Assumptions

The linear model depicted in Fig. 3b represents the quantization error as an additive noise source. It is imperative to understand that quantization noise is actually an error and is partly deterministic. The quantization noise can be modeled as an additive noise source assuming: 1) Quantization levels are equiprobable. This is true for signals with uniformly distributed amplitude but only approximately true for sinusoidal signals 2) the quantizer does not overload 3) the quantization steps are uniform 4) the quantization noise and input signal are uncorrelated.

The weakest assumption is considering quantization noise being independent of the input signal [9]. In a sigma-delta modulator, the state of the system is determined by the output of loop integrator value along with the input value. The modulator has only one state variable and therefore the loop can lock itself into a mode where the output bit stream repeats in a pattern [5]. Therefore, the frequency spectrum of the output bit stream will contain significant noise energy concentrated at multiples of the limit cycle frequency.

Clearly, the above effect raises questions on the assumption of quantization noise modeled as an additive noise source and the stability of the modulator. Dithering has been used commonly to randomize the input of the quantizer. This is an attractive solution, however it requires an additional signal source and it also usually reduces the dynamic range of ADC. An alternative solution is to increase the loop order or/and increase the quantizer bits.

C. Higher order loops

Higher order loops is based on the idea of embedding multiple sigma-delta loop within the main loop. With more than one integrator in the loop, the quantization noise responses rises as an M^{th} exponential function as compared to the linear relationship of the first order topology. The higher the order the more aggressively the quantization noise gets shaped in the baseband frequencies. Therefore increasing the loop order effectively reduces the quantization noise power at low frequency resulting in higher effective resolution for the same oversampling ratio. The basic architecture is shown in fig. 2.

An order M modulator based on the architecture shown in fig.2 can be analyzed extending equation 1 for higher orders. For the N^{th} order the $H_x(z) = z^{-N}$ and $H_e(z) = (1\text{-}z^{-1})^N$ which contains M zeros at z = 1 or at DC frequency on the unit circle [10]. Similarly to the first order modulator the SNR for the N^{th} order modulator can be derived and expressed as:

$$SNR = 10\left[\log\left(\frac{\sigma_x^2}{\sigma_e^2}\right) - \log\left(\frac{\pi^{2N}}{2M+1}\right)\right] + (20N+10)\log\left(\frac{f_s}{2f_b}\right) \text{ (dB)} \quad (3)$$

Comparing Equation 3 to the first order modulator SNR it is observed that there is a tremendous improvement in SNR. For an N^{th} order modulator, every doubling in oversampling ration provides an extra (6N+3) dB of SNR, or equivalent (N+ 1/2) bits of resolution. Fig. 4 shows the frequency response of first, third and fifth order modulator.

Increasing the modulator order improves the SNR dramatically. However this improvement is achieved at the cost of the stability of the modulator. With increased number of integrators in the feedforward loop the input to quantizer grows large and causes the quantizer to overload. Three common approaches to stabilize the quantizer include, 1) designing the generic Nth order modulator on the basis of the root locus method, 2) increasing the size (number of bits) of the in loop ADC-DAC to allow a greater dynamic range of signals in the loop [11], and 3) cascading multiple stages of first order sigma delta modulator.

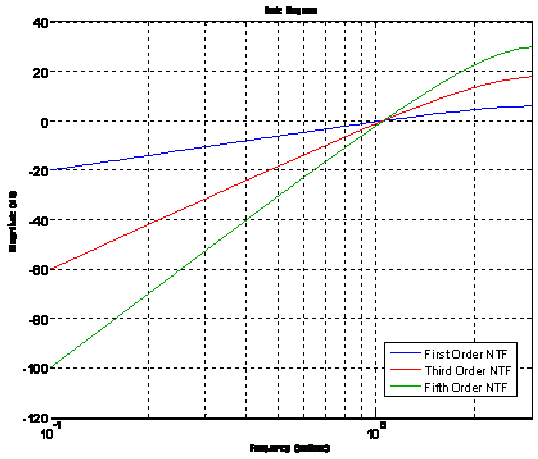


Figure 4: NTF Frequency Response for First, Third and Fifth Order Modulator

D. Nth Order Modulator (Feedforward/Feedback)

The NTF of ΣΔ converters can be realized for achieving higher resolution by pushing more noise power outside the signal band. This can be realized by using architecture shown in Fig. 5 that allows placing the zeros and poles of the NTF at desired locations. The system function for this topology can be analyzed by deriving the transfer function using Masons Rule, assuming the quantization noise is an additive noise source. The resulting system function is expressed in the equations below [5]:

$$y[n] = H_x(z)x[z] + H_e(z)e[z] \quad (1)$$

Where

$$H_x(z) = \frac{\sum_{i=0}^{N} A_i(z-1)^{N-i}}{z\left[(z-1)^N - \sum_{i=1}^{N} B_i(z-1)^{N-i}\right] + \sum_{i=0}^{N} A_i(z-1)^{N-i}} \quad (4)$$

$$H_e(z) = \frac{(z-1)^N - \sum_{i=1}^{N} B_i(z-1)^{N-i}}{z\left[(z-1)^N - \sum_{i=1}^{N} B_i(z-1)^{N-i}\right] + \sum_{i=0}^{N} A_i(z-1)^{N-i}} \quad (5)$$

E. Design of Loop Coefficients

Equations 4 and 5 provide the designer a degree of freedom to give an arbitrary shape to the noise shaping filter. Thus once the pole-zero location are know the loop coefficients can be easily derived. The A_i and B_i coefficients control the poles and zeros of the NTF respectively. It has been observed from simulations that a small portion of the noise spectrum at the upper edge of the baseband dominates the total in-band noise power. To reduce this effect, the NTF can be shaped within the in-band. As compared to Fig. 4 where the noise power approximately linearly with increase in frequency, the in-band NTF can be shaped using Chebyshev polynomials to achieve frequency response as shown in Fig. 6. Comparing the 4th order NTF to the Chebyshev designed 4th order modulator it can be noticed that within the signal band the Optimal Chebyshev filter provides increased noise shaping. The loop coefficients in this design can be derived using the method

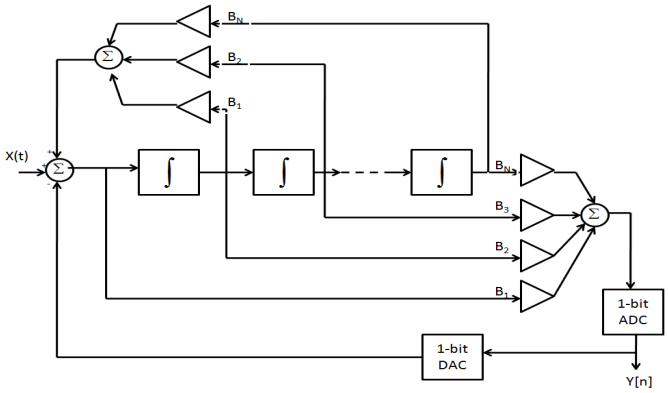


Figure 5: Nth Order Sigma Delta Modulator

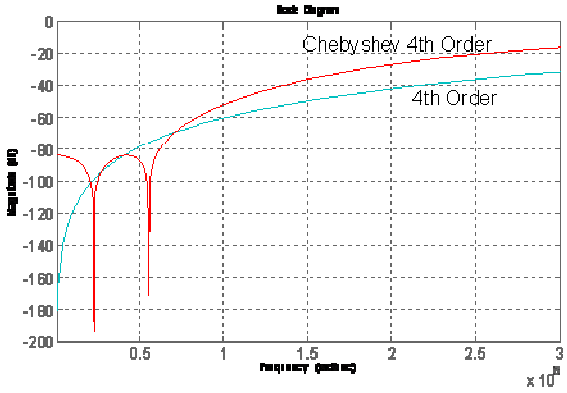


Figure 6: Frequency Response of Chebyshev Designed NTF

described in [5]. The above architecture was then implemented in Matlab to obtain spectral specifications of the modulator. The simulation results are presented in part 3. With increased number of integrator in the loop and increased feedback/feedforward paths, the input to the quantizer is more random and thus the important assumption of the quantization noise and the input of the quantizer being uncorrelated are valid.

F. Signal Dependent Stability

The model shown in Fig.3 is unfortunately inadequate in providing sufficient information about the stability of the system. The technique commonly used in analyzing the stability of a nonlinear system was first presented by Kalman [3] where he modeled nonlinear block with an arbitrary number of gain values. Thus, the quantizes in our case could be modeled with a linear gain values dependent on the quantizer input as shown in Fig. 7.

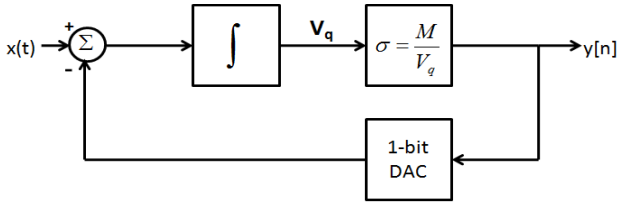


Figure 7: Sigma Delta Modulator modeled with a variable gain Quantizer

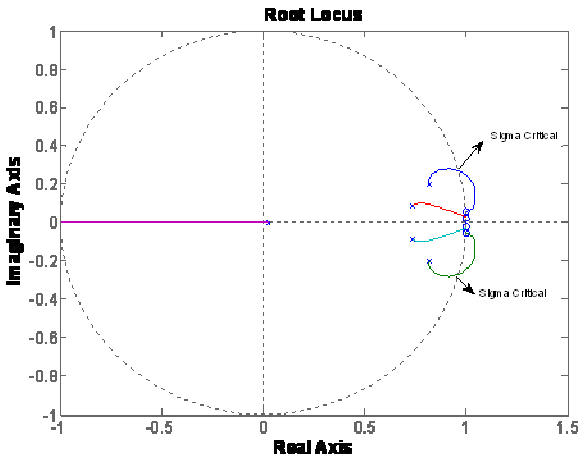


Figure 8: Root Locus Plot for 4th Order Sigma Delta Modulator

The gain value as shown is given by:

$$\sigma = \frac{M}{V_q} \tag{6}$$

where σ is the quantizer gain, V_q is the quantizer input and M is the output. where σ is the quantizer gain, V_q is the quantizer input and M is the output. It can be observed as the input amplitude varies the quantizer gain can have values ranging from zero to infinite, though practical limitations either extremes occurring. Modeling the quantizer in this particular way produces a root locus where the roots or the poles of the system move along the locus as the quantizer gain varies. For the system to become unstable and exhibit limit cycle, the poles of the system have to driven outside the unit circle. The root locus thus plots how the poles move with the changing quantizer gain. For the 4th order sigma delta modulator designed the $\sigma_{critical}$ = 0.593. Thus the modulator does not lead to stable limit cycle if the quantizer gain is less than 0.593. The quantizer gain model helps explain the experimentally observed phenomena of limit cycles and signal dependent stability. Instability could result whenever the signal is too large driving the roots outside the unit circle. Thus, stability can be controlled and designed by appropriately choosing A_i and B_i coefficients.

G. Multi-Bit Quantizer

Single Bit quantizer based ΣΔ ADC approach discussed so far is very suitable for MOS VLSI process because of its insensitivity to process and component variation [12-14]. However, it can be shown that [15-16] employing multibit ΣΔ structures can improve system stability. Further, increasing the levels of the quantizer improves the Dynamic Range of the modulator. The Dynamic range in dB can be derived [10]:

$$DR_{dB} = 10\log\left[\frac{3}{2}(2^B - 1)^2 \frac{(2L+1)OSR^{2L+1}}{\pi^{2L}}\right] \tag{7}$$

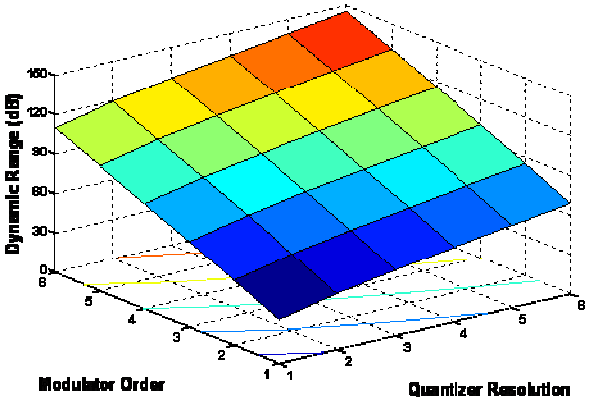


Figure 9: Range for Sigma Delta Modulator

A contour plot in Fig. 9 describes the improvement in Dynamic Range of the modulator with increase in number of bits of the quantizer and modulator order. However, this drastic improvement in DR and SNR requires the stringent absolute accuracy on the low resolution feedback DAC.

III. SIMULINK MODEL

Figure 5. architecture was modeled in Simulink of Matlab. Table 1 summarizes the gain coefficients used to obtain chebyshev shaped NTF at low frequencies.

TABLE I
FEEDBACK COEFFICIENTS

i	A_i	B_i
0	0.8653	-
1	1.1920	-3.540×10^{-3}
2	0.3906	-3.542×10^{-3}
3	0.06926	-3.134×10^{-3}
4	0.005395	-1.567×10^{-3}

An ideal multibit DAC is modeled in Simulink with mismatch effects as shown in Fig. 10 [17]. The non-linearity of the DAC introduces noise source in the feedback. The dac non-linearity is directly fedback to the input and thus is not shaped. This effect is modeled in Fig. 10. The unit elements are given by:

$$C_i = C + e_i \tag{8}$$

Where C is the ideal value and e_i is a deviation from the ideal value with a Gaussian distribution. The effects of this mismatch are significant as the increase the noise floor as shown in section 4. Various techniques such Dynamic Element Matching (DEM) have been used to remove this error, which is beyond the scope of this paper [12-14].

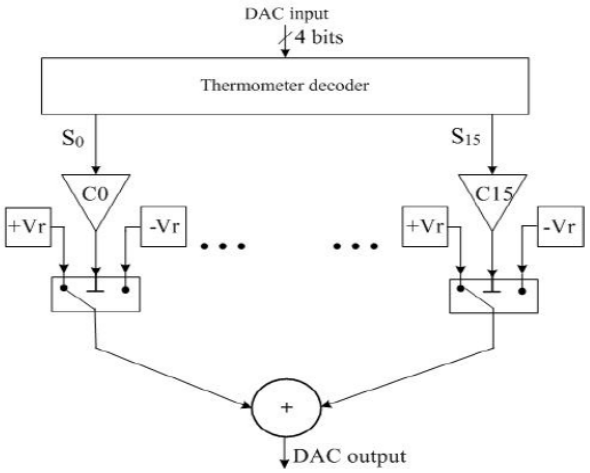


Figure 10: Behavioral modeling of multibit DAC

IV. Simulation Results

Behavioral modeling technique is a useful tool for gaining intuitive understanding or the modulators operations and design of loop coefficient. Fig 11 displays the power spectral density (PSD) for the 4th modulator designed with a single bit quantizer and a four bit quantizer. First, it is important to observe that the NTF has a chebyshev shape in the baseband. As explained in previous section, this improves the SNR that is evident from comparing theoretical SNR computed using equation 7 and measured SNR for chebyshev. The chebyshev noise shaping in signal band has slightly higher SNR. Further, the 4-bit quantizer PSD provides lowers the noise floor and provides much higher SNR.

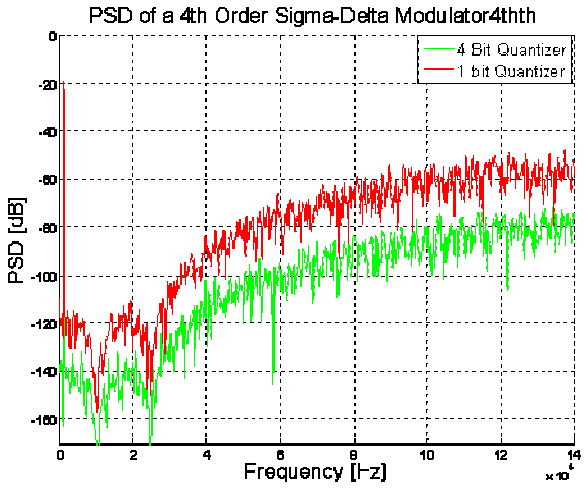


Figure 11: PSD of 4th order Sigma-Delta Modulator

Figure 12 depicts the statistics of the quantizer input. It is easily observed that with increase in the quantizer size the quantizer has much smaller input compared to the single bit. This assures the quantizer would not overload and thus increase in quantizer size supports the argument that the stability of the ΣΔ modulator improves.

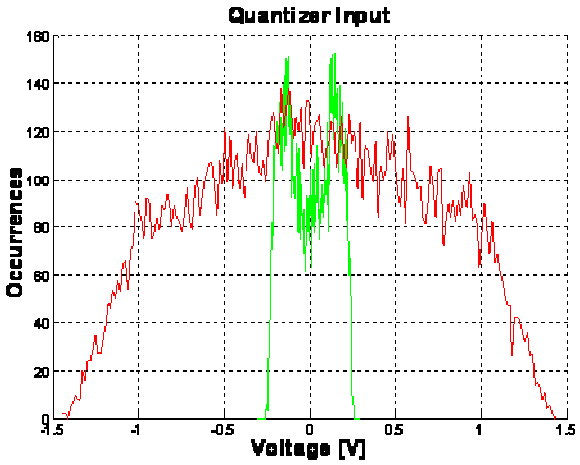


Figure 12: Quantizer input statistics

Fig. 13 shows the effect the DAC nonlinearity introduces to the sigma delta modulator output. The noise floor in the signal band is raised and also hints of low frequency signal are evident. This low frequency signal is usually corrected using dynamic element matching techniques.

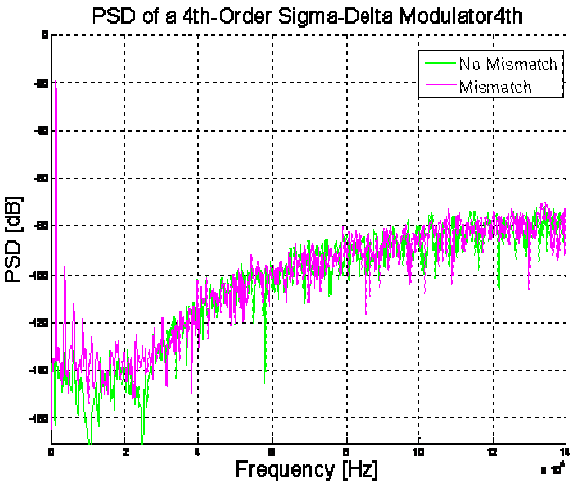


Figure 13: Mismatch effects of DAC on Sigma Delta PSD

TABLE III
Specifications Achieved

Architecture	Number of Quantizers	Theoretical SNR (dB)	Simulated SNR (dB)	ENOB (bits)
4th Order	1	79.90	81.18	13.26
4th Order Ideal DAC	4	103.32	102.7	16.77
4th Order Non-Ideal DAC	4	103.22	96	15.66

V. CONCLUSION

In conclusion, this paper discusses a successful approach for modeling a higher order multibit sigma delta modulator using Simulink, Matlab. The paper discusses key developments made in the oversampling data converter field and then models a 4^{th} order multibit sigma delta modulator in Matlab. The simulations results prove that the behavioral modeling provide reliable results, as seen from Table 3, and the approach could be used for predicting specifications from other architectures.

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