Optimal Area and Impedance Allocation for Dual – String DACs

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***Abstract*—The relationship between yield, area, and impedance distribution in dual-string DACs is developed. Optimal area allocation and impedance distributions strategies for maximizing yield in the presence of local random process variations are introduced. Simulation results show that a factor of 4 or more reduction in area for a given yield is possible if typical area/impedance allocations are replaced with an optimal area/impedance allocation.**

I. INTRODUCTION

Dual-ladder resistor string digital analog converters (DAC), which incorporate fine string least significant bits (LSB) ladders in parallel between two successive coarse ladder taps are widely used in industry [1,3,4,6]. When properly designed, the dual-ladder structures inherit most of the advantages of a string DAC such as monotonicity, speed, and versatility [1]. The major advantage of the dual-ladder DACs with a reduced number of resistors in the coarse ladder comes at the layout stage where layout complexity can be reduced since a common centroid layout of the coarse string resistors will effectively cancel linear gradient effects [4] for the entire DAC. Conventional wisdom suggests that the value of the coarse string resistors should be small and the area for the coarse string resistors should be large for a properly designed dual-ladder DAC [5].

As with any string DAC, if gradient effects are cancelled, the linearity performance of this architecture is limited by the random mismatch of the resistors in the ladders. This mismatch is usually dominated by the local random variations in the sheet resistance throughout the body of the resistors. The resultant random variations in the individual resistors are usually modeled as a Gaussian random variable. It is well-known that maximizing the resistor area is effective for minimizing the overall mismatch of the resistors [3]. Thus, a tradeoff can be made between area and matching accuracy. Beyond the conventional wisdom given in [5] that suggests the coarse ladder resistors should be larger in size and smaller in value than the fine string resistors to improve the integral nonlinearity (INL), there is little in the literature that suggests how large the area or how small the value of the resistors should be for obtaining good linearity performance.

In this paper, linearity performance tradeoffs between area in the coarse string and area in the fine string and between the resistance values in the coarse string and the resistance values in the fine string are discussed. Optimal area allocation strategies and optimal impedance allocation strategies for minimizing the INL are presented. Finally, a discussion is included about how much performance is lost if optimal area allocation strategies and optimal impedance allocation strategies are not utilized.

The rest of the paper is organized as follows. In Section II, the effect of sizes and resistances on the normalized variation of a simple circuit is analyzed. The relationship between linearity, area ratios, and resistance in the dual ladder resistor string DAC is discussed in the Section III. Simulation results for the linearity of several selections of resistor values and area are presented in Section IV.

II. VARIATION OF RESISTOR

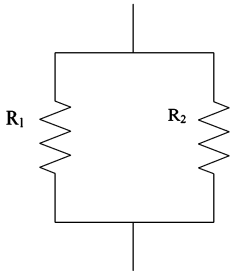

Figure 1. Two Resistor Circuit

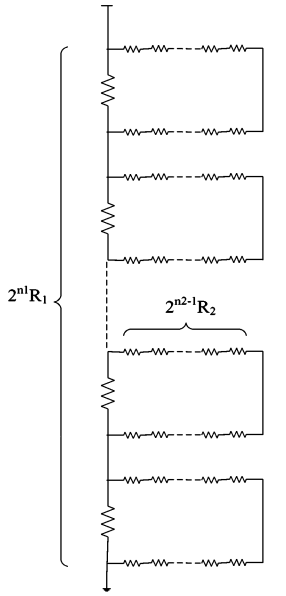

Figure 2. A dual resistor string

A simple circuit comprised of two parallel resistors is discussed in this section. The normalized variance of the equivalent resistance of the two resistors will be characterized in detailed. The results will provide insight into the analysis and optimization of the integral nonlinearity (INL) of the dual ladder resistor string that is discussed in the next section.

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Consider the two resistors shown in the Figure 1 where the resistance values and layout areas are R_1, R_2, A_1 and A_2. The equivalent resistance of the parallel combination is $R = \frac{R_1 R_2}{R_1 + R_2}$. For notational convenience, the variables u and v are defined by the expressions $u = \frac{A_1}{A_{TOT}}$ and $v = \frac{R}{R_1}$, where A_{TOT} is the total area of two resistors.

If a common centroid layout is used, any linear gradient effects of the resistor can be ignored and each of the resistances can be decomposed into the nominal resistance R_N and a component due to the local random variation in the sheet resistance R_R. With this notation, the equivalent resistance can be expressed as

$$R = \frac{R_{1N} R_{2N}}{(R_{1N} + R_{2N})} \frac{\left(1 + \frac{R_{1R}}{R_{1N}}\right)\left(1 + \frac{R_{2R}}{R_{2N}}\right)}{\left(1 + \frac{R_{1R} + R_{2R}}{R_{1N} + R_{2N}}\right)} \quad (1)$$

The resistance can be expanded in a Taylors series. Since $\frac{R_{1R} + R_{2R}}{R_{1N} + R_{2N}}$ is assumed small, this series can be truncated after the first-order terms. With this expansion, it follows that the normalized random component of the resistance can be expressed as

$$\frac{R_R}{R_N} = \frac{R_{1R}}{R_{1N}} + \frac{R_{2R}}{R_{2N}} - \frac{R_{1R}}{R_{1N} + R_{2N}} - \frac{R_{2R}}{R_{1N} + R_{2N}} \quad (2)$$

It thus follows that the variance of the normalized local random component can expressed by

$$\sigma^2_{\frac{R_R}{R_N}} = \sigma^2_{\frac{R_{1R}}{R_{1N}}} \left(\frac{R_{2N}}{R_{1N} + R_{2N}}\right)^2 + \sigma^2_{\frac{R_{2R}}{R_{2N}}} \left(\frac{R_{1N}}{R_{1N} + R_{2N}}\right)^2 \quad (3)$$

It is known that the normalized variance of a resistor is inversely proportional to the layout area of the resistor, A, and proportional to the square of $A_{\rho N}$, a process parameter that characterizes the variance of the resistor due to local random variations in the resistance in the process; $\sigma^2_{\frac{R_R}{R_N}} = \frac{A^2_{\rho N}}{A_i}$. Thus, it follows that the normalized variance can be written as

$$\sigma^2_{\frac{R_R}{R_N}} = \frac{A^2_{\rho N}}{A_{TOT}} \left[\frac{1}{u}(v)^2 + \frac{1}{(1-u)}(1-v)^2\right] \quad (4)$$

This variance can now be minimized by equating the partial derivatives with respect to u and v to zero. It follows from (4) that a minimum will be obtained if u = v. Therefore, the normalized variance of the local random component assumes a minimum value if and only if the ratio of the layout area of one resistor to the total area of the circuit is equal to the ratio of the equivalent resistance to the same resistance. A locus of critical points, which is a straight line in the u-v plane, is shown in Figure 3. Substituting u = v into (4), if follows that the minimum variance is given by $\sigma^2_{\frac{R_R}{R_N}} = \frac{A^2_{\rho N}}{A_{TOT}}$. The normalized deviations in the variance from the optimal value for different resistance ratios and different area ratios are summarized in Table 1.

If (u,v) is on the straight line, the normalized value is equal to 1, while in the upper right corner or the lower left corner of the table, this variance increases significantly.

This analysis shows that, for the same values of resistance and area of the circuit, as long as the ratio of the layout area of one resistor to the total area of the circuit is equal to the ratio of the equivalent resistance to its resistance, the variance of the equivalent random resistance is minimum, otherwise, if the layout area of one resistor is very big or very small and the resistance values are not sized favorably, the variance will be very large.

TABLE I. $\sigma^2_{\frac{R_R}{R_N}} : \frac{A^2_{\rho N}}{A_{TOT}}$ WITH DIFFERENTIMPEDANCES AND AREAS (1)

$A_1 / (A_1 + A_2)$	$R_2/(R_1+R_2)$				
	0.01	0.25	0.5	0.75	0.99
0.01	1	1.3	1.9	3.9	98.0
0.25	6.8	1	1.3	2.3	56.3
0.5	25.3	1.3	1	1.3	25.3
0.75	56.3	2.3	1.3	1	6.8
0.99	98.0	3.9	2.0	1.3	1

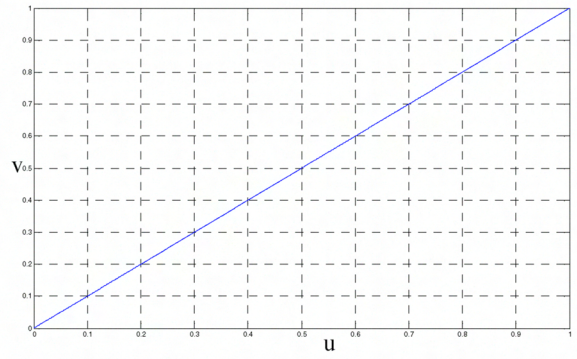

Figure 3. A locus of critical points

III. INL VARIATION OF A DUAL LADDER DAC

In the following, the performance of a dual –ladder resistor string DAC is analyzed by evaluating the variance of the integral nonlinear (INL) at different output taps. The coarse ladder in Figure 2 consists of 2^{n_1} coarse resistors each nominally of value R_1 and $2^{n_1+n_2}$ fine string resistors, each nominally of value R_2. The fine strings that are connected in parallel with each pair of coarse string taps each determine 2^{n_2} tap voltages.

The total number of tap voltages is thus $2^n=2^{n1+n2}$. The variance of the INL on each of the 2^n tap voltages is derived and the selection of areas and the resistors on both two ladders is determined to obtain the minimum value of the maximum error in the INL profile. Let x and z represent the ratio of the coarse ladder area to the total area of DAC, $\left(\frac{2^{n_1} A_1}{A_{TOT}}\right)$, and the ratio of the total equivalent resistance of DAC to the total resistance on the coarse ladder $\frac{R_{TOT}}{2^{n_1} R_1}$. Then, as in the previous section, the normalized variance of the equivalent resistance in one coarse ladder/fine ladder section can be expressed by

$$\sigma^2_{\frac{R_{eqR}}{R_{eqN}}} = \frac{2^{n_1} A^2_{\rho N}}{A_{TOT}} \left[\frac{z^2}{x} + \frac{(1-z)^2}{(1-x)} \right] \tag{5}$$

The output voltage at the tap $m = p \times 2^{n_2} + q$, $0 \le p < 2^{n_1}$ and $0 \le q < 2^{n_2}$, of the fine string ladder can be expressed as

$$V_m = \frac{V_{REF}}{\sum_1^{2^{n_1}} R_{eq,i}} \left[\sum_1^{p} R_{eq,i} + R_{eq,p+1} \left(\frac{\sum_1^{q} R_{2j}}{\sum_1^{2^{n_2}} R_{2j}} \right) \right] \tag{6}$$

This can be written as

$$V_m \approx \left(\frac{V_{REF}}{2^n} \right) \left[2^{n_2} p + 2^{n_2} \frac{\sum_1^{p} R_{eqR,i}}{R_{eqN}} - 2^{n_2 - n_1} p \frac{\sum_1^{2^{n_1}} R_{eqR,i}}{R_{eqN}} + q + q \frac{R_{eqR,p+1}}{R_{eqN}} + \frac{\sum_1^{q} R_{2Rj}}{R_{2N}} \right.$$
$$\left. - 2^{-n_2} q \frac{\sum_1^{2^{n_2}} R_{2Rj}}{R_{2N}} - 2^{-n_1} q \frac{\sum_1^{2^{n_1}} R_{eqR,i}}{R_{eqN}} \right] \tag{7}$$

where the resistance is decomposed into the normial resistance and the local random resistance. The INL profile in LSB ($V_{LSB}=V_{REF}/2^n$)at tap m is the difference betweeen V_m and the ideal tap voltage $mV_{REF}/2^n$. Expressed in LSB, we obtain:

$$INL_m = 2^{n_2} \frac{\sum_1^{p} R_{eqR,i}}{R_{eqN}} - 2^{n_2 - n_1} p \frac{\sum_1^{2^{n_1}} R_{eqR,i}}{R_{eqN}} + q \frac{R_{eqR,p+1}}{R_{eqN}} + \frac{\sum_1^{q} R_{2Rj}}{R_{2N}}$$
$$- 2^{-n_2} q \frac{\sum_1^{2^{n_2}} R_{2Rj}}{R_{2N}} - 2^{-n_1} q \frac{\sum_1^{2^{n_1}} R_{eqR,i}}{R_{eqN}} \tag{8}$$

By observing that $\sigma^2_{\frac{R_{2R}}{R_{2N}}} = \frac{A^2_{\rho N}}{A_2} = \frac{A^2_{\rho N}}{A_{TOT}} \times \frac{2^n}{(1-x)}$, it follows that the variance of INL_m can be expressed as:

$$\sigma^2_{INL_m} = \frac{2^{n_1} A^2_{\rho N}}{A_{TOT}} \left[\frac{z^2}{x} + \frac{(1-z)^2}{(1-x)} \right] \left[\left(2^{n_2} - p \times 2^{n_2 - n_1} - q \times 2^{-n_1} \right)^2 p + \right.$$
$$+ \left(q - p \times 2^{n_2 - n_1} - q \times 2^{-n_1} \right)^2 + \left(p \times 2^{n_2 - n_1} + q \times 2^{-n_1} \right)^2 (2^{n_1} - p - 1)$$
$$\left. + \frac{2^{n_2}}{(1-x)} \left(q \left(1 - q \times 2^{-n_2} \right)^2 + q^2 \times 2^{-2n_2} \left(2^{n_2} - q \right) \right) \right] \tag{9}$$

To minimize this variance, consider the patial derivative of this variance with respect to z which can be expressed as

$$\frac{\partial \sigma^2_{INLm}}{\partial z}(x,z) = \frac{A^2_{\rho N}}{A_{TOT}} 2^{n1} \left[\left(2^{n_2} - p \times 2^{n_2 - n_1} - q \times 2^{-n_1} \right)^2 p \right.$$
$$\left. + \left(q - p \times 2^{n_2 - n_1} - q \times 2^{-n_1} \right)^2 + \left(p \times 2^{n_2 - n_1} + q \times 2^{-n_1} \right)^2 (2^{n_1} - p - 1) \right] \left[\frac{2z}{x} + \frac{-2(1-z)}{(1-x)} \right] \tag{10}$$

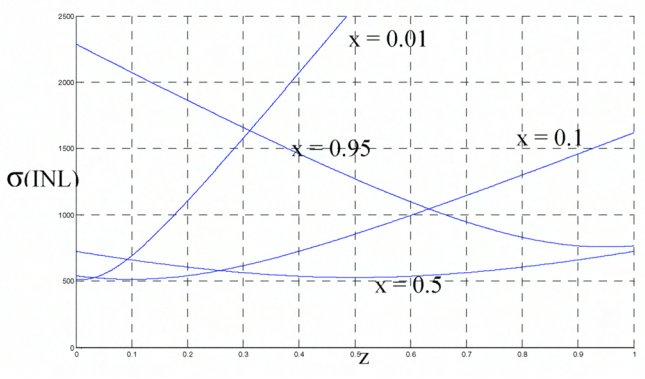

Figure 4. The minimum σ_{INL_m} with respect to x

For a given x, the variance in (9) is minimized by equating (10) to 0. It thus follows from (10) that a minimum will be obtained if z = x. It can also be shown that even when x = z, the INL decreases with x assuming a minimum value as x and z approach 0. Qualitatively, the normalized variance of the local random component in the dual-string DAC is minimum if the ratio of the total impedance to the coarse ladder impedance is equal to the given ratio of the layout coarse area to the total area of the circuit.

The standard deviation of the INL, plotted as a function of x, for a 10 bit dual ladder string DAC is ploted in Figure 4. It can be shown that increasing the number of bits on the coarse ladder will reduce the variance of INL. However, an increased number of resistors in the coarse ladder will increase the layout complexity. Furthermore, the smaller the values of x and z are, the smaller the value of the variance that is obtained. If there is no coarse ladder, σ(INL) will assume the minimum value.

IV. Simulation Results and Discussions

To visualize the results given in Section III, the special case where $n_1 = 4$ and $n_2 = 6$ will be considered for 9 different impedance and layout area allocations. These are shown as INL profile curves in Figure 5 when x and z are 0.01, 0.5 and 0.95. Depending upon the values of x and z, the INL profile shows ripple with local maxima and the local minima occurring at coarse ladder taps or at mid taps of the fine ladders. There are a total 2^{n_1+1} of these critical taps. The maximum variance always occurs at a sub-tap of the fine string DAC located in the neighborhood of the middle tap, independent of the impedance or area allocation used.

It can be seen that the INL deviation increases with |x – z| and decreases when both x and z move close to the origin. The maximum INL deviations shown in Fig. 4 are summarized numerically in Table 2.

These results show that when x and z are small, for example, x = z = 0.01, the normalized standard deviation of the maximum INL, $\sigma^2_{INL_m} : \frac{A^2_{\rho N}}{A_{TOT}}$, is approximately 512. Choosing non-optimal values of x and z reduces the effective number of bits (ENOB) of the DAC. For example, even when choosing x = z to get the minimum deviation for a fixed value of x, the ENOB reduces by 0.0412 bits when x = z = 0.5 and reduces by 0.536 bits when x = z = 0.95. Moreover, if x is in the neighborhood of 1 and z in the neighborhood of 0 or vice versa, then the deviation will be very large. The ENOB in the case x =0.95, z = 0.01 reduces by 2.15 bits and in the case x= 0.01, z = 0.95, it reduces by 3.25 bits.

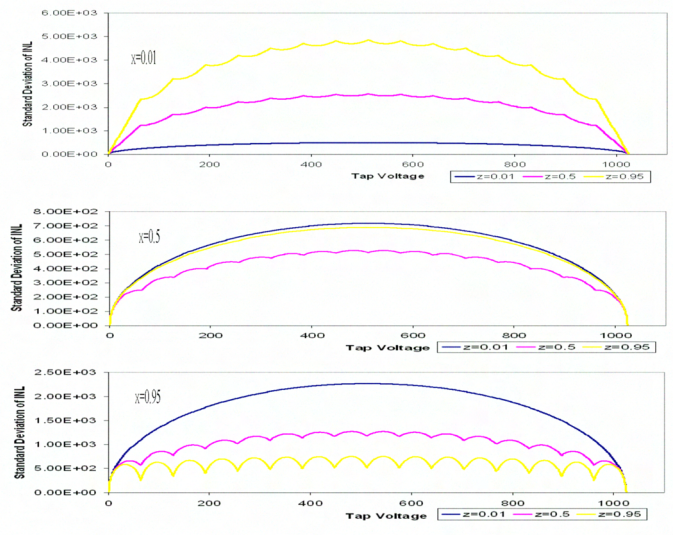

Figure 5. INL profiles of the dual ladder DAC

TABLE II. SIMULATION RESULTS OF INL DEVIATION

z	x=0.01		x =0.5		x= 0.95	
	$\sigma_{max(INL)}$	Δn_{EQ}	$\sigma_{max(INL)}$	Δn_{EQ}	$\sigma_{max(INL)}$	Δn_{EQ}
0.01	512.02		716.98	0.486	2267.19	2.15
0.5	2572.9	2.33	526.84	0.0412	1271.16	1.31
0.95	4864.07	3.25	690.24	0.431	7565.82	0.563

Figure 6 shows another way to compare the resistances and areas allocated to the coarse and fine ladders. In this figure, the area overhead associated with a non-optimal impedance/area allocation is shown where it is assumed that the total area must be increased to maintain the INL at the level obtained for optimal impedance/area allocation. When the area of the coarse string is equal $\frac{1}{10}$ of the total area, the total area increases 10% if the total resistance on fine string is $0.04R_C$, it increases by 50% if $R_F = R_C$, and it increased by more than 400% if $R_F = 10R_C$.

Although the area allocation in [3] was not directly given, a die photograph showed that the total area for the fine resistor string was approximately 7 times that for the coarse string. Assuming the fine area / coarse area ratio is also equal to 6.87, and the fine resistor / coarse resistor is equal to 38.4, we can characterize this layout by the parameters x= 0.13 z= 0.97. With these assumption, the area could be reduced by a factor of 7 with a near optimal allocation of x = 0.13, z = 0.13 while maintaining the same overall INL yield.

Correspondingly, Van de Plassche [5] suggested the coarse string area is "large", and discussed an impedance allocation of $R_C = 125\Omega$ and $R_F = 4800\Omega$. Although "large" is not quantitatively defined, if it is assumed that large means the area ratio of the coarse resistor array to that of the fine resistor array is large, one can make an assessment of the yield potential. As an example, if a large A_C / A_F ratio corresponds to 10 we can characterize the allocation strategy by the parameters x = 0.91 and z = 0.97. With this assumption, the area could be reduced by a factor of 1.05. With a near optimal allocation of x= 0.91, z = 0.91. Of course, if "large" were interpreted as some other ratio, the area reduction factor could be quite different.

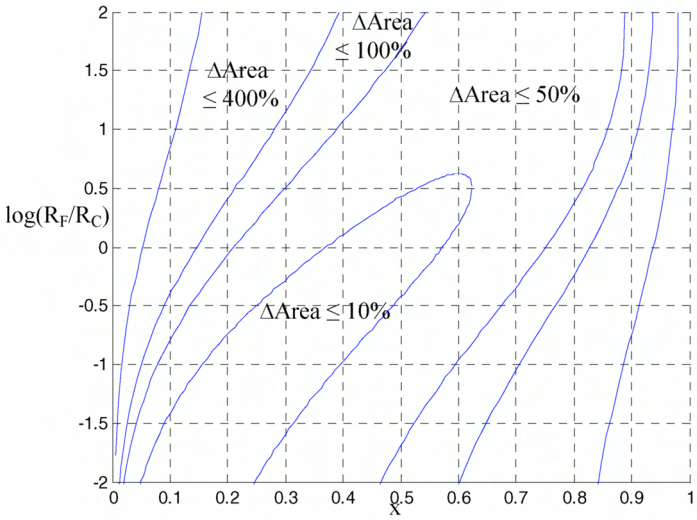

Figure 6. Effect of selection of impedance and area

V. CONCLUSIONS

In this paper, the effects of random variations in sheet resistance on the linearity performance of a dual-ladder resistor string DAC were analyzed. A formulation of the INL was presented. The relation between linearity, area allocation, and impedance allocation were discussed and optimal area and impedance allocation strategies were presented. It was shown that significant reductions in area or correspondingly improvement in yield can be obtained if an optimal area and impedance allocation strategy is adopted.

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