Analyses of Static and Dynamic Random Offset Voltages in Dynamic Comparators

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***Abstract*—When mismatches are present in a dynamic comparator, due to internal positive feedback and transient response, it is always challenging to analytically predict the input-referred random offset voltages since the operating points of transistors are time varying. In this paper, a novel balanced method is proposed to facilitate the evaluation of operating points of transistors in a dynamic comparator. Thus, it becomes possible to obtain an explicit expression for offset voltage in dynamic comparators. We include two types of mismatches in the model: 1) static offset voltages from the mismatch in μC_{ox} and threshold voltage V_{th} and 2) dynamic offset voltage due to the mismatch in the parasitic capacitances. From the analytical models, designers can obtain an intuition about the main contributors to offset and also fully explore the tradeoffs in dynamic comparator design, such as offset voltage, area and speed. To validate the balanced method, two topologies of dynamic comparator implemented in 0.25-μm and 40-nm CMOS technology are applied as examples. Input-referred offset voltages are first derived analytically based on SPICE Level 1 model, whose values are compared with more accurate Monte Carlo transient simulations using a sophisticated BSIM3 model. A good agreement between those two verifies the effectiveness of the balanced method. To illustrate its potential, the explicit expressions of offset voltage were applied to guide the optimization of "Lewis-Gray" structure. Compared to the original design, the input offset voltage was easily reduced by 41% after the optimization while maintaining the same silicon area.**

***Index Terms*—Dynamic comparators, dynamic offset voltage, Monte Carlo method, static offset voltage.**

I. Introduction

COMPARATORS have a crucial influence on the overall performance in high-speed analog-to-digital converters (ADCs) [1]. Since they are decision-making circuits that interface the analog and digital signals, the accuracy, which is often determined by its input-referred offset voltage, is essential for the resolution of high-performance ADCs [2]. Dynamic comparators are widely used in high-speed ADCs due to its low power consumption and fast speed. However, there is a lack of thorough and accurate analysis in the literatures regarding how to evaluate the input offset voltages analytically. Although there exist various offset cancellation circuits and digital calibration techniques [3], [4] , to apply such additional circuits to cancel offset voltages increases the power consumption and silicon area and lowers the overall speed. When the transistor feature size is scaled down, random offsets impact the yield of ADCs more severely [5]. Different from the offset caused by mismatch from the gradient effect, random offset cannot be relieved by any layout strategy [6]. In order to achieve an optimum dynamic comparator design, it is essential to have analytical methods to predict offset voltages, especially random offset voltages, and provide a deeper insight in the main offset contributors.

Neglecting error sources from external circuit, such as timing error and variation of reference voltages, the offset voltage in a dynamic comparator is mainly comprised of two types of mismatch: 1) static mismatch from variation in μC_{ox} and threshold voltage V_{th} and 2) dynamic mismatch from internal node parasitic capacitors' imbalance. In the literature, both of the mismatches are not well characterized.

First, the previous authors tend to analyze the static input offset voltage in a dynamic comparator in the same way as in the traditional operational amplifier [7]–[9]. The calculation of offset voltage in the operational amplifier (op-amp) based comparator is straightforward since the operation regions of all transistors are well defined. However, in dynamic comparators with an internal positive feedback, the previous method is not applicable since g_m and g_o of any transistor are time-dependent and not well defined. The authors fail to clearly state how to determine the value of transconductance g_m and output conductance g_o of the transistors at time-varying condition.

To overcome the difficulties in determining the operation regions and bias conditions of transistors in a dynamic comparator when the mismatch exists, we previously proposed a balanced method to calculate the static input offset voltage [10]. In this method, we first solve the bias point at comparison phase when the circuit is perfectly balanced without any mismatch. Then, if any mismatch is involved, we apply a compensation voltage ΔV_{in} at one of the input terminals to cancel the mismatch effect and ensure the comparator to reach the balanced status again. ΔV_{in} is the input-referred offset voltage. Its variance σ^2_{Vos} is regarded as the square of random offset voltage. Therefore, analytical expressions for static input offset voltage are derived and allow designers to focus on the most influential offset contributors. In very recent publication about thermal noise analysis in dynamic comparators [11], authors divided the transient process into three phases and performed noise analysis from stochastic differential equations in each time phase. However, in each phase, it is still not straightforward to determine the bias points for each transistor. In addition, utilizing the piece-wise linear method takes considerable effort and time.

Second, very little emphasis is placed on mismatch of internal parasitic capacitance. Although the feature size of transistors continues to be scaled down, the associated parasitic capacitance is not necessarily decreased due to the reduction of the

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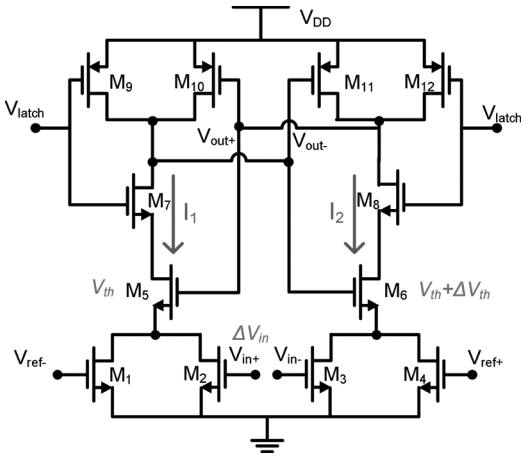

Fig. 1. "Lewis-Gray" structure.

oxide thickness and the junction depths [5]. In [12], [13] , the authors point out that 1-fF or 2-fF capacitance mismatch at the output can lead to offset of several tens of millivolts. Comparing with the absolute capacitance mismatch, our study finds that the relative capacitance mismatch defined as $\Delta C/C_n$ will more significantly affect input offset voltage. ΔC is the capacitor mismatch at differential nodes; C_n is nominal capacitance at those nodes.

This paper is organized as follows. In Section II, the balanced method is explained and applied to an example to analyze the static offset voltage from random mismatch in μC_{ox} and V_{th}; then, the dynamic offset voltage from internal capacitor mismatch is derived based on the similar approach. In Section III, our analytical results are compared with the more accurate Monte Carlo transient simulations. "Lewis-Gary" comparator implemented in 0.25-μm and 40-nm CMOS technology are built and analyzed. A good agreement between the simulated values and derived values shows the effectiveness of this balanced method. The derived analytical expressions provide deeper insights in the most dominant offset contributors and design tradeoffs. In Section IV, the analytical results are applied to guide the optimization of a dynamic comparator and easily reduce the offset voltage by 41% by resizing the transistors while maintaining a constant total area. In Section V, the method proposed in Section II is further verified by predicting offset voltage for another popular comparator topology built in 40 nm CMOS process. Section VI summaries the work.

II. Random Offset Voltage in Dynamic Comparators

We use the comparator architecture in Fig. 1 for our analysis. It is based on the structure reported in [14]. The so-called "Lewis-Gary" comparator is a widely used dynamic comparator in pipeline A/D converters. The method we proposed to evaluate offset voltage can be similarly extended to characterize offset in other dynamic comparators. In Section V, we applied the proposed method to another popular comparator topology introduced in [7] and developed its analytical model for offset voltage. The simulated results also show a good agreement between the derived results with Monte Carlo simulation results.

A. Static Offset Voltage From μC_{ox} and V_{th} Mismatches

A fully differential dynamic comparator will maintain a balanced state if no mismatch exists in the circuit. For static offset voltage, balanced state means that $V_{out+} = V_{out-}$; currents I_1 and I_2 in both branches are identical at all times during the transient process. The balanced state can be described by a space Φ_b comprised of power supplies, external bias voltage V_{latch} and comparison threshold or reference voltages V_{ref+} and V_{ref-} and transistor node voltages, which is written as $\Phi_b = \{V_{DD}, V_{latch}, V_{ref+}, V_{ref-}, V_{s5}$ or V_{s6}, V_{d5} or V_{d6}, V_{out+} or $V_{out-}\}$, in which the subscripts s and d mean source and drain voltage of transistor, respectively. When mismatch occurs, the circuit will lose its balance so that $V_{out+} \neq V_{out-}$. A voltage ΔV_{in} can be applied to compensate the mismatch effect and make V_{out+} equal to V_{out-}. This compensation voltage ΔV_{in} is the input offset voltage. The new balanced state Φ_{bn} is the same as Φ_b, because mismatches are small disturbances that will not change the bias condition of the comparator.

In order to calculate ΔV_{in}, node voltages at balanced state Φ_b need to be found and then are treated as the desired state when ΔV_{in} is applied to compensate mismatch. The chosen time point to calculate Φ_b is not important since under balanced condition node voltages for both branches are always symmetrical all the time. In this paper, the time point when the control signal V_{latch} reaches V_{DD} is chosen. Therefore, the operation regions of all of the transistors are well defined. Transistors of $M_1 - M_4$ connecting to the input and reference voltages are in the triode region and act like voltage-controlled resistors. M_{10} and M_{11} have equal drain and gate voltage, which makes them work at saturation region. M_7 and M_8 work as switches embedded in cross-coupled inverter pairs made of M_5M_{10} and M_6M_{11}. They are turned on during comparison phase and working in the triode region because of its high gate voltage $V_{g7,8} = V_{DD}$. The drain voltage of M_5 and M_6 is pulled up closed to V_{out+} or V_{out-} and works in saturation. M_9 and M_{12} are both turned off because control signal V_{latch} is V_{DD}, which indicates that mismatch effects in M_9 and M_{12} are negligible. Once the operation region for each transistor is known, combining with known power supply voltages, input voltages and process parameters, each node voltage in the dynamic comparator at balanced state can be readily solved.

If other time point for the analysis is chosen, for instance, when V_{latch} is half of the V_{DD}, the operation regions of M_7 and M_8 becomes unclear. In that situation, the operation regions need to be assumed first, and then verified by solving each node voltages under the balanced condition. Iteration may be necessary to find the operation region of M_7 and M_8.

In this paper, mismatch in μC_{ox} and threshold voltage V_{th} are assumed to be the dominant factors to cause the static offset voltage. First, mismatch between M_5 and M_6 is considered and other pairs are assumed to be perfectly matched. Since at the balanced state, by KCL, the current flowing through M_5 is the sum of currents in M_1 and M_2; the current in M_6 is sum of that in M_3 and M_4. The operation regions of the transistors $M_1 - M_4$ and $M_5 - M_6$ are well defined when the circuit is balanced and analyzed at $V_{latch} = V_{DD}$. $M_1 - M_4$ work as voltage control resistors and operate in triode region. M_5 and M_6 have the drain volt-

ages almost equal to $\mathrm{V_{out-}}$ and $\mathrm{V_{out+}}$, respectively, so they are in saturation. Applying square law model, the currents through $\mathrm{M_1}-\mathrm{M_4}$, $\mathrm{M_5}$ and $\mathrm{M_6}$ can be expressed as

$$I_{\mathrm{ds1}} = \mu_1 C_{\mathrm{ox}} \cdot \left(\frac{W_1}{L_1}\right) \cdot \left(V_{ref-} - V_{t1} - \frac{V_{ds1}}{2}\right) \cdot V_{\mathrm{ds1}} \quad (1)$$

$$I_{\mathrm{ds2}} = \mu_2 C_{\mathrm{ox}} \cdot \left(\frac{W_2}{L_2}\right) \cdot \left(V_{\mathrm{in+}} + \Delta V_{\mathrm{in}} - V_{t2} - \frac{V_{\mathrm{ds1}}}{2}\right) \cdot V_{\mathrm{ds1}} \quad (2)$$

$$I_{\mathrm{ds3}} = \mu_3 C_{\mathrm{ox}} \cdot \left(\frac{W_3}{L_3}\right) \cdot \left(V_{\mathrm{in-}} - V_{t3} - \frac{V_{\mathrm{ds3}}}{2}\right) \cdot V_{\mathrm{ds3}} \quad (3)$$

$$I_{\mathrm{ds4}} = \mu_4 C_{\mathrm{ox}} \cdot \left(\frac{W_4}{L_4}\right) \cdot \left(V_{\mathrm{ref+}} - V_{t4} - \frac{V_{\mathrm{ds3}}}{2}\right) \cdot V_{\mathrm{ds3}} \quad (4)$$

$$I_{\mathrm{ds5}} = \frac{\mu_5 C_{\mathrm{ox}}}{2} \cdot \frac{W_5}{L_5} \cdot (V_{\mathrm{out+}} - V_{s5} - V_{t5})^2 \quad (5)$$

$$I_{\mathrm{ds6}} = \frac{\mu_6 C_{\mathrm{ox}}}{2} \cdot \frac{W_6}{L_6} \cdot (V_{out-} - V_{s6} - V_{t6})^2. \quad (6)$$

When $\mu \mathrm{C_{ox}}$ and threshold voltage $\mathrm{V_{th}}$ has mismatch between $\mathrm{M_5}$ and $\mathrm{M_6}$, they can be expressed in terms of a nominal part and a variation part. Since μ and $\mathrm{C_{ox}}$ are always in a form of product, the combined variation can be regarded as the only variation in mobility μ for the convenience of calculation

$$\mu_5 = \mu_n + \Delta\mu_5 \quad (7)$$

$$\mu_6 = \mu_n + \Delta\mu_6 \quad (8)$$

$$V_{t5} = V_{tn} + \Delta V_{t5} \quad (9)$$

$$V_{t6} = V_{tn} + \Delta V_{t6} \quad (10)$$

where μ_{n} and $\mathrm{V_{tn}}$ are the nominal values of nMOS mobility and threshold voltage, respectively. $\Delta\mu_5$ and $\Delta\mu_6$ are the mobility variations for $\mathrm{M_5}$ and $\mathrm{M_6}$. $\Delta \mathrm{V_{t5}}$ and $\Delta \mathrm{V_{t6}}$ are the variations in threshold voltages of $\mathrm{M_5}$ and $\mathrm{M_6}$, respectively.

As a compensation voltage to ensure the comparator work at balanced condition Φ_{b}, ΔV_{in} is the offset voltage V_{os_M5M6} caused by mismatch between $\mathrm{M_5}$ and $\mathrm{M_6}$. It can be written as function of mobility μ and threshold voltage $\mathrm{V_{th}}$ based on (1)–(10) as follows:

$$V_{os\_M5M6} = \frac{(\mu_n + \Delta\mu_5)\left(\frac{W_5}{W_1}\right)}{2\mu_n V_{s5}} \times (V_{out+} - V_{s5} - V_{tn} - \Delta V_{t5})^2 - \frac{(\mu_n + \Delta\mu_6)\left(\frac{W_6}{W_1}\right)}{2\mu_n V_{s6}} \times (V_{out-} - V_{s6} - V_{tn} - \Delta V_{t6})^2 \quad (11)$$

where $\mathrm{V_{out+}}$, $\mathrm{V_{out-}}$, V_{s5}, and V_{s6} are solved node voltages at balanced state Φ_{b} and $\mathrm{V_{out+}} = \mathrm{V_{out-}}$, $\mathrm{V}_{s5} = \mathrm{V}_{s6}$. For matching purposes, all of the transistors are sized to have the same channel length L, and the four input transistors $\mathrm{M_1}-\mathrm{M_4}$ are sized in the same dimensions.

In the practical application, the variation part ΔV_t and $\Delta\mu$ is normally very small compared with the nominal component if reasonable yield are to be guaranteed [6]. Therefore, it can be derived that offset voltage from $\mathrm{M_5M_6}$ mismatch can be approximated in the expression

$$V_{os\_M5M6} \approx K_{VT5} \cdot \Delta V_{t5} + K_{VT6} \cdot \Delta V_{t6} + K_{\mu 5} \cdot \frac{\Delta\mu_5}{\mu_n} + K_{\mu 6} \cdot \frac{\Delta\mu_6}{\mu_n} \quad (12)$$

where

$$K_{VT5} = -\frac{V_{out+} - V_{s5} - V_{tn}}{V_{s5}} \cdot \frac{W_5}{W_1} \quad (13)$$

$$K_{VT6} = \frac{V_{\mathrm{out-}} - V_{s6} - V_{tn}}{V_{s6}} \cdot \frac{W_6}{W_1} \quad (14)$$

$$K_{\mu 5} = \frac{(V_{\mathrm{out+}} - V_{s5} - V_{tn})^2}{2 \cdot V_{s5}} \cdot \frac{W_5}{W_1} \quad (15)$$

$$K_{\mu 6} = -\frac{(V_{\mathrm{out-}} - V_{s6} - V_{tn})^2}{2 \cdot V_{s6}} \cdot \frac{W_6}{W_1}. \quad (16)$$

In BSIM3 and BSIM4 model, mobility μ and threshold voltage $\mathrm{V_{th}}$ have a weak correlation in high-order terms [15], [16]. To simplify the derivation, we assume that μ and $\mathrm{V_{th}}$ are uncorrelated with each other and have a nearly Gaussian distribution. It is well known that the linear combination of Gaussian random variables is Gaussian [6]. Random offset voltage caused by mismatch from $\mathrm{M_5}$ and $\mathrm{M_6}$ can be derived from the variance of (12) to yield

$$\sigma^2_{V_{OS\_M5M6}} = K^2_{VT5} \cdot \sigma^2_{V_{t5}} + K^2_{VT6} \cdot \sigma^2_{V_{t6}} + K^2_{\mu_5} \cdot \sigma^2_{\mu_5/\mu_n} + K^2_{\mu_6} \cdot \sigma^2_{\mu_6/u_n} \quad (17)$$

where K^2_{VT5}, K^2_{VT6}, $K^2_{\mu 5}$, and $K^2_{\mu 6}$ have been expressed in (13)–(16). Similarly, input random offset voltages caused by mismatch of the other pairs can also be found as follows. Random offset from mismatch between $\mathrm{M_1}$ and $\mathrm{M_4}$ is

$$\sigma^2_{V_{os\_M1M4}} = \sigma^2_{V_{t1}} + \sigma^2_{V_{t4}} + (V_{\mathrm{ref+}} - V_{tn})^2 \cdot \sigma^2_{V_{\mu_4/\mu_n}} + (V_{\mathrm{ref-}} - V_{tn})^2 \cdot \sigma^2_{V_{\mu_1/\mu_n}}. \quad (18)$$

Random offset from mismatch between $\mathrm{M_2}$ and $\mathrm{M_3}$ is

$$\sigma^2_{V_{os\_M2M3}} = \sigma^2_{V_{t2}} + \sigma^2_{V_{t3}} + (V_{\mathrm{in+}} - V_{tn})^2 \cdot \sigma^2_{V_{\mu_2/\mu_n}} + (V_{\mathrm{in-}} - V_{tn})^2 \cdot \sigma^2_{V_{\mu_3/\mu_n}}. \quad (19)$$

Random offset from mismatch between $\mathrm{M_{10}}$ and $\mathrm{M_{11}}$ is

$$\sigma^2_{V_{os\_M10M11}} = \frac{(V_{\mathrm{DD}} - V_{\mathrm{out+}} - V_{tp})^2}{9V^2_{s5}} \sigma^2_{V_{t10}} + \frac{(V_{\mathrm{DD}} - V_{\mathrm{out+}} - V_{tp})^2}{9V^2_{s6}} \cdot \sigma {V_{t11}}^2 + \frac{(V_{\mathrm{DD}} - V_{\mathrm{out+}} - V_{tp})^4}{36 \cdot V^2_{s5}} \sigma^2_{\mu_{10}/\mu_p} + \frac{(V_{\mathrm{DD}} - V_{\mathrm{out+}} - V_p)^4}{36 \cdot V^2_{s6}} \sigma^2_{\mu_{11}/\mu_p}. \quad (20)$$

Random offset from mismatch between M7 and M8 is

$$\begin{aligned}\sigma^2_{V_{os\_M7M8}} &= \left(\frac{W_7}{W_2}\cdot\frac{V_{\rm ds7}}{V_{s5}}\right)^2\cdot\sigma^2_{V_{t7}} \\ &+\left(\frac{W_8}{W_2}\cdot\frac{V_{\rm ds8}}{V_{s5}}\right)^2\cdot\sigma^2_{V_{t8}}+\left(\frac{W_7}{W_2}\cdot\frac{V_{\rm ds7}}{V_{s5}}\right)^2 \\ &\cdot\left(V_{\rm latch}-V_{d5}-V_{tn}-\frac{V_{\rm ds7}}{2}\right)^2\cdot\sigma^2_{V_{\mu_7/\mu_n}} \\ &+\left(\frac{W_8}{W_2}\cdot\frac{V_{\rm ds8}}{V_{s5}}\right)^2 \\ &\cdot\left(V_{\rm latch}-V_{d6}-V_{tn}-\frac{V_{\rm ds8}}{2}\right)^2\cdot\sigma^2_{V_{\mu_8/\mu_n}} \quad (21)\end{aligned}$$

where $\mathrm{V_{tp}}$ is the nominal value for the threshold voltage of pMOS; $\sigma^2_{\rm Vti}$, $\sigma^2_{\mu i/\mu n}$, and $\sigma^2_{\mu i/\mu p}(\mathrm{i}=1,2\ldots11)$ characterize random mismatch in threshold voltage and mobility of nMOS and pMOS transistors, which can be modeled as follows [5], [17]:

$$\sigma^2_{V_t}=\frac{A^2_{V_t}}{W\cdot L}+S^2_{V_{T0}}\cdot D^2 \quad (22)$$

$$\sigma^2_{\mu_i/\mu_n}=\frac{A^2_{\mu}}{W\cdot L}+S^2_{\mu}\cdot D^2 \quad (23)$$

where W and L are the width and length of the transistor pair. A_{vt}, A_β, S^2_{VT0}, and S^2_μ are process-dependent parameters and S^2_{VT0} and S^2_μ describe the variation of V_{T0} and μ with the spacing. D is the distance on chip between the matching transistors, which will be neglected because of its minor contribution to the overall mismatch.

If the random mismatches in each pair are uncorrelated or nearly uncorrelated, the overall static random offset voltage σ_{Vos} from mismatch in $\mu\mathrm{C_{ox}}$ and threshold voltage $\mathrm{V_{th}}$ in the dynamic comparator can be described as follows:

$$\sigma^2_{V_{os}}=\left(\sigma^2_{V_{os\_M5M6}}+\sigma^2_{V_{os\_M1M4}}+\sigma^2_{V_{os\_M2M3}}+\sigma^2_{V_{os\_M7M8}}+\sigma^2_{V_{os\_M10M11}}\right)^{1/2}. \quad (24)$$

Static random offset resulting from mismatch between $\mathrm{M_9}$ and $\mathrm{M_{12}}$ are neglected in the calculation, because they work as switches during the reset state to pull up differential output to $\mathrm{V_{DD}}$, and then are turned off during the comparison stage.

From offset expressions (17) to (21), we can have the following conclusions about the comparator in Fig. 1:

- Static random offset voltages caused by mismatch in transistors pairs of $\mathrm{M_1}$ and $\mathrm{M_4}$, $\mathrm{M_2}$ and $\mathrm{M_3}$ can be reduced by increasing the size of those transistors, because $\sigma^2_{\rm Vti}$ and $\sigma^2_{\mu i/\mu n}(\mathrm{i}=1,2,3,4)$ are inversely proportional to the product of W and L.
- Random offset voltages caused by mismatch in transistors pairs of $\mathrm{M_5}$ and $\mathrm{M_6}$, $\mathrm{M_7}$ and $\mathrm{M_8}$ can not be guaranteed to be reduced when the sizes of the transistors are increased since the widths also appear in the numerator of the (13)–(16) and (21).

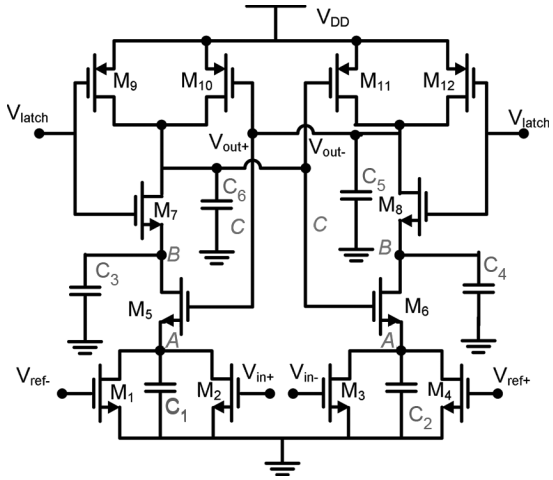

Fig. 2. "Lewis-Gray" structure with internal paracitic capacitors.

- A particular aspect ratio W/L can be found to make an optimum tradeoff between random offset voltage and transistor size denoted by the product of W and L, which is discussed in detail in Section IV.

B. Dynamic Offset Voltage From Internal Capacitor Mismatch

Distinguished from mismatch caused by $\mu\mathrm{C_{ox}}$ and threshold voltage $\mathrm{V_{th}}$, the effects of parasitic capacitance mismatch are shown only during transient process and therefore called dynamic offset. A four-terminal MOS device includes twelve different parasitic capacitors [16]. For a matched pair in the dynamic comparator, any dimension mismatch due to process variation and asymmetric interconnection will cause capacitance mismatch. It has been demonstrated that a 1fF capacitance mismatch at the output node may contribute several tens of millivolts of input-referred offset voltage [13]. For a simple two-inverter latch structure, the authors in [13] have shown analytically the derivation of input referred offset voltage. For the more complicated dynamic comparator as shown in Fig. 2, an accurate analysis like what they proposed will be very tedious.

As shown in Fig. 2, $\mathrm{C_5}$ and $\mathrm{C_6}$ contain all of the parasitic capacitance from $\mathrm{V_{out-}}$ and $\mathrm{V_{out+}}$ to ground, respectively. An accurate analysis to calculate the offset voltage due to capacitor mismatch in the dynamic comparator is tedious since we have to consider the transient current and voltage due to capacitance charge and discharge.

By using the balanced method, a simple formula to calculate the input referred offset voltage due to $\mathrm{C_5}$ and $\mathrm{C_6}$ mismatch using square law model is derived as follows. In order to calculate the offset voltage, a DC voltage $\mathrm{V_{OS,C56}}$ is virtually added to $\mathrm{V_{in+}}$ terminal. When the comparator is balanced, $\mathrm{V_{out+}}$ and $\mathrm{V_{out-}}$ are equal and $d\mathrm{V_{out+}}/dt$ and $d\mathrm{V_{out-}}/dt$ are equal. The time point to calculate the dynamic offset voltage is chosen at when $\mathrm{M_{10}}$ and $\mathrm{M_{11}}$ are about to be turned on.

Therefore, the compensation dc voltage $\mathrm{V_{OS,C56}}$ is the input-referred dynamic offset voltage. To make the formula more readable, we assume that the transient currents through the parasitic capacitance except $\mathrm{C_5}$ and $\mathrm{C_6}$ are negligible. Then the following equations can be written:

$$C_5\frac{dV_{\rm out-}}{dt}=I_{\rm ds1}+I_{\rm ds2} \quad (25)$$

TABLE I
KEY VALUES FOR THE DYNAMIC COMPARATOR IN 0.25 μm

Process	0.25μm CMOS
Power supply	V_{DD}=1.5V, V_{ss}=0V
Transistor sizing	$(W/L)_{1,2,3,4}$=(1.5u/0.45u)x4
	$(W/L)_{5,6,7,8}$=(3.5u/0.45u)x4
	$(W/L)_{10,11}$=(1.5u/0.45u)x4
V_{ref}	V_{ref+}=1.6V, V_{ref-}=1.2V
Clock signal V_{latch}	High=1.5V;Low=0V
	Rise and fall time = 10ps
	Pulse width=20ns; Freq=10MHz
Switch (PMOS)	$(W/L)_{9,12}$=1.5u/0.45u

TABLE II
KEY VALUES FOR THE DYNAMIC COMPARATOR IN 40 NM

Process	40nm CMOS
Power supply	V_{DD}=1.0V, V_{ss}=0V
Transistor sizing	$(W/L)_{1,2,3,4}$=(0.16u/0.05u)x4
	$(W/L)_{5,6,7,8}$=(0.38u/0.05u)x4
	$(W/L)_{10,11}$=(0.16u/0.05u)x4
V_{ref}	V_{ref+}=0.8V, V_{ref-}=0.6V
Clock signal V_{latch}	High=1.0V;Low=0V
	Rise and fall time = 1ps
	Pulse width=500ps; Freq=1GHz
Switch (PMOS)	$(W/L)_{9,12}$=0.16u/0.05u

$$C_6\frac{dV_{\text{out}+}}{dt} = I_{\text{ds3}} + I_{\text{ds4}} \tag{26}$$

$$\frac{dV_{\text{out}+}}{dt} = \frac{dV_{out-}}{dt}. \tag{27}$$

From (25)–(27), it follows that

$$\frac{I_{\text{ds1}} + I_{\text{ds2}}}{C_5} = \frac{I_{\text{ds3}} + I_{\text{ds4}}}{C_6}. \tag{28}$$

Applying the square-law model to replace the drain source current in (28), the input-referred dynamic offset $V_{os,C56}$ due to mismatch in C_5 and C_6 is derived as

$$V_{os,C56} = \frac{\Delta C_{56}}{C_6}\frac{I_{\text{ds3}} + I_{\text{ds4}}}{\mu_n C_{\text{ox}}\frac{W_2}{L_2}V_{ds1}} \tag{29}$$

where $\Delta C_{56} = C_5 - C_6$.

From (29), it's shown that the dynamic offset voltage is more affected by the relative capacitance mismatch $\Delta C_{56}/C_6$ than just the absolute capacitance mismatch ΔC_{56}. If the relative capacitance mismatch is decreased at output nodes, the input referred offset voltage will be reduced. A possible strategy to minimize the dynamic offset voltage is increasing the transistor area of M_5M_6 pair so that the relative mismatch is reduced. Moreover, if the comparator speed requirement can be easily met, some precision capacitors with very good matching properties can be added at the output nodes to further shrink the relative capacitor mismatch. The Monte Carlo simulations in Section III confirm the above conclusions.

III. NUMBERICAL EXAMPLES AND MONTE CARLO SIMULATION RESULTS

The previous analysis is validated with simulations results in this section. The "Lewis-Gary" comparator is implemented in 0.25-μm and 40-nm CMOS process. The key values are listed in Tables I and II. For better matching purposes, transistor length is chosen to be the same within each process.

A. Simulations Results for Static Offset Voltage

First, all node voltages are solved when no mismatch is presented. The bias conditions at balanced state Φ_b can be determined. In 0.25 μm comparator, it can be calculated that: $V_{\text{out}+} = V_{\text{out}-} = 0.601$ V, $V_{d5} = V_{d6} = 0.585$ V, $V_{s5} = V_{s6} = 0.0089$ V. In 40 nm comparator, the bias condition is calculated as: $V_{\text{out}+} = V_{\text{out}-} = 0.458$ V, $V_{d5} = V_{d6} = 0.439$ V, $V_{s5} = V_{s6} = 0.0129$ V. Then, the calculated node voltages are applied to (17)–(21) to find numerical value for random offset caused by mismatch due to process variation in each pair. A_{vt} and A_μ in σ_{Vt} and $\sigma_{\mu i/\mu n}$ are process-dependent parameters, whose values for different processes are listed as a reference in Table III [5].

TABLE III
MISMATCH PARAMETER FOR SEVERAL CMOS TECHNOLOGIES

Technology	Type	A_{vt}(mV·μm)	A_β(%·μm)
2.5 μm	NMOS	30	2.3
	PMOS	35	3.2
1.2 μm	NMOS	21	1.8
	PMOS	25	4.2
0.7 μm	NMOS	13	1.9
	PMOS	22	2.8
0.5 μm	NMOS	11	1.8
	PMOS	13	2.3
0.35 μm	NMOS	9	1.9
	PMOS	9	2.25
0.25 μm	NMOS	6	1.85
	PMOS	6	1.85
40 nm	NMOS	1.8	0.45
	PMOS	1.7	0.68

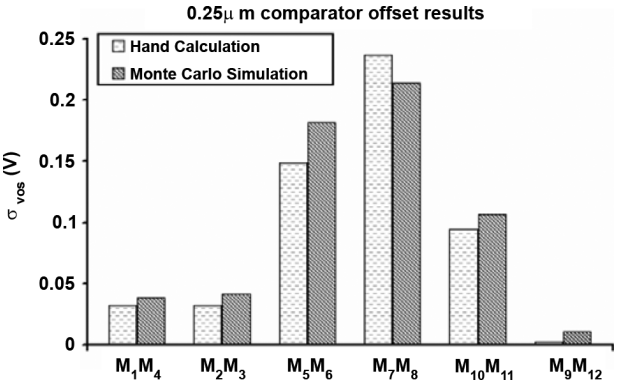

Fig. 3. Comparison between analytical results and Monte Carlo simulation for each pair in a 0.25-μm comparator.

Monte Carlo transient simulation is performed by using the BSIM3 model. In the model file, the mobility μ_n and threshold voltage V_{th} are defined as Gaussian distributed variables with a standard deviation modeled by (22) and (23). One hundred iterations are done for each pair while assuming no mismatch exists in other pairs so that $\sigma_{\text{Vos\_M1M4}}$, $\sigma_{\text{Vos\_M2M3}}$, $\sigma_{\text{Vos\_M5M6}}$, $\sigma_{\text{Vos\_M7M8}}$, $\sigma_{\text{Vos\_M10M11}}$, and $\sigma_{\text{Vos\_M9M10}}$ can be determined one by one. In Figs. 3 and 4, the random offset voltage calculated by the analytical method shows a good agreement with the Monte Carlo simulation results. From the plot, we can easily tell the most influential offset contributors.

B. Simulations Results for Dynamic Offset Voltage

In Section II, the explicit expression of dynamic offset voltage due to capacitance mismatch at the output nodes has been de-

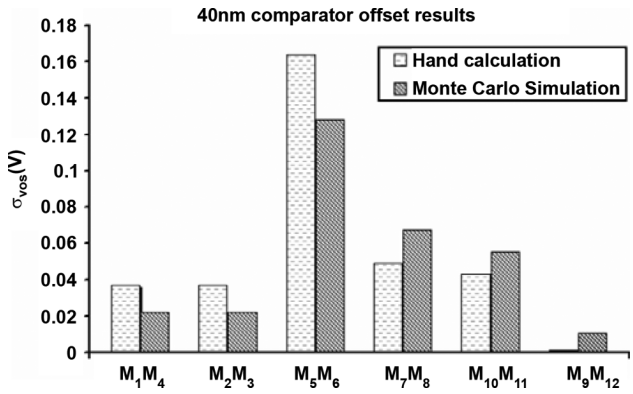

Fig. 4. Comparison between analytical results and Monte Carlo simulation for each pair in a 40-nm comparator.

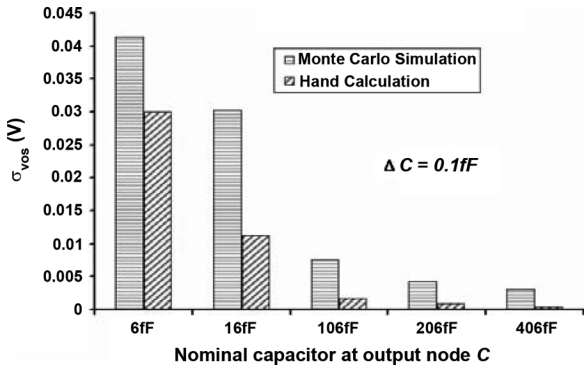

Fig. 5. Comparison of dynamic offset voltages due to $\mathrm{C}_{5,6}$ mismatch derived by analytical model and Monte Carlo simulation.

rived in (29). To demonstrate its effectiveness, Monte Carlo transient simulations are conducted based upon the comparator described in Table I. As we have predicted from the analytical model, it is the relative capacitance mismatch $\Delta\mathrm{C}/\mathrm{C_n}$ than just the absolute mismatch $\Delta\mathrm{C}$ that plays a key role in determining the dynamic offset voltage. As shown in Fig. 5, it is clear that as the output nominal capacitance is increasing but the absolute mismatch capacitance is kept as a constant 0.1fF, the dynamic offset is decreasing. The calculated and simulated dynamic offset voltages show a reasonable agreement.

For the dynamic comparator illustrated in Fig. 2, the contributions to offset voltage from parasitic capacitors at different nodes are usually different. In order to compare the effects of the capacitance mismatch at different nodes, the mismatch capacitor $\Delta\mathrm{C}$ is added to one of the three nodes A, B and C and the relative capacitance mismatch is kept to be 1.67%. The Monte Carlo simulation demonstrates that capacitance mismatch at the output node C accounts for 76% overall dynamic offset voltage. The capacitance mismatch of $\mathrm{C}_{1,2}$ and $\mathrm{C}_{3,4}$ contributes the remaining dynamic offset voltage. It shows that capacitor mismatch at output node is the most influential contributor to the dynamic offset.

To probe more, we further investigate the capacitor mismatch at differential nodes A and B. As reported in Fig. 6, when the nominal capacitance at differential node A, B increases, the dynamic offset voltages increase. The results are predictable since a larger capacitor will dump larger transient currents to ground. The transient currents flow through input pairs $\mathrm{M}_{2,3}$ are reduced

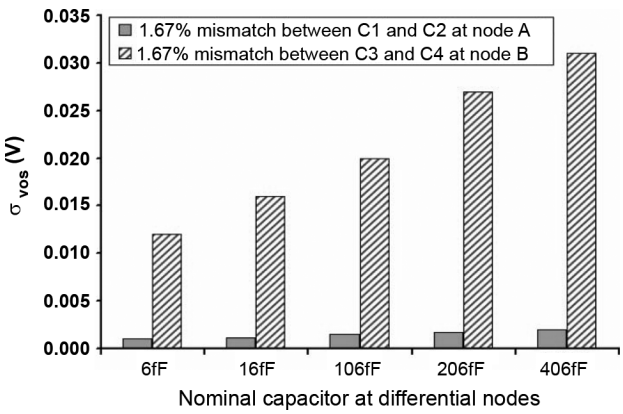

Fig. 6. Dynamic offsets from $\mathrm{C}_1\&\mathrm{C}_2$ and $\mathrm{C}_3\&\mathrm{C}_4$ mismatch.

as a result. To cancel the effects of capacitance mismatch in differential nodes, a larger input voltage ΔV_{in} is required to compensate the mismatch. It suggests that the internal capacitance at nodes A and B should be kept as small as possible.

IV. One Application of the Random Offset Analytical Model

Without any offset cancellation technique, a dynamic comparator will not easily achieve input offset voltage less than several tens of millivolts. Mismatch caused by random variations cannot be relieved from any layout strategy. From pervious sections, it is indicted that by symmetric layout, well-balanced routing and extra balanced capacitive loading, the dynamic mismatch at sensitive nodes-output nodes can be reduced. By contrast, it seems more difficult for designers to control the random mismatch from $\mu\mathrm{C_{ox}}$ and $\mathrm{V_{th}}$. As a matter of fact, by utilizing the analytical model in the analytical model in (17)–(21), the static random offset voltage can be reduced by proper sizing without increasing the total area of the comparator.

The following procedures are applied to find the proper sizes to achieve smaller random offset voltage given a fixed total area.

1) Based on the analytical results in (17)–(21), the input random offset voltage due to each transistor pair can be calculated. Then, all of the transistor pairs are divided into several groups following the rule that in each group there contains both a critical matching pair and uncritical pairs.
2) First focus on the mismatch in one group and assume there is no mismatch in the other groups. Based on the conclusion from Section II, a minimum random offset voltage can be found by properly adjusting the sizes of the transistor pairs depending on their contributions to the offset voltages. Apply the same procedure to the remaining groups to achieve minimum random offset in each group.

Apply the above procedure to the comparator example described in Table I. Based on the calculated offset voltage from each transistor pair, six pairs of transistors are divided into two groups. Group 1 is composed of bottom four uncritical matching transistor pairs $\mathrm{M}_1 - \mathrm{M}_4$ and critical matching transistor pairs $\mathrm{M_7M_8}$. Group 2 includes the four uncritical matching pMOS transistors $\mathrm{M}_9 - \mathrm{M}_{12}$ and critical matching nMOS pairs $\mathrm{M_5M_6}$.

First, group 1 is optimized. The area budget is moved from $\mathrm{M}_1 - \mathrm{M}_4$ to $\mathrm{M_7M_8}$ by increasing width of $\mathrm{M_7M_8}$ at a step size

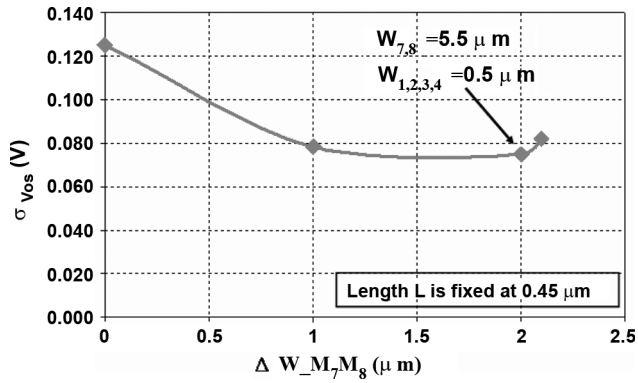

Fig. 7. Random offset versus ΔW of matching critical pair M_7M_8.

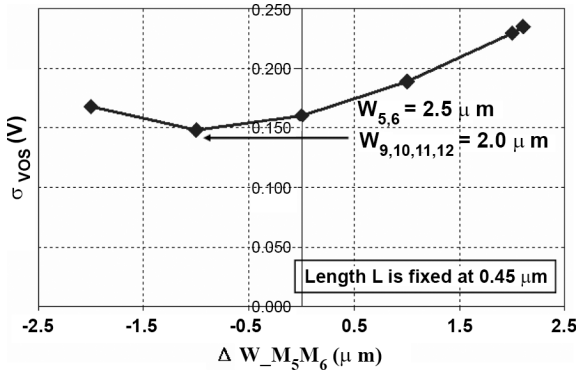

Fig. 8. Random offset versus ΔW of matching critical pair M_5M_6.

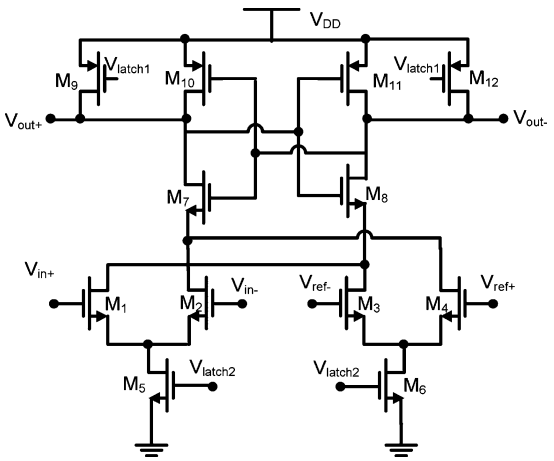

Fig. 9. Topology II dynamic comparator.

of 0.5 μm while the total area in the group is maintained as a constant. The simulated random offset voltage versus width change in M_7M_8 denoted by ΔW_M_7M_8 is shown in Fig. 7. It is shown that when ΔW_M_7M_8 is equal to 2 μm, which means the widths of M_7M_8 are increased from 3.5 μm to 5.5 μm and widths of $M_1 - M_4$ are decreased from 1.5 μm to 0.5 μm. The random offset voltage reaches the minimum value 78.3 mV within group 1. The similar area allocation procedure is applied to group 2 made of M_5M_6 and $M_9 - M_{12}$. The simulated random offset versus ΔW of M_5M_6 is shown in Fig. 8. Finally, the sizes are optimized and listed in Table IV.

After this optimization, Monte Carlo simulation is applied with mismatch presented in all the pairs, and the overall random

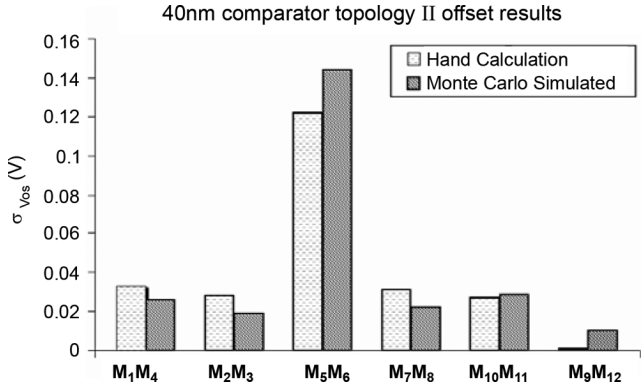

Fig. 10. Comparison between analytical results and Monte Carlo simulation for each pair in 40 nm comparator in Fig. 9.

TABLE IV
DIMENSIONS AND RANDOM OFFSET COMPARISON

Name	Original sizes (μm/ μm)	Optimized sizes (μm/ μm)
M_1M_3	1.5/0.45	0.5/0.45
M_2M_4	1.5/0.45	0.5/0.45
M_5M_6	3.5/0.45	2.5/0.45
M_7M_8	3.5/0.45	5.5/0.45
$M_{10}M_{11}$	1.5/0.45	2.0/0.45
M_9M_{12}	1.5/0.45	2.0/0.45
σ_{Vos}	*254 mV*	*150 mV*

offset voltage is 150 mV, which is reduced by 41% compared with 254 mV in the original sizing. The total area is still kept as a constant.

V. Model Validation in Comparator Topology II

To further validate the effectiveness of our method in Section II, here we present another dynamic comparator topology and apply the method to analyze its offset. The topology is first introduced in [7].

The operation of the comparator can be simply described as follows. When latch signal reaches zero, M_5 and M_6 are turned off and current paths are cut off. M_9 and M_{12} reset the differential output to V_{DD}. When latch signal is raised high, differential output nodes are disconnected from V_{DD}. Depending on the difference between input voltage and reference voltage, cross coupled inverter pairs made of M_7M_{10} and M_8M_{11} regeneratively amplify the difference and determine which of the outputs goes to V_{DD} and which to 0 V.

As detailed in Section II, to find out the offset voltage from mismatch in μC_{ox} and threshold voltage V_{th}, we will first determine the bias conditions at perfectly balanced condition. We choose $V_{latch} = V_{DD}$ as the time point for analysis. M_7, M_8, M_{10} and M_{11} all have the same gate and drain voltages since $V_{out+} = V_{out-}$ at balanced state. Therefore, they are working in the saturation region. M_5 and M_6 work as tail current sources. They are supported to be working in saturation to eliminate large offset due to the mismatch [8]. To avoid M_5 and M_6 goes into triode when latch signal goes high, instead of using the clock

going from 0 to V_{DD}, a lower voltage clock V_{latch2} is used to guarantee that M_5 and M_6 remain in saturation [12]. $M_1 - M_4$ are in triode region and act like voltage-controlled resistors.

Once the operation regions are determined, by KCL, we can calculate offset voltage caused by each pair in the comparator. Random offset from mismatch between M_2 and M_3 is

$$\begin{aligned}\sigma^2_{V_{os\_M2M3}} &= \sigma^2_{V_{t2}} + \sigma^2_{V_{t3}} \\ &\quad + (V_{\text{in}-} - V_{d5} - V_{tn} - \frac{V_{\text{ds2}}}{2})^2 \cdot \sigma^2_{V_{\mu_2/\mu_n}} \\ &\quad + (V_{\text{ref}-} - V_{d6} - V_{tn} - \frac{V_{\text{ds3}}}{2})^2 \cdot \sigma^2_{V_{\mu 3/\mu_n}}. \quad (30)\end{aligned}$$

Random offset from mismatch between M_1 and M_4 is

$$\begin{aligned}\sigma^2_{V_{os\_M1M4}} &= \sigma^2_{V_{t1}} + \sigma^2_{V_{t4}} \\ &\quad + (V_{\text{in}+} - V_{d5} - V_{tn} - \frac{V_{\text{ds1}}}{2})^2 \cdot \sigma^2_{V_{\mu 1/\mu_n}} \\ &\quad + (V_{\text{ref}+} - V_{d6} - V_{tn} - \frac{V_{\text{ds4}}}{2})^2 \cdot \sigma^2_{V_{\mu 4/\mu_n}}. \quad (31)\end{aligned}$$

Random offset from mismatch between M_5 and M_6 is

$$\begin{aligned}\sigma^2_{V_{os\_M5M6}} &= \left(\frac{W_5}{W_1}\right)^2 \frac{(V_{\text{latch2}} - V_{tn})^2}{V^2_{\text{ds1}}} \sigma^2_{V_{t5}} \\ &\quad + \left(\frac{W_6}{W_1}\right)^2 \frac{(V_{\text{latch2}} - V_{tn})^2}{V^2_{\text{ds1}}} \sigma^2_{V_{t6}} \\ &\quad + \left(\frac{W_5}{W_1}\right)^2 \frac{(V_{\text{latch2}} - V_{tn})^4}{4 \cdot V^2_{\text{ds1}}} \sigma^2_{\mu_5/\mu_n} \\ &\quad + \left(\frac{W_6}{W_1}\right)^2 \frac{(V_{\text{latch2}} - V_{tn})^4}{4 \cdot V^2_{\text{ds1}}} \sigma^2_{\mu_6/\mu_n}. \quad (32)\end{aligned}$$

Random offset from mismatch between M_7 and M_8 is

$$\begin{aligned}\sigma^2_{V_{os\_M7M8}} &= \left(\frac{W_8}{W_1}\right)^2 \frac{(V_{\text{out}} - V_{s8} - V_{tn})^2}{V^2_{\text{ds1}}} \sigma^2_{V_{t8}} \\ &\quad + \left(\frac{W_7}{W_1}\right)^2 \frac{(V_{\text{out}+} - V_{s7} - V_{tn})^2}{V^2_{ds1}} \sigma^2_{V_{t7}} \\ &\quad + \left(\frac{W_8}{W_1}\right)^2 \frac{(V_{\text{out}-} - V_{s8} - V_{tn})^4}{4 \cdot V^2_{\text{ds1}}} \sigma^2_{\mu_8/\mu_n} \\ &\quad + \left(\frac{W_7}{W_1}\right)^2 \frac{(V_{\text{out}+} - V_{s7} - V_{tn})^4}{4 \cdot V^2_{\text{ds1}}} \sigma^2_{\mu_7/\mu_n}. \quad (33)\end{aligned}$$

Random offset from mismatch between M_{10} and M_{11} is

$$\begin{aligned}\sigma^2_{V_{os\_M10M11}} &= \left(\frac{W_{10}}{W_1}\right)^2 \frac{(V_{\text{DD}} - V_{\text{out}+} - V_{tn})^2}{4 \cdot V^2_{\text{ds1}}} \sigma^2_{V_{t10}} \\ &\quad + \left(\frac{W_{11}}{W_1}\right)^2 \frac{(V_{\text{DD}} - V_{\text{out}-} - V_{tn})^2}{4 \cdot V^2_{\text{ds1}}} \sigma^2_{V_{t11}} \\ &\quad + \left(\frac{W_{10}}{W_1}\right)^2 \frac{(V_{\text{DD}} - V_{\text{out}+} - V_{tn})^4}{16 \cdot V^2_{\text{ds1}}} \sigma^2_{\mu_{10}/\mu_n} \\ &\quad + \left(\frac{W_{11}}{W_1}\right)^2 \frac{(V_{\text{DD}} - V_{\text{out}-} - V_{tn})^4}{16 \cdot V^2_{\text{ds1}}} \sigma^2_{\mu_{11}/\mu_n}. \quad (34)\end{aligned}$$

TABLE V
KEY VALUES FOR COMPARATOR II IN 40 NM

Process	40nm CMOS
Power supply	V_{DD}=1.0V, V_{ss}=0V
Transistor sizing	$(W/L)_{1,2,3,4,5,6}$=(0.16u/0.05u)x4
	$(W/L)_{7,8}$=(0.38u/0.05u)x4
	$(W/L)_{10,11}$=(0.16u/0.05u)x4
V_{ref}	V_{ref+}=0.8V, V_{ref-}=0.6V
Clock signal V_{latch}	V_{latch1} High=1.0V;Low=0V V_{latch2} High=0.4V; Low=0V
	Rise and fall time = 1ps
	Pulse width=500ps; Freq=1GHz
Switch (PMOS)	$(W/L)_{9,12}$=0.16u/0.05u

The topology II dynamic comparator implemented in 40 nm operates at 1.0 GHz clock frequency with a 1.0-V power supply. Table V shows key design parameters. The bias condition at each node is solved as: $V_{\text{out}+} = V_{\text{out}-} = 0.579$ V, $V_{s7} = V_{s8} = 0.193$ V, $V_{d5} = V_{d6} = 0.179$ V. Then, the calculated node voltages are applied to (30)–(34) to find numerical value for random offset caused by mismatch due to process variation in each pair. The calculated values are plotted with the Monte Carlo transient simulation results as a comparison. It can be seen that the analytical gives a good prediction in the offset voltage from each pair and especially in the main offset contributors.

VI. CONCLUSION

In this paper, we presented a novel balanced method to analyze input referred offset voltages in dynamic comparators. The method solves the problem that in a dynamic comparator the operating points of transistors are not well defined in the transient process. Based on this method, the explicit expressions for static offset voltages caused by μC_{ox} and V_{th} variation and dynamic offset voltages caused by capacitance mismatch are derived based upon "Lewis-Gray" dynamic comparator. The comparator is implemented in 0.25-μm and 40-nm CMOS process as examples. The analytical results from those expressions achieve good agreements with more accurate Monte Carlo transient simulations. The analytical model also gives a good prediction to the offset in the second topology dynamic comparator. Those explicit formulas of offset voltages allow designers to find out the most dominant contributors to offset and to use those formulas as guidance to design and optimize dynamic comparators.

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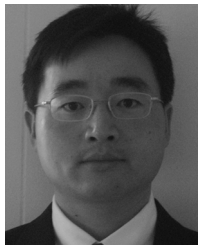

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