Stimulus Generator for SEIR Method Based ADC BIST

Jingbo Duan, Bharath Vasan, Chen Zhao, Degang Chen, and Randall Geiger
Iowa State University
Ames, IA 50011

Abstract — **Testing of ADC in SOC is a significant challenge since it usually has no connection to the outside. Built-in self-test (BIST) is regarded as a promising alternative to traditional test. Most reported ADC BIST research works try to replicate a production test scheme on chip. This approach requires input ramp with high linearity which is hard to achieve on chip. This paper investigates signal generator implementation issues of adapting stimulus error identification and removal method which was presented for production test into a practical ADC BIST solution. A stimulus generator using very small transistor count is presented. Extremely simple methods for generating small constant voltage level shifts are introduced and evaluated. Simulation results show that generated signals with less than 7 bits linearity, together with the simple level shifts, are able to test a 16-bit ADC to 16 bit accuracy level. These results demonstrate that accurate BIST of deeply embedded AMS blocks may be practically implemented on chip with very low overhead.**

I. Introduction

Increasingly more analog and mixed signal (AMS) blocks are integrated in complex Systems-on-Chip (SOCs). Testing of these deeply embedded AMS blocks has emerged as a major challenge in SOC technique. Lack of access to internal analog nodes, difficulty in maintaining signal integrity driving accurate signals on and off chip, and long external testing time are among the reasons leading to the challenge. As a result, practical low-cost Built-In Self-Test (BIST) is regarded as the alternative to traditional production test.

Significant research efforts have been invested on ADC BIST with most being focused on replicating a production test scheme on chip. Most reported ADC BIST strategies require highly linear stimulus generator [1]-[3], which is the most challenging block in ADC BIST. The stringent accuracy requirement on stimulus severely limits the viability of such an approach, since it is even more challenging to design stimulus generators with higher linearity but in much smaller area than AMS blocks under test.

Several algorithms that allow low linear stimuli to be used in test of high linearity ADC were presented in [4]-[6]. Experimental results of first two papers showed that 16 bits ADC can be tested within reasonable accuracy using stimulus with only 7 bits linearity.

This paper investigates signal generator implementation issues of adapting one of such algorithms into a practical ADC BIST solution. A stimulus generator using very small transistor count is presented. Extremely simple methods for generating small voltage level shifts are introduced and evaluated. Simulation results show that generated signals are able to test 16-bit ADC to 16 bit accuracy level. In section 2, the stimulus error identification and removal (SEIR) method is briefly reviewed first. Then constancy requirements of voltage level shift are derived. In section 3, a signal generator with small number of transistors is presented. In section 4, methods for generating voltage level shift are presented. Simulation results are given in section 5.

II. Cost Effective ADC TEST Method

2.1 SEIR method

In quasi-static linearity test procedure with ideal input ramp signal, each transition level of ADC can be expressed as following.

$$T_i = T_0 + (T_{N-2} - T_0) \cdot t_i \qquad i = 0,1...N-2 \tag{1}$$

In which, T_0 and T_{N-2} are the first and last transition levels of ADC respectively. Transition time t_i can be acquired from histogram data. Differences between these tested transition levels and end points fit line transition levels give INLs.

In real test environment, input ramp signal is nonlinear and can be expressed as the sum of an ideal ramp and the nonlinear part.

$$V(t) = T_0 + (T_{N-2} - T_0) \cdot t + \sum_{j=1}^{M} a_j F_j(t) + \varepsilon \tag{2}$$

The nonlinear part is modeled by a set of basis functions $F_j(t)$ and ε is the residual error. If coefficients of all basis functions are known, nonlinearity of input ramp is known.

In SEIR method, two ramp signals with the same nonlinearity are used to test the ADC. The only difference between these two signals is a constant voltage level shift so that $V_2(t)$ equals to $V_1(t)$ - α.

Similar to equation (1), we can get following equations

$$T_i = T_0 + (T_{N-2} - T_0) \cdot t_i^{(1)} + \sum_{j=1}^{M} a_j F_j\left(t_i^{(1)}\right) + \varepsilon \tag{3}$$

$$T_i = T_0 + (T_{N-2} - T_0) \cdot t_i^{(2)} - \alpha + \sum_{j=1}^{M} a_j F_j\left(t_i^{(2)}\right) + \varepsilon \tag{4}$$

These two equations contain non-linearity information of both ADC and input ramp. Remove T_i from (3) and (4), we can solve coefficients of all basis functions by using least square method.

978-1-4244-4495-3/09/$25.00 ©2009 IEEE

$$\{\hat{a}_j s, \hat{\alpha}\} = \arg\min\left\{\sum_{k=0}^{N-2}\left[\hat{t}_{k,1} - \hat{t}_{k,2} + \sum_{j=1}^{M} a_j\left[F_j(\hat{t}_{k,1}) - F_j(\hat{t}_{k,1})\right] + \alpha\right]^2\right\} \quad (5)$$

The set of basis functions represents the nonlinear part of input ramp. The real transition level T_i of ADC can be calculated from (3) or (4).

2.2 Constancy requirement of voltage level shift

The SEIR requires the voltage level shift to be constant, which is impossible in real implementation. Non-constant voltage level shift causes computation errors in coefficients of basis functions and then errors in transition levels. The computation error of transition level T_k caused by non-constant voltage level shift is.

$$\hat{T}_{k-e} = \sum_{j=1}^{M} \delta_j F_j(\hat{t}_k) = -\frac{1}{\alpha}\int_0^{\hat{t}_k} N(\tau)d\tau \quad (6)$$

In which, α is the constant part and $N(t)$ is the non-constant part of voltage level shift.

Then the error in estimated INL_k is

$$\hat{INL}_{k-e} = \hat{T}_{k-e} \cdot \frac{N-2}{T_{N-2} - T_0} \quad (7)$$

The maximum estimation error is

$$\max\left|\hat{INL}_{k-e}\right| = \frac{2^n}{\alpha} \cdot \max\left|\int_0^{\hat{t}_k} N(\tau)d\tau\right| \quad (8)$$

In which, n is the resolution of ADC, the value of $\hat{t}_k$ is from 0 to 1. Since the test is based on end point fit line, there is no estimation in the first and last transition level. From equation (6), we have

$$\int_0^1 N(\tau)d\tau = 0 \quad (9)$$

Define the maximum variation of $N(t)$ as

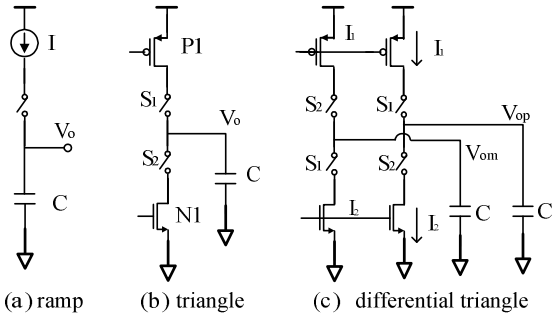
$$\Delta\alpha = \max(N(\hat{t}_k)) - \min(N(\hat{t}_k)) \quad (10)$$

From equation (8), we have

$$\max\left|\hat{INL}_{k-e}\right| \le \frac{2^n}{\alpha} \cdot \frac{\Delta\alpha}{2} \quad (11)$$

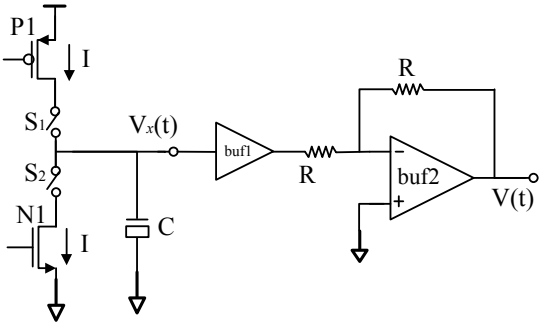
Use $\Delta\alpha/\alpha$ as the constancy requirement of voltage level shift.

$$\frac{\Delta\alpha}{\alpha} \le \frac{INL_e}{2^{n-1}} \quad (12)$$

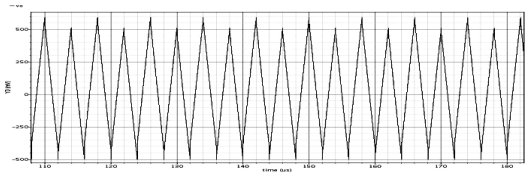


(a) ramp (b) triangle (c) differential triangle

Fig.1. Capacitor charging circuits



(a) Signal generator



(b) Triangular signal

Fig.2. Ramp or triangle signal generation

INL_e is the required maximum estimation error. For a 16-bit ADC, in order to make the maximum estimation error smaller than 0.2 LSB, we can calculate the constancy requirement of the voltage level shift is 6.1ppm. Equation (12) gives the most conservative constraint of voltage level shift. But the estimation error depends on the shape of non-constant part, and can be calculated from (8) if the shape is known. The value of $\Delta\alpha/\alpha$ needs to be smaller than 25ppm when $N(t)$ is a 1st order function, and 47.5ppm when $N(t)$ has parabola shape.

III. Stimulus Generator

BIST schemes for ADC blocks in SOC must have very small cost overhead and stimulus generators should consume very small area. A simple and direct implementation is charging a capacitor with a current source as shown in Fig.1.a. Very large capacitor is needed to generate a very slowly ramp signal, which is costly to be implemented on chip. The alternative way is using triangular signal as stimulus of ADC as shown in Fig.1.b. Output resistance values of P1 and N1 change with output voltage even when they are both in saturation region [7]. Without any enhancement, this circuit can easily generate a ramp signal with about 7-bit linearity, which is enough for SEIR. The structure shown in Fig.1.c provides differential triangle signal with the same rising and falling slope.

Fig.2.a shows a low overhead generator that can generate two triangular signals with a small voltage level shift between them. A MOS CAP is charged and discharged by two simple current sources to get rising and falling ramps. An amplifier is used as the inverting unit gain buffer to generate a small voltage level shift and also accommodate switch capacitor application. In order to keep the voltage level shift constant enough for 16-bit level test, DC gain of the opamp is designed to be 88dB. Since the triangular

signal has very low frequency, the bandwidth does not to be large and it is 22MHz here. Another buffer buf1 is used to separate capacitor from resistors in buf2. Since linearity requirement of the triangular signal at the output of buf1 is still low, a source follower is good enough to be buf1.

Due to noise and environmental variation, voltage level shift cannot be constant during test procedure, which decreases the accuracy of SEIR. One way to relieve this influence is interleaving the original triangular signal and the shifted signal [6]. Fig.2.b shows the output triangular signal, in which the original triangular signal and the shifted signal are interlaced.

This signal generator costs small power and area. The charge and discharge current source can be very simple, without any enhancement for constant output resistor or linear current. The MOS transistor has higher capacitance density than MIM capacitor so that area can be smaller for same capacitance value.

IV. Introducing Voltage Level Shift

The buf2 in Fig.2.a can act as an adder, and the small voltage level shift can be added to stimulus signal at two nodes of the buffer as shown in Fig.3.a. Take both differential and common mode gain into consideration, the output voltage can be expressed as

$$V_O = \frac{(A_d + A_c/2)(1+R/R_1+R/R_2)}{1+R/R_1+R/R_2+A_d-A_c/2}\cdot V_2 - \frac{(A_d - A_c/2)}{1+\frac{R}{R_1}+\frac{R}{R_2}+A_d-\frac{A_c}{2}}\cdot(V_1\frac{R}{R_1}+V_{in}\frac{R}{R_2}) \quad (13)$$

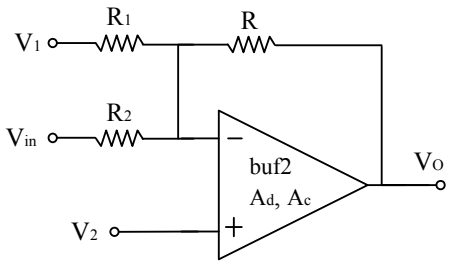
A_d is the differential gain and A_c is the common mode gain of the amplifier.

When V_1 is used as voltage level shift, V_2 in (13) equals to 0. The voltage level shift can be expressed as

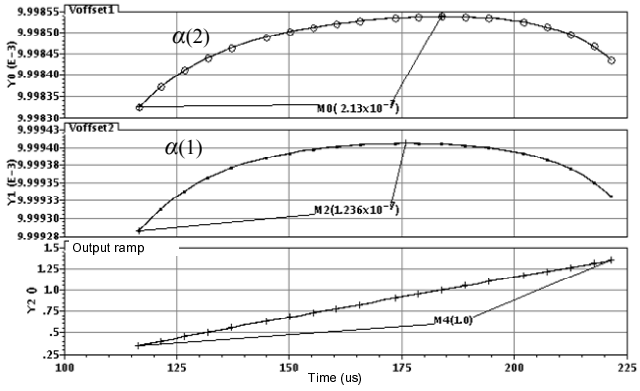
$$\alpha_1 = \frac{(A_d - A_c/2)}{1+R/R_1+R/R_2+A_d-A_c/2}\cdot\frac{R}{R_1}V_1 \approx (1-\frac{1+R/R_1+R/R_2}{A_d-A_c/2})\cdot\frac{R}{R_1}V_1 \quad (14)$$

Assume the buffer has unity gain, and R_1=R_2=R with good layout matching. Neglect nonlinearity of resistors and V_1, constancy of the voltage level shift can be expressed as

$$\frac{\Delta\alpha_1}{\alpha_1} = \frac{-\Delta\left(\frac{1+R/R_1+R/R_2}{A_d-A_c/2}\right)}{1-\frac{1+R/R_1+R/R_2}{A_d-A_c/2}} \approx -3\bullet\Delta\left(\frac{1}{A_d-A_c/2}\right) \quad (15)$$



(a) Buffer



(b) Output waveform

Fig.3. Adding level shift to stimulus

When V_2 is used as voltage level shift, V_1 in (13) equals to 0 and R_1 is infinite. The voltage level shift can be expressed as

$$\alpha_2 = \frac{(A_d - A_c/2)+A_c}{1+R/R_2+A_d-A_c/2}\bullet(1+\frac{R}{R_2})V_2 \approx (1+\frac{A_c}{A_d-A_c/2})(1-\frac{1+R/R_2}{A_d-A_c/2})\bullet(1+\frac{R}{R_2})V_2 \quad (16)$$

Neglect the nonlinearity of resistors, constancy of the voltage level shift can be calculated as following.

$$\frac{\Delta\alpha_2}{\alpha_2} = \frac{-\Delta\left(\frac{1+R/R_2}{A_d-A_c/2}\right)}{1-\frac{1+R/R_2}{A_d-A_c/2}} + \frac{\Delta\left(\frac{A_c}{A_d-A_c/2}\right)}{1+\frac{A_c}{A_d-A_c/2}} \approx -(2-A_c)\cdot\Delta\left(\frac{1}{A_d-A_c/2}\right)+\frac{\Delta(A_c)}{A_d-A_c/2} \quad (17)$$

Neglect the third term of (17), the constancy becomes

$$\frac{\Delta\alpha_2}{\alpha_2} \approx -(2-A_c)\cdot\Delta\left(\frac{1}{A_d-A_c/2}\right) \quad (18)$$

Compare (18) with (15), adding voltage level shift at the positive node of amplifier provides better constancy if the common mode gain is in the range of (-1, 5).

Fig.3.b shows a ramp waveform with magnitude of 1V at the output of buf2, and two voltage level shifts that are generated at nodes V1 and V2 respectively. The opamp used in this buffer has 88dB DC voltage gain, 22MHz unity gain frequency and -5dB positive common mode voltage gain. As shown in the plot, the constancy of α_1 and α_2 are 21 ppm and 12 ppm respectively. The difference between constancy of these two voltage level shifts agrees with the relation between (15) and (18).

The amplifier in buf2 is a regular two-stage miller compensated amplifier with seven transistors. Instead of adding the voltage level shift to ramp, the intrinsic offset voltage of the amplifier can be used as the voltage level shift required in SEIR. Fig.4.a shows the 1st stage of the amplifier, four different methods can be used to introduce mismatch and then offset voltage to the amplifier.

As shown in Fig.4.a, a small current mismatch is introduced by M6 and M7. Cascode transistor M7 is added to decrease the channel length modulation of M6 so that the current ΔI_a can be more constant. A PMOS transistor with gate being connected to control signal is good enough to act as a switch here. The equivalent intput offset voltage can be expressed by (19).

$$V_{os(a)} = \frac{\Delta I_a}{g_{m2}} \tag{19}$$

Non-constancy of $V_{os(a)}$ is caused by non-constant mismatch current and non-constant transconductance of input pair. Large voltage gain can keep variation of g_{m2} small.

The second way of generating offset voltage is introducing size mismatch between the two input transistors. M8 has the same length as M2 and M1 but smaller width. The gate and source of M8 have the same connection as M1. The drain of M8 is connected to that of M1 through a PMOS switch. The equivalent input offset voltage is

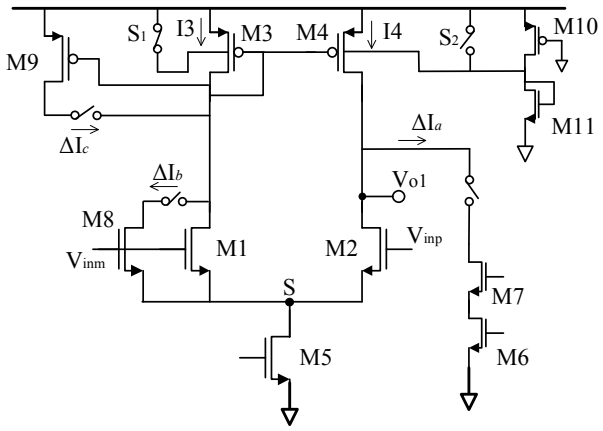
$$V_{os(b)} = \frac{g_{m8}}{2g_{m1}} \cdot (V_{GS8} - V_{Tn}) \tag{20}$$

Non-constancy of $V_{os(b)}$ comes from variation of V_{GS8} and the non-constant transconductance of M8 and M1. Since M8 and M1 have the same length and connections, the nonlinearity of g_{m8} and g_{m1} can partly cancel each other.

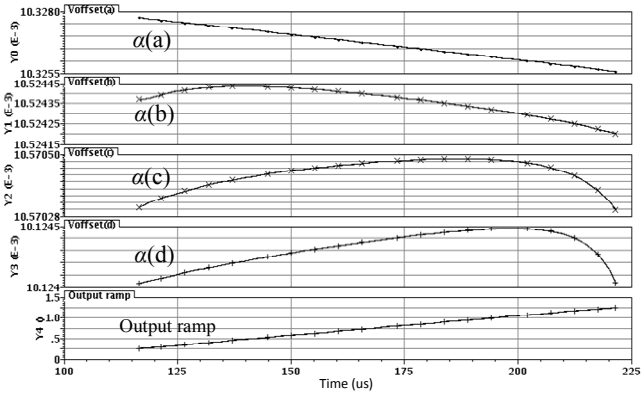
The third way of generating offset voltage is introducing size mismatch between active loads. M9 has the same length as M3 and M4 but smaller width. The gate and source of M9 have the same connection as M3. The drain of M9 is connected to the drain of M3 through a PMOS switch. The equivalent input offset voltage can be expressed by (21).

$$V_{os(c)} = \frac{g_{m9}}{2g_{m1}} \cdot (V_{GS9} - V_{Tp}) \tag{21}$$

Non-constancy of $V_{os(c)}$ comes from variation of gate voltage of M9 which is also the drain voltage of M1 and the non-constant transconductance of M9 and M1. Since V_{GS9} has the same variation tendency as V_{GS1}, the variation of g_{m9} and g_{m1} can also partly cancel each other.



(a) Introducing mismatch



(b) Output waveform

Fig.4. Offset voltage in amplifier

The fourth method to generate offset voltage is bulk connection mismatch between active load. S1 is always closed and S2 is connected to control voltage. The equivalent input offset voltage can be expressed in terms of threshold voltage mistmach between M3 and M4.

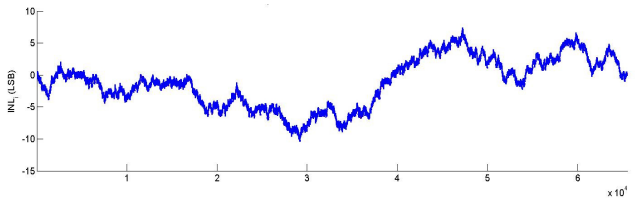
$$V_{os(d)} = \frac{g_{m3}}{g_{m1}} \cdot \left| V_{th3} - V_{th4} \right| \tag{22}$$

Non-constancy of the $V_{os(d)}$ comes from the nonlinear transconductance of M1 and M3. Keeping variation of input voltage V_{inm} small helps reduce the non-constancy.

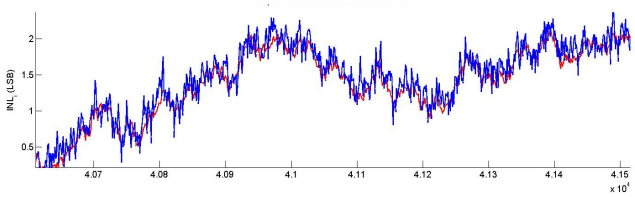
The voltage level shift is just two times of the input offset voltage. Fig.4.b shows the output ramp and voltage levl shift generated by these four methods. The output ramp has magnitude of 1V under 1.8V power supply. Constancy of voltage level shift generated from method (a), (b), (c), and (d) are 211ppm, 21ppm, 17ppm, and 44ppm respectively. The constancy of method (a) is 10 times worse than other methods. Instead of helping increase constancy, the constant ΔI_a in (19) aggravates the constancy of voltage level shift. It also can be seen that method (b) and (c) need only 2 extra transistors and are very easy to be implemented.

Table.2. Comparison of 4 voltage level shifts

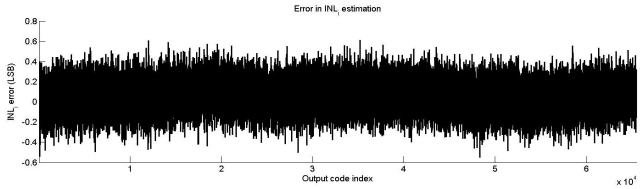
Level shift method	(1)	(2)	(a)	(b)	(c)	(d)
Ramp linearity (%)	1	1	1	1	1	1
Constancy (ppm)	21	12	211	21.1	17.3	44.4
INL Estimation error(LSB)	0.69	0.65	2.16	0.74	0.61	0.87
Number of transistors	NA	NA	5+	2	2	4



(a) True and estimated INL



(b) Zoomed in INL plot



(c) Error of INL estimation

Fig.5. INL estimation error for 16 bit ADC

V. Simulation Results

Some simulations have been done in both Cadence and Matlab to validate the ramp generator and voltage level shift generator. Ramp and voltage level shift generator are designed at transistor level with 0.18µm CMOS process and 1.8V power supply voltage. A 16-bit ADC with 1V full scale range is modeled in Matlab code. Random error is introduced to every transition level to generate INL error.

The output data of the signal generator is used as the input of ADC in Matlab. To accommodate the testing, the ramp signal is sampled by $32*2^{16}$ points. The ramp has magnitude of 1V and 1% linearity. ADC receives both original and shifted ramp signal from Cadence. The voltage level shift is about 1% of the full scale range. 1 LSB random noise is added to ramp signals before histogram testing.

Fig.5.a shows the true and estimated INL of the ADC, and Fig.5.b shows the zoomed in plot. The red curve is true INL curve and the blue curve is estimated INL of the ADC. It can be seen that estimated INL curve tracks true INL curve very well. Estimation errors of all INL_i are plotted in Fig.5.c, the largest estimation error is about 0.61LSB. Under the same simulation setup, INL test accuracy is also around 0.6LSB when ideal linear ramp is used. Other simulation results show that the INL estimation accuracy does not change when true ADC INL is different. More simulation results are shown in Table.2. As shown in the table, the error of INL estimation is proportional to the constancy of voltage level shift.

VI. Conclusion

By adapting SEIR method to on chip ADC BIST, the linearity requirement of stimulus is decreased. So that signal generators can be realized by simple circuits and in small area. A capacitor charging circuit based signal generator and six methods of generating voltage level shift are presented and evaluated. Simulation results show that the generated signal, together with voltage level shift which is generated by only 2 transistors can be used to test 16 bits ADC to 16 bit accuracy level.

References

[1] H. K. Chen, C. H. Wang, and C. C. Su, "A self calibrated ADC BIST methodology," in Proc. 20th IEEE VLSI Test Symp., 2002, pp. 117–122.

[2] Dongmyung Lee, et al, "Code-width testing-based compact ADC BIST circuit," IEEE Trans. Circuits Syst. II, vol. 51, pp. 603 – 606, Nov. 2004.

[3] Yun-Che Wen, "A BIST scheme for testing analog-to-digital converters with digital response analyses," IEEE 23rd VLSI Test Symp., 2005, pp. 383 – 388.

[4] L. Jin, K. Parthasarathy, T. Kuyel et al, "Accurte Testing of Analog-to-Digital Converters Using Low Linearity Signals With Stimulus Error Identification and Removal," IEEE Trans. Instrum Meas., vol. 54, pp. 1188 – 1199, June 2005.

[5] L. Jin, D. Chen and R. L. Geiger, "SEIR linearity testing of precision A/D converters in nonstationary environments with center-symmetric interleaving," IEEE Trans. Instrum Meas., vol. 56, pp. 1776 – 1785, Oct. 2007.

[6] H. Jiang, B. Olleta, D. Chen and R. L. Geiger, "Testing high-resolution ADCs with low-resolution/accuracy deterministic dynamic element matched DAC," IEEE Trans. Instrum Meas., vol. 56, pp. 1753 – 1762, Oct. 2007.

[7] J. H. Huang et al, "A physical model for MOSFET output resistance," in IEDM Tech. Dig., 1992, pp.569–572.