Signal generators for cost effective BIST of ADCs

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Abstract— **Conventional approach to linearity testing of ADCs requires a signal generator that is more linear than the device under test (DUT). Recently introduced ADC testing algorithms dramatically relax the linearity requirements on the signal generator in exchange for maintaining a known functional relationship between two unknown nonlinear test signals. Simple signal generators that can be used to generate the two non-linear signals are discussed. Simulation results show that the generated signals can be used to test ADCs with resolution ranging between 6 and 17bits.**

I. INTRODUCTION

Traditional quasi static linearity testing of analog to digital converters (ADC) s requires signals that are 3 to 4 bits more linear than the ADC under test. The challenge of generating highly linear or spectrally pure stimulus signals with a very small die area is one of the biggest challenges in developing practical methods for Built in Self Test (BIST) of ADCs[4]-[5]. For this reason, quasi static linearity BIST of even a 12-bit ADC is almost never attempted in commercial products.

Recently, methods for high-resolution ADC testing have been introduced [1] – [3] that dramatically relax the linearity requirements of the test signal generators. Measured results have been presented [1] that make use of stimuli that are only 7-bit linear to test 16-bit ADCs and simulation results indicate that even lower levels of linearity could be used. In this work, two imprecise nonlinear but functionally related excitations (FRE) were applied to the ADC under test to obtain two sets of correlated output data. From these two sets of data, the linearity of the device under test (DUT) can be accurately extracted. The dramatic reduction in linearity requirements of the signal generator offers potential for overcoming one of the major challenges in practically implementing BIST for high-performance ADCs.

Specific requirements on the functional relationship between the two nonlinear excitations must be met to use this approach for testing. One functional relationship that can be used is a constant shift. Practically, two low linearity ramps, the second being shifted by a small voltage from the first, can serve as the two FRE test signals. With this approach, the requirement on the linearity of the stimulus is replaced with the requirement of constancy of the shift between the two signals. A constant shift can be viewed as generating the second signal by adding a small offset to the first. This paper focuses on the design of signal generators that can add a small but constant offset voltage to a given signal. The constancy requirements for different ADC resolution requirements are discussed in Section II. . Simple and practical signal generators that can be used for BIST of ADCs are presented in Section III. Different methods of adding the voltage offset are considered in Section IV and Section V.

II. CONSTANCY REQUIREMENT

Shift-based non-linear FRE testing offers trade-offs between linearity in the test signal generator and constancy of the shift [1]-[3].The shift constancy requirement is strongly dependent upon the specific characteristics of the FRE testing algorithm. For FRE based SEIR testing used in this work, it can be shown that for a small shift, the algorithmic error in estimating the INL of the ADC will be bounded by 0.25LSB if the following condition [4] is satisfied:

$$\frac{\Delta\alpha}{\alpha} < \frac{1}{2^{n-21}}\,(\text{ppm}) \qquad (1)$$

where α is the nominal value of the voltage shift (offset voltage) ,n is the resolution of the ADC under test and Δα is the maximum change in the shift over the full scale input range. Note that this expression is not dependent upon the linearity of the excitation. Although not stated here, there are some readily satisfied restrictions on the high spatial frequency content of the excitation [1]. From this expression, it can be seen that the constancy of voltage shift should be around 32ppm for testing a 16-bit ADC and around 2000ppm for testing a 10-bit ADC. With this approach, the requirement on the linearity of stimulus signals is completely replaced by a requirement on the constancy of the voltage shift. Practically, α is typically around 0.1% to 1% of the full scale range [1].

III. SIMPLE RAMP GENERATOR CIRCUITS:

Simple circuits like the one shown in Fig. 1 can be used to generate a ramp-like signal.

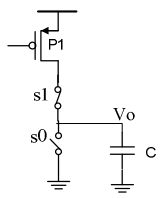

Fig.1: Ramp generator circuit.

The PMOS transistor P1 acts as a current source. Switches s1 and s0 are used to initiate the charge and discharge of the capacitor C. For BIST implementation, the capacitor area must be small. The output is termed "ramp-like" because the non ideal transistor P1 and the nonlinear part of the capacitor C will introduce modest nonlinearities that cause the output to differ from an ideal ramp output. This ramp-like signal can be used as one of the two inputs for a shift-based FRE testing strategy.

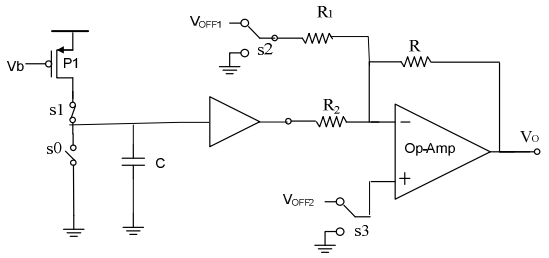

Fig.2: Simple signal generator circuit.

A standard analog summing circuit can be used to introduce a shift in the ramp-like signal by adding a small dc voltage to the ramp-like signal. The circuit of Fig. 2 shows one such op-amp based summing circuit. The shift can be added by either closing switch s2 or by closing switch s3. If the gain of the op-amp is sufficiently high, this circuit will provide a constant dc offset but if the op amp gain is not sufficiently high, nonlinearities in the operational amplifier will introduce small nonlinearities in the shift.

It is well-known that the offset voltage of an operational amplifier invariably introduces an undesirable shift in the output voltage of most op-amp based circuits. If the offset voltage of an operational amplifier can be controlled by a switch, however, the offset voltage change from when the switch is open to when the switch is closed will provide two signals that are ideally different by a constant shift. The circuit diagram for such a ramp generator is as shown in Fig.3 where switch s3 is used to intentionally introduce mismatch internal to the operational amplifier. The offset voltage in an operational amplifier is comprised of two parts, the systematic part and the random part. The random part, caused by random mismatches and process variations, is not of concern to us. This is because it would be common to both ramp-like signals. Likewise, the systematic part which is common to both ramp-like signals is not of concern either. The difference in the systematic part, which is under the designer's control, can be changed to introduce the desired offset (shift) in the output voltage.

The input-referred offset voltage for the ramp-like signal generator of Fig. 3 is shown explicitly in Fig. 4 where it has been assumed that a constant voltage source V_{OS} can be used to model the offset effects.

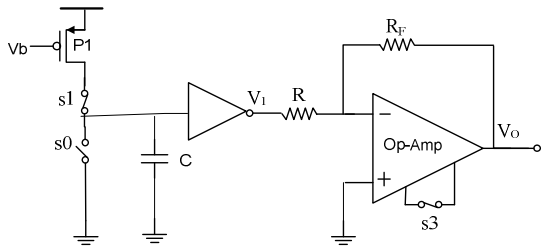

Fig.3: Offset voltage based ramp-like signal generator

If the amplifier is linear, the output voltage is given by,

$$Vo = -V_1 \frac{\frac{R_F}{R_1}}{1+(1+\frac{R_F}{R_1})\frac{1}{A_{OL}}} + V_{OS}\frac{(1+\frac{R_F}{R_1})}{1+(1+\frac{R_F}{R_1})\frac{1}{A_{OL}}} \qquad (2)$$

where A_{OL} is the open loop dc gain of the amplifier. If we define Vos1 and Vos1 to be the offset voltages before and after s3 is closed and assume A_{OL} is not affected by s3, it follows that the difference in the two ramp-like signals is given by the expression.

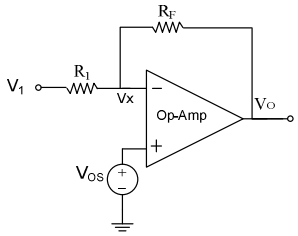

Fig.4: Simple inverting amplifier.

$$V_D = (V_{OS2} - V_{OS1})\frac{(1+\frac{R_F}{R_1})}{1+(1+\frac{R_F}{R_1})\frac{1}{A_{OL}}} \qquad (3)$$

$$V_D \approx (V_{OS2} - V_{OS1})\,(1+\frac{R_F}{R_1}) \text{ if } A_{OL} \to \infty \qquad (4)$$

If A_{OL} is affected by s3 or if A_{OL} is nonlinear, the shift predicted by (3) is not valid. These concerns are germane in this BIST application because of the requirements given in Section II that the shift be really constant for testing high resolution ADCs.

IV. INTERNAL INTRODUCTION OF SHIFT VOLTAGES

Fig.5 and Fig.6 show two well-known two-stage amplifiers. The amplifier in Fig.5 uses the standard five-transistor first stage followed by a common source second stage. The two-stage amplifier in Fig.6 has a higher dc gain and uses a cascode amplifier for the first stage and a common source amplifier for the second stage. If we consider the first stage of the amplifier in Fig. 5 as a stand-alone amplifier with output V_{OUT1} along with the two-stage structures in Fig.5 and Fig.6 with outputs V_{OUT3} and V_{OUT4}, three amplifiers are identified with varying circuit complexity and varying gain.

Any mismatch in a nominally symmetric circuit will introduce offset. The switches ϕ1- ϕ3 and Θ1-Θ6 shown in the amplifiers of Fig. 5 and Fig. 6 introduce offset in different ways in the first stage of the amplifiers. When used in the structure of Fig. 3, two ramp-like signals that differ by a shift are generated. One is generated with all switches open and the second with exactly one switch closed. For example, closing switch ϕ1 introduces a bias-current mismatch between the left and right sides of the circuit, closing switch ϕ2 introduces a mismatch in the p-channel loads, and closing switch ϕ3 causes an effective mismatch in the differential input pair.

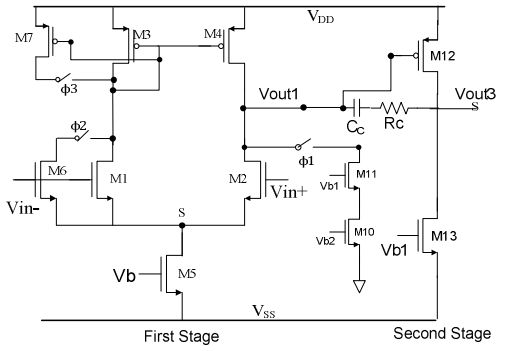

Fig.5: Two-stage amplifier with five-transistor first stage and switch controlled offset

Correspondingly, in the amplifier of Fig. 6, Θ1- Θ4 introduce bias current mismatch. For notational convenience, cascode current sources are depicted as ideal current sources in this figure. Θ5 introduces a mismatch in the differential input pair and Θ6 changes the bulk voltage of M6 thus causing a mismatch in the p-channel loads.

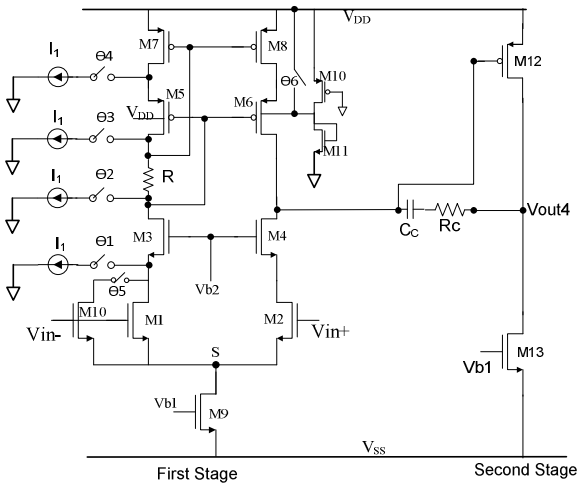

Fig.6: Two-stage amplifier with cascode first stage and switch-controlled offset

V. SIMULATION RESULTS:

All amplifiers have been designed in the 0.18u TSMC process with a supply of 1.8V. The ramp-like input is 1V full scale. The shift values that are used are in the range from 1mV to 4mV. The resistors in the feedback amplifier were both 1MΩ. All switches are single n-channel transistors with a switch control voltage of 3.3V. In the results tables shown, a '1' indicates which switch is closed. The maximum deviation in the shift over the full scale input range was simulated and expression (1) was used to obtain the equivalent number of bits, n_{EQ} of an ADC that can be tested with this signal generator.

1. Single stage amplifiers.

In the five-transistor amplifier, the transistors were sized for 0.2 volts of excess bias and a total power dissipation of 0.18mW.The nominal dc gain of the op-amp is 34dB and the GB is 130MHz. For the case of closing ϕ1, M10 was sized to introduce a current of 1% of the tail current value to produce the desired offset voltage. Correspondingly, the aspect ratio of the transistor in parallel with the driving transistor is around 3% of the driving transistor's aspect ratio. The aspect ratio of the transistor in parallel with the load is around 5% the load transistor's aspect ratio. Simulation results for the performance of the level shifters are tabulated in Table 1.

Single Stage Amplifier:Five Transistor

ϕ1	ϕ2	ϕ3	α(mV)	n_{EQ}
1	0	0	3.9	5.3
0	1	0	3.5	5.7
0	0	1	3.9	6.1

Table1.

2. Two stage amplifiers

In the amplifier with the five-transistor first stage and common source second stage, the transistors were all sized for 0.2 volts of excess bias. Power dissipation of the first stage and second stage were 0.18mW and 0.54mW, respectively. The nominal dc gain of op-amp is 76dB and the GB is 143MHz. In the two-stage amplifier with the cascode first stage, the transistors were all sized for 0.2 volts of excess bias. Power dissipation of the first stage and second stage were 0.27mW and 0.81mW, respectively. The nominal dc gain of op-amp is 105dB and the GB is 72MHz. Simulation results are tabulated in Table 2.

From Table 1 and Table 2, it can be observed that changing the source of internal offset and changing the amplifier gain plays a big role on the constancy of the shift with ADC BIST capability ranging from under 6 bits to in excess of 16 bits with these amplifiers.

3. Optimization of two stage amplifiers.

Since in this BIST application, the ramp-like shift generators are used for quasi static testing of ADCs, the

speed of the operational amplifier is of little concern. Hence the Gain Bandwidth product requirements on the two stage op-amp can be relaxed. This allows us to drop the current levels in the second stage and hence reduce the overall power dissipation As discussed above, the shift becomes more constant as the gain is increased.

Two Stage Amplifier with Five Transistor first stage

$\phi1$	$\phi2$	$\phi3$	α(mV)	n_{FO}
1	0	0	3.6	12.7
0	1	0	3.8	13.5
0	0	1	3.6	13.2

Two Stage Amplifier with Cascode first stage

$\Theta1$	$\Theta2$	$\Theta3$	$\Theta4$	$\Theta5$	$\Theta6$	α(mV)	n_{FO}
1	0	0	0	0	0	3.5	14.9
0	1	0	0	0	0	3.6	14.9
0	0	1	0	0	0	3.6	14.3
0	0	0	1	0	0	3.8	14.3
0	0	0	0	1	0	3.8	16.4
0	0	0	0	0	1	2.2	14.3

Table2.

. The two-stage structures can be modified to extract more gain from the first stage by decreasing the excess bias on the first-stage transistors. The excess bias on the transistors of first stage, in the two stage amplifier of Fig.5, was reduced to 0.175 volts and the power of the second stage was dropped to half that of the first stage. The new dc gain of op-amp is 87dB and the GB is 40MHz. Correspondingly, the transistors in the first stage of the two-stage amplifier with the cascode first stage were resized to achieve an excess bias of 0.18 volts. The power of the second stage was dropped to half that of first stage. The nominal dc gain of this op-amp is increased to 116dB and its GB is 36MHz. Simulation results of the resultant shift generator are tabulated in Table 3.

Comparing the results in Table 3 with those in Table 2, it can be observed that significant improvements in the linearity of the shift can be attained through a more optimal choice of biasing voltages and power dissipation. Most importantly, it can be concluded from these tables that practical signal generators can be designed that are useful for BIST of ADCs with resolution ranging from 6 bits to nearly 18 bits using the FRE approach with the shift relationship.

VI. CONCLUSION:

Simple signal generator circuits that can be used for practical BIST of ADCs using the shift operator in the FRE approach to testing have been introduced. Simulation results indicate that these signal generators can be used for linearity testing of ADC whose resolution range from 7bits to 18bits.

Two Stage Amplifier with Five Transistor first stage

$\phi1$	$\phi2$	$\phi3$	α(mV)	n_{FO}
1	0	0	3.8	13.5
0	1	0	3.5	16.4
0	0	1	3.4	17.1

Two Stage Amplifier with Cascode first stage

$\Theta1$	$\Theta2$	$\Theta3$	$\Theta4$	$\Theta5$	$\Theta6$	α(mV)	n_{FO}
1	0	0	0	0	0	3.7	15.8
0	1	0	0	0	0	3.8	15.9
0	0	1	0	0	0	3.8	17.0
0	0	0	1	0	0	3.7	16.9
0	0	0	0	1	0	3.6	17.8
0	0	0	0	0	1	1.1	17.4

Table 3.

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