Design Procedure and Performance Potential for Operational Amplifier using Indirect Compensation

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Abstract—**A design procedure for an operational amplifier using indirect compensation is presented in this paper. Indirect compensation has inherent benefits in regards with power to speed trade-off. The technique has been seldom used in the past because a clear methodology for designing such an amplifier has not been provided. This paper develops the mathematical and analytical insight for designing an operational amplifier with this technique. The paper also provides a design strategy and an example to illustrate the use of the proposed design procedure.**

I. INTRODUCTION

CMOS op-amps are integral part in various analog and mixed signal circuits and systems. The driving force behind the development of CMOS digital design, demands for high integration to lower fabrication costs, and lower voltage supplies to reduce power consumption. Given current standard CMOS fabrication process cannot withstand supply voltages higher than 1.1V[1] , there is a strong push to perform research in circuits able to operate at this voltage, however without sacrificing performance.

Single stage amplifiers have traditionally been preferred for their ability to simultaneously achieve adequate dc gains and large gain-bandwidth (GBW) products. These architectures rely on a technique called cascoding to provide adequate DC-gain using only a single stage [2, 3]. With supply voltages declining [3], the single-stage cascoded based architectures have become unsuitable for some application. As a result, designers have started looking for alternative architectures to overcome the drawbacks of single stage amplifiers. Multiple stage amplifiers can thus be used to achieve higher gain circuit designs. Nevertheless, multistage amplifiers generally are difficult to compensate. Many compensations schemes for multistage amplifiers have been investigated and reported [3-6]. The most widely used compensation technique in analog circuit and systems design is undoubtedly pole splitting using Miller capacitor.

This paper revisits an alternative method to miller compensation using an indirect compensation [7, 8, 12] scheme as shown Figure 2. Indirect feedback is provided using a common gate amplifier from the output of the amplifier to the output of the internal stage. As it will be shown the technique relies on boosting the speed of the internal stages of a multi-stage amplifier and thus pushing the non-dominant poles to higher frequencies. The technique provides promising performance. In the past the technique has been ignored as a clear design procedure has not been provided. In this paper a clear design procedure is laid out to maximize the amplifier performance.

In section II we will briefly develop mathematically the traditional miller compensation and bring upfront the reasons of significantly reduced bandwidth. Analytical and mathematical analysis of the alternative multistage op-amp topology with indirect feedback frequency compensation is presented in Section III. Design guidelines are provided in Section IV for designing an amplifier with indirect frequency compensation. A design example is shown Section V and the results are compared to conventional miller compensation.

II. MILLER COMPENSATION

Dominant pole compensation with pole splitting is a traditional technique used to achieve adequate phase margin. The transfer function for a Miller compensated two-stage op-amp with small signal model in Figure 1 is

$$\frac{V_{out}}{V_d} = \frac{gm_1R_1gm_2R_2\left(1-\frac{s}{z_1}\right)}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)} \qquad Equation: 1$$

The zero is in the right half place and the dominant pole are located at

$$p_1 = -\frac{1}{gm_2R_2R_1C_c} \qquad z_1 = \frac{gm_2}{C_c} \qquad Equation: 2$$

And the non-dominant pole is located at

$$p_2 = -\frac{gm_2C_c}{C_cC_1 + C_1C_L + C_cC_L} \approx -\frac{gm_2}{C_1 + C_L} \qquad Equation: 3$$

To eliminate the RHP zero and improve the phase margin of the op amp, lead compensation which adds a nulling resistor in series with compensation capacitor to increase the impedance of the feedthrough path is reported in [5].

The open-loop gain of the op-amp is given as $A_v = gm_1R_1gm_2R_2$, while the unit gain frequency or (gain-bandwidth) is given as $f_{un} = gm_1/2\pi C_c$. It can be observed the capacitance C_1 loads the second pole. C_1 is a function

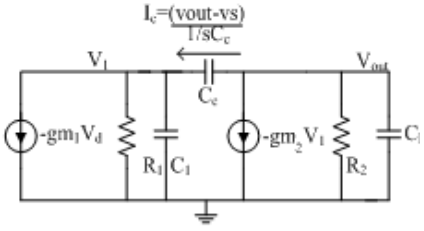

Figure 1: Small Signal Model for Miller Compensation

of the miller capacitor C_c and parasitics. For large capacitive loads (C_L) a large compensation capacitor is required which pushes the p_2 to lower frequency. Thus the amplifier speed gets limited by the second stage.

III. INDIRECT COMPENSATION

The recommended architecture in this paper is based on providing the feedback current indirectly from the output node to the high impedance node of the first stage as shown in Figure 2. The compensation capacitor is connected to an internal low impedance node, which allows an indirect feedback of the compensation current from the output node to the internal high impedance node. A common gate amplifier is used to provide the indirect path, however the internal common gate amplifier achieves a higher purpose. In order to obtain an insight into the indirect feedback compensation, the small signal model for the common gate stage op-amp topology is shown in Figure 3. The transfer function for the amplifier can be derived and simplified.

$$\frac{V_{out}}{V_d} = -A_V\left(\frac{b_0 + b_1 s}{a_0 + a_1 s + a_2 s^2 + a_3 s^3}\right) \quad Equation: 4$$

$b_0 \approx gm_6 R_A roc$

$b_1 \approx R_A roc(C_c + C_A)$

$a_0 \approx (gm_c R_A + 1)\, roc$

$a_1 \approx gm_2 R_2 R_1 roc C_c\,(gm_6 R_A + 1)$

$a_2 \approx (gm_6 R_A + 1) R_2 C_1 R_1 roc(C_2 + C_c) + R_2 C_2 R_A[roc(C_c + C_A) + R_1(C_c + C_A + C_1)]$

$a_3 \approx R_1 C_1 R_2 roc R_A(C_2 C_A + C_2 C_c + C_c C_A)$

Using the numerator expression, we obtain the location of the zero to be at which is evidently a left half plane zero.

$$z_1 \approx -\frac{b_0}{b_1} = -\frac{g_{mc}}{C_c + C_A} \quad Equation: 5$$

With the assumption that $p_1 \gg p_2,\ p_3$, the dominant real pole [2] is given as

$$p_1 \approx -\frac{a_0}{a_1} = -\frac{1}{g_{m2} R_2 R_1 C_c} \quad Equation: 6$$

Now for $s \gg p_1$, the denominator of the transfer function D(s), can be approximated as

$$D(s) \approx \left(1 - \frac{s}{p_1}\right)\left(1 + \frac{a_2}{a_1} s + \frac{a_3}{a_1} s^2\right) \quad Equation: 7$$

In the above equation, the non-dominant poles are real and widely spaced and apart when $\left(\frac{a2}{a1}\right)^2 \gg 4\left(\frac{a_3}{a_1}\right)$. The above condition is satisfied when

$$gm_6 \gg \frac{4 gm_5 C_c\left(\frac{C_L C_c}{C_L + C_c} + C_A\right)}{C_1(C_L + C_c)} \quad Equation: 8$$

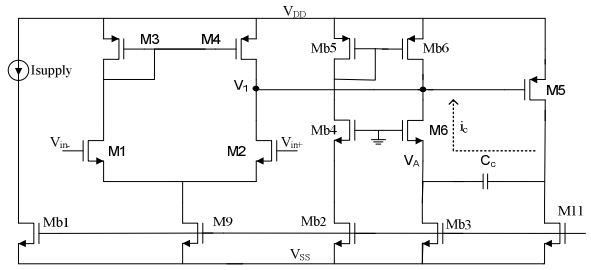

Figure 2: Indirect Frequency Compensation Schematic

The above equation requires a large gm_6 in comparison to gm_5. However when the condition is satisfied the non-dominant poles are real and are located at frequency shown below. The non-dominant poles are given by:

$$p_2 \approx -\frac{a_1}{a_2} = -\frac{g_{m2} C_c}{C_1(C_c + C_2)} \approx -\frac{g_{m2} C_c}{C_L C_1} \quad Equation: 9$$

$$p_3 \approx -\frac{a_2}{a_3} \approx -\frac{g_{m6}}{\left(\frac{C_L C_C}{C_L + C_c}\right)} + \frac{1}{R_1 C_1} \approx -\frac{g_{m6}}{\left(\frac{C_L C_C}{C_L + C_c}\right)}$$

For large C_L the non dominant pole $p_3 \approx -\frac{g_{mc}}{(C_c)}$

The unity-gain frequency of the op-amp is given as:

$$f_{uf} \approx \frac{\omega_{un}}{2\pi} = \frac{|p_1| A_V}{2\pi} = -\frac{g_{m1}}{2\pi C_C} \quad Equation: 10$$

From Equation 9 the non-dominant pole, when using indirect feedback compensation, is located at $-\frac{g_{m2} C_c}{C_L C_1}$ while the second pole for Miller compensation was located at $-\frac{gm_2}{C_1 + C_L}$.

By comparing the two equations, we can examine that the second pole, p_2, has moved further away from the dominant pole by a factor of approximately C_c/C_1. Furthermore the LHP zero adds to the phase response near the unity gain frequency and thus improves the phase margin. The overall transfer function of the system can be express as

$$\frac{V_{out}}{V_d} = \frac{\omega_{un}}{s} \cdot \frac{1}{1 + \frac{s}{\frac{g_{m2} C_c}{C_L C_1}}} \cdot \frac{1 + \frac{s}{\frac{g_{mc}}{C_c + C_A}}}{1 + \frac{s}{\frac{g_{m6}}{\left(\frac{C_L C_C}{C_L + C_c}\right)}}} \quad Equation: 11$$

Thus the condition on gm_6 can be re-written as the following

$$f_{T6} > \frac{gm_6}{C_c + C_A} > 4\frac{gm_2 C_c}{C_1(C_L + C_c)} \frac{\frac{C_L}{C_c + C_c} + C_A}{C_c + C_A} \quad Equation: 12$$

$$f_{T6} > |z_1| > f_{T2} \cdot \frac{C_c}{C_L + C_c} \quad Equation: 13$$

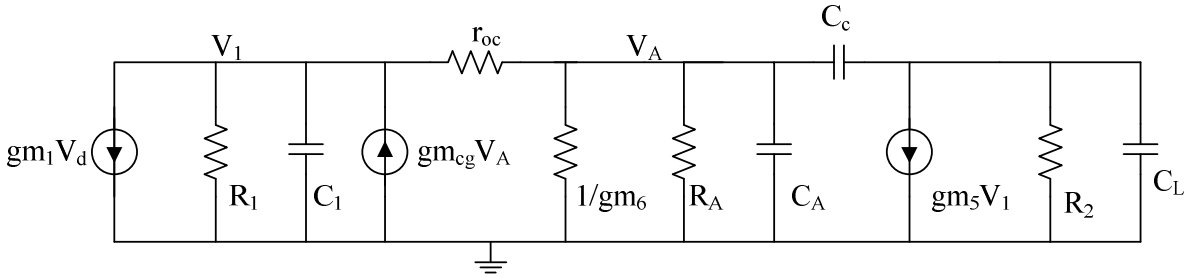

Figure 3: Small Signal Model for Indirect Compensation

The above argument implies that now we can achieve pole splitting with a much lower value of compensation capacitor (Cc) and a lower value of second stage transconductance (gm2). Conversely, lower value for gm_2 translates into lower power as the bias current can be reduced. On the other hand, we can achieve higher unity gain frequency for the op-amp without affecting stability and hence obtain a higher speed amplifier or drive a larger load capacitor for a given phase margin[11]. Analytically the reason the non-dominant pole shifted to a higher frequency is because the compensation capacitor now does not load the first stage output. Also equation 13 is a key requirement for this architecture as it expresses the condition with respect to the transition frequency (f_T) of transistor M6 and M2 the common gate amplifier and output stage respectively. It signifies that the indirect path has to be much faster than the output stage which thus relocates non dominant pole to higher frequency and thus improving the unity gain frequency. Blatantly observing, indirect feedback compensation can lead to the design of op-amps with significantly lower power, higher speed and lower layout area.

Further, it can be noticed the non-dominant pole p_3 is approximately equal to z_1 as the parasitic capacitance $C_A \ll C_c$. Thus Vout/Vin can be reduced to

$$\frac{V_{out}}{V_s} = \frac{\omega_{uf}}{s} \times \frac{1}{1-\frac{s}{p_2}} \qquad Equation: 14$$

Following Mahattanakul [10] constraints and design strategies for sizing common gate amplifier M_5 can be developed. The phase margin with 100% feedback can be shown to be

$$\varphi_M = \tan^{-1}\frac{|p_2|}{\omega_{uf}} = \tan^{-1}\frac{\omega_{T5}C_c}{\omega_{uf}C_L} \qquad Equation: 15$$

Where by denoting $V_{eff5} = V_{SG6} - V_{t5}$

$$\omega_{Tc5} = \frac{gm_5}{C_{gs5}} = \frac{\frac{3}{2}\mu_p}{{L_5}^2}V_{eff5} \qquad Equation: 16$$

is the transition frequency for M6. Combining 9,15 and 16 yields

$$L_5 = \sqrt{\frac{3\mu_p V_{eff6} C_c}{2\omega_{uf} C_L \tan\varphi_M}} \qquad Equation: 17$$

IV. DESIGN PROCEDURE

The dc and transient characteristics of a two stage op-amp are independent of the compensation method, the design procedure of the op-amp in Figure 2 can be obtained by modifying the design procedure in [10]. The necessary modifications are in Step 3 and Step 10 where the compensation conditions of (8) and (17) are applied, i.e.,

Step 3) Use (14), $Veff_5 = {V_{HR}}^{out+}$ [11] to compute L_6.

Step 10) Use (8) to choose values of $(W/L)_6$ and I_{D6}

The proposed design procedure of the op-amp in Figure 2 is shown in Table I.

TABLE I
PROPOSED OP-AMP DESIGN PROCEDURE

Step 1	$C_c = \frac{16KT}{3\omega_{uf}S_n(f)}\left[1+\frac{SR}{\omega_{uf}\left({V_{HR}}^{CM+}+V_{tn}\right)}\right]$
Step 2	$I_{D11} = SR(C_c + C_L)$
Step 3	$L_5 = \sqrt{\frac{3\mu_p {V_{HR}}^{out+} C_c}{2\omega_{uf}C_L\tan\varphi_M}}$
Step 4	$W_5 = \frac{2SR(C_c+C_L)}{\mu_p C_{ox}\left({V_{HR}}^{out+}\right)^2}L_6$
Step 5	$I_{D9} = C_c SR$
Step 6	$\left(\frac{W}{L}\right)_{1,2} = \frac{{\omega_{uf}}^2 C_c}{\mu_n C_{ox} SR}$
Step 7	$\left(\frac{W}{L}\right)_9 = \frac{2SRC_c}{\mu_n C_{ox}\left({V_{HR}}^{CM-} - V_{tn} - \frac{SR}{\omega_{uf}}\right)^2}$
Step 8	$\left(\frac{W}{L}\right)_{11} = \left(\frac{C_c+C_L}{C_c}\right)\left(\frac{W}{L}\right)_9$
Step 9	$\left(\frac{W}{L}\right)_{3,4} = \frac{\left(\frac{W}{L}\right)_5}{2\left(\frac{W}{L}\right)_{11}}\left(\frac{W}{L}\right)_9$
Step 10	$\left(\frac{W}{L}\right)_6 = \frac{4\left(\frac{W}{L}\right)_5 C_c\left(\frac{C_L C_c}{C_L+C_c}+C_A\right)}{C_1(C_L+C_c)}$

Definitions
$V_{HR}^{CM+} = VDD - V_{CM(MAX)}$
$V_{HR}^{CM-} = V_{CM(MIN)} - VSS$
$V_{HR}^{OUT+} = VDD - V_{OUT(MAX)}$
$V_{HR}^{OUT-} = V_{OUT(MIN)} - VSS$

V. Design Example

A design example is provided to illustrate the use of the procedure. Following the design procedure in section IV the transistor sizing for schematic in Figure 2 is provided in Table IV. As seen from Table 5, the architecture provides the same gain bandwidth for less than half the power in comparison to miller compensation in [10].

TABLE II
PROCESS PARAMETERS (AMI 0.5 MICRON C5N)

Parameters	NMOS	PMOS
$\mu \left[cm^2/_{Vsec}\right]$	458	212
$V_t\ [V]$	0.7	-0.9
$T_{ox}\ [nm]$	13.9	13.9

TABLE III
OPAMP SPECIFICATION

Supply Voltages	± 2.5 V
Load Capacitance: C_L	5 pF
DC gain: A_o	80 dB
Unity-gain Frequency: f_u	5 MHz
Phase Margin: φ_M	60°
Slew Rate: *SR*	5 V/µs
Input Common Mode Range: V_{CMR}	± 1.5 V
Output Swing: $V_{out\ \{max,min\}}$	± 2.3 V

TABLE IV
DESIGN PARAMETERS

$(W/L)_{1,2}$	1.5µm/1.8µm
$(W/L)_{3,4}$	1.95µm/1.8µm
$(W/L)_9$	1.95µm/1.05µm
$(W/L)_5$	88.05µm/3.0µm
$(W/L)_{11}$	6.0µm/1.05µm
$(W/L)_{6,MB4}$	22.05µm/1.05µm
$(W/L)_{MB5,MB6}$	130.05µm/3.0µm
$(W/L)_{MB2,MB3}$	7.05µm/1.05µm
C_c	0.5 pF

TABLE V
SIMULATED RESULTS

Design	Propose	Miller [11]
DC gain: A_o	81 dB	85.1 dB
Unity-gain Frequency: f_u	5.74 MHz	6 MHz
Phase Margin: φ_M	63°	65°
Slew Rate: *SR+/-*	5.8/-5.1 V/µs	6.0/-5.2 V/µs
Input Common Mode Range: V_{CMR+} / V_{CMR-}	2.1/-1.6 V	2.1/-2.18 V
Output Swing: $Vout_{MAX}/Vout_{MIN}$	2.32/-2.31 V	2.16/-2.2 V
Power	101 µW	207 µW

Comparing Table V to Table III, it can be seen the operational amplifier performance meets the specifications as desired and thus the design procedure is a good guideline for designing indirect feedback frequency compensation based operational amplifiers.

VI. Conclusion

The simulated results confirm that the proposed procedure can be effectively used to design an op-amp with indirect feedback compensation. Table V further reflects the potential of indirect feedback in comparison to standard miller compensation for providing stability to the op-amp. The benefits are consistent with analysis provided in Section III. The general procedure provided in Table IV thus is a good guideline for designing operational amplifiers with indirect frequency compensation and utilizing the architectures inherent benefits.

VII. References

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