Threshold-Based Voltage Reference with pn- Junction Temperature Compensation

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Abstract

A new voltage reference with output dependent upon the threshold voltage of an NMOS transistor is introduced. A low temperature coefficient is achieved by using a pn-junction PTAT current generator to compensate for the negative temperature coefficient of the threshold voltage. Implemented in a standard 0.6μm CMOS process with an output of 1.67V, it has a temperature coefficient of 4.9ppm/°C over a 195 °C range.

1. Introduction

Integrated voltage references with low sensitivity to temperature and supply voltage are a critical component in many integrated circuits. Several methods of realizing references are discussed in [1]. All invariably use the weighted sum of two voltages, one with a positive temperature coefficient and one with a negative temperature coefficient, with the weight adjusted so that the thermal derivative vanishes at a predetermined temperature. The difference of two pn-junction voltages is very linear in temperature and is actually proportional to absolute temperature (PTAT). This difference is widely used to generate the positive temperature coefficient (PTC) voltage. Correspondingly, the pn-junction voltage has a negative temperature coefficient (NTC) and is widely used in references to generate the NTC voltage. Unfortunately, the pn-junction voltage does not vary linearly with temperature and is the major contributor to the non zero temperature coefficient (TC) of the reference. Many different curvature-compensation techniques have been developed to address this problem [4][5], but they are all based on pn-junction type circuit. As an alternative, Manku [7] suggests using a single NMOS device to achieve a low TC reference and suggests a TC of 13ppm from 0°C to 125 °C is achievable but gives no circuit. Filanovsky [8] demonstrated that diode-connection transistors can stabilize the current and voltage reference.

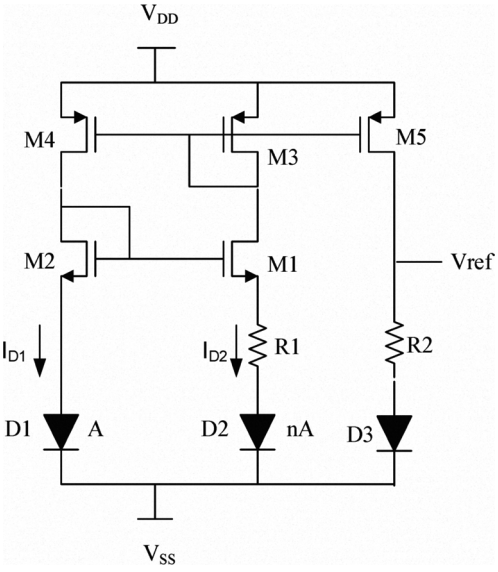


Fig. 1 Conventional bandgap voltage reference circuit.

In this paper, emphasis is placed on using the threshold voltage of an NMOS device to generate the NTC voltage. The resultant voltage reference designed in a 0.6um processes has an output voltage of 1.67V and a TC of 4.9ppm/°C over the -50°C to 145°C range.

2. Conventional Bandgap Reference Circuit

The object in reference generation is to establish a DC voltage or current which is independent of supply and remains constant when temperature varies. The weighted addition of two signals that have opposite sign but equal magnitude linear temperature coefficients can generate a temperature-independent output. If V_1 has a positive variation with temperature and V_2 has a negative variation with temperature, the reference voltage can be expressed as

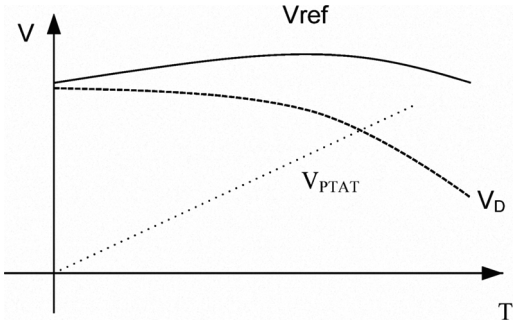


Fig. 2 Relationship between linear V_{PTAT} and nonlinear V_D on the output voltage of the conventional bandgap reference circuit.

$$V_{ref}=\alpha_1 V_1+\alpha_2 V_2, \quad (1)$$

where α_1 and α_2 are constants.

The thermal derivative of V_{ref} will vanish when

$$\alpha_1 \frac{\partial V_1}{\partial T}+\alpha_2 \frac{\partial V_2}{\partial T}=0. \quad (2)$$

The basic principle of most bandgap references is present in the commonly used voltage reference shown in Fig.1. In this circuit, the reference voltage is the sum of the NTC pn-junction voltage of D_3 and the PTAT voltage drop across R_2.

Assume $M_{1\text{-}2}$ are identical, and $M_{3\text{-}5}$ are identical. The reference output voltage thus can be written as

$$V_{ref}=V_{D3}+\frac{R_2}{R_1}\frac{kT}{q}\ln(n), \quad (3)$$

where k is Boltzmann's constant (1.38×10^{-23} J/K), q is electronic charge(1.6×10^{-19} C), and n is the area ratio of pn-junctions of D_2 and D_1. The temperature behavior of a pn-junction can be described as [3]

$$V_D=V_T\ln(I_D)+V_{G0}-V_T\left[\ln\left(\tilde{J}_{SX}A\right)+m\ln(T)\right], \quad (4)$$

where V_T is the thermal voltage, m is the order of the temperature dependence of the mobility, V_{G0} is the bandgap voltage of silicon, A is the junction area and $\tilde{J}_{SX}$ is a process constant. The positive TC comes from the difference between two V_D when I_{D1} equals I_{D2}, and $A_2=nA_1$ as can be seen from the expression

$$\Delta V_D=V_{D1}-V_{D2}=V_T\ln n. \quad (5)$$

It follows upon differentiation of (5) that ΔI_D is PTAT

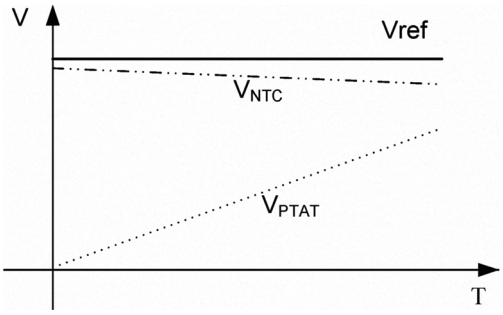


Fig. 3 The ideal zero TC reference voltage of proposed method.

$$\frac{\partial(\Delta V_D)}{\partial T}=\frac{k}{q}\ln n. \quad (6)$$

Differentiation of (4) with respect to T shows that the TC of V_D is nonlinearly dependent on temperature thus creating an error in the reference voltage. The relationship between the NTC voltage, the PTAT voltage, and the overall reference voltage for a conventional reference is shown in Fig. 2.

3. Circuit Implementation

Since V_{PTAT} is linear with temperature, it will be combined with a more linear NTC circuit in the proposed voltage reference. The threshold voltage of an NMOS transistor is modeled by [6]

$$V_{tn}(T)=V_{tn0}(T_0)+\frac{\partial V_{tn}}{\partial T}(T-T_0), \quad (7)$$

Where V_{tn} is threshold voltage, T_0 is an arbitrary reference temperature, and $\frac{\partial V_{tn}}{\partial T}$ is a negative constant that is about -0.782mV/°C. If the threshold voltage of an NMOS transistor is added to the weighted PTAT voltage, one can ideally obtain a zero TC reference voltage as conceptually shown in Fig.3.

Consider the well-known circuit in Fig.4(a) (start up circuit not shown). Assuming for simplicity that $MP_{5\text{-}10}$ are identical, $MP_{1\text{-}4}$ are identical, the resistors are made of the same material and are ratio-matched, and output impedance effects in the transistors are negligible, it

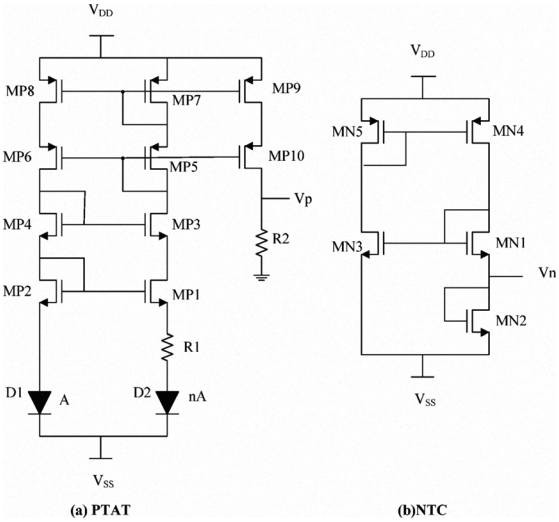


Fig. 4(a) A basic V_{PTAT} circuit, and (b) The threshold voltage extracted circuit.

follows that V_P is a PTAT voltage given by the expression

$$V_P = V_t \ln n\left(\frac{R_2}{R_1}\right) \qquad (8)$$

The simple supply-independent bias generator of Fig.4(b) (start-up circuit not shown) can extract the n-channel threshold voltage and provides the NTC voltage. If the square-law model without body effects and channel length modulation is used to model the MOS transistors, it follows that V_n can be expressed as

$$V_n = \frac{1-\sqrt{\frac{\beta_{N3}}{M\beta_{N1}}}}{1-\sqrt{\frac{\beta_{N3}}{M\beta_{N2}}}-\sqrt{\frac{\beta_{N3}}{M\beta_{N1}}}} V_m \propto V_m, \qquad (8)$$

where V_{tn} is threshold voltage, M is the mirror gain $\frac{W_{N5}}{L_{N5}}\frac{L_{N4}}{W_{N4}}$, and β_k is $\frac{1}{2}\mu_n C_{ox}\frac{W_k}{L_k}$ for k $\in$ {N1, N2, N3}. The formula shows that V_n is proportion to V_{tn}, and independent of mobility and C_{OX} since these model parameters cancel in the β ratios. However, since channel length modulation effects have been neglected in this analysis, the negative TC output voltage will exhibit a small supply dependence. The supply dependence can be reduced by using relatively long channel lengths. The channel length modulation effects and the bulk effect will also introduce a weak temperature-dependent

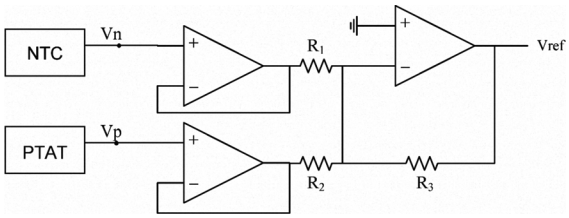


Fig. 5 Complete zero TC Voltage reference circuit.

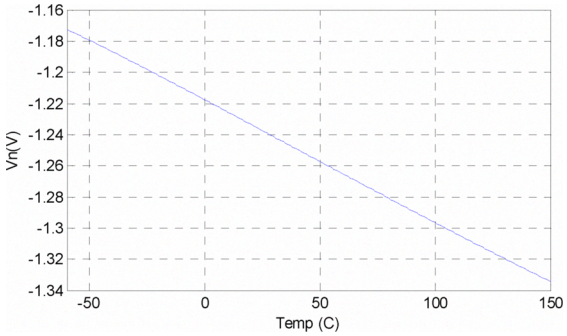


Fig. 6 The output of NTC circuit.

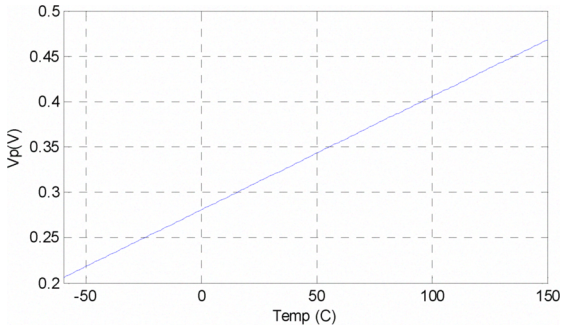


Fig. 7 The output of PTAT circuit.

nonlinearity but closed-form expressions for these effects are unwieldy.

To demonstrate the potential of combining the PTAT and NTC voltages, the weighted adder shown in Fig.5 is used. The operational amplifiers are assumed to be ideal to exclude any non-ideal effects coming from the amplifiers. More practical methods of combining the PTAT and NTC voltages can be used but are not the focus of this work.

4. Simulation Result

The circuit shown in Fig. 4 was designed for realization in the 0.6 μm AMI process using the BSIM3v.3 MOS

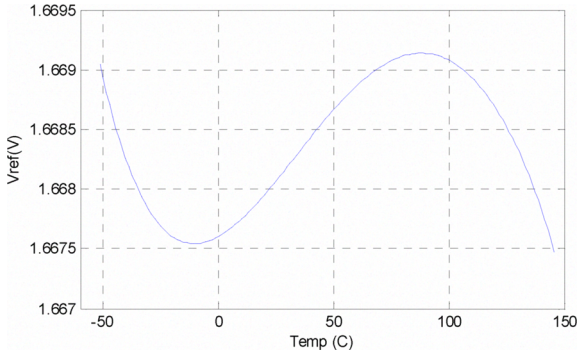


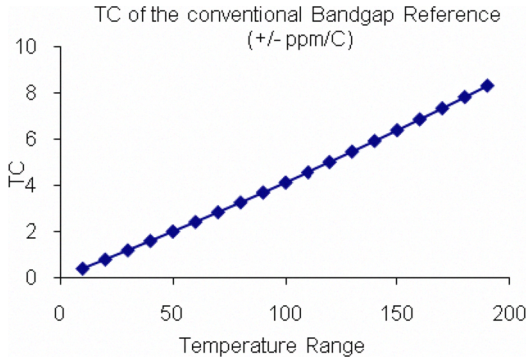
Fig. 8 Reference voltage simulate from -50°C to 145°C.

model. The TC parameters and resistor values used in the simulation are shown in Table 1. Fig. 6 and Fig. 7 show the simulation results for Vn and Vp. Fig. 8 shows the overall reference voltage $V_{ref.}$ V_{ref} is 1.668V at 27°C and the TC is 4.91ppm/°C from -50°C to 145°C. It can be seen that there are two inflection points which are due to the weak nonlinearities in the NTC.

Table. 2 shows the comparison between different works [7][8][9]. When compared with the conventional bandgap circuit result shown in Fig. 9, the new reference provides a reduction in the TC of nearly a factor of 2.

5. Conclusion

A new approach for designing a voltage reference using a pn-junction based PTAT source and an n-channel V_t based NTC source was introduced. Simulation results show the new circuit has a TC equals of 4.91ppm/°C from -50°C to 145°C which is nearly a factor of 2 less than that of a standard bandgap reference.



Fig, 9 An ideal relationship between TC and temperature range of the conventional [2] bandgap reference.

Table 1 TC of Vn and Vp and weighted resistors in the adding circuit.

Voltage	TC	Weighted Resistor	
Vn	-7.82×10^{-4}	R1	1KΩ
Vp	1.25×10^{-3}	R2=R3	1.6KΩ

Table 2 Comparison of recent works.

	Temperature range	TC
This work	-50°C~145°C(190°C)	4.91ppm
[7]1995	0°C~125°C(125°C)	13ppm
[8]2000	-50°C~150°C(200°C)	31.3ppm
[9]2004	-50°C~150°C(200°C)	4ppm
Conventional [Fig. 9]	190°C	8.32ppm

6. References

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