Phase Control of Triangular Stimulus Generator for ADC BIST

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***Abstract*—Coherent sampling is required in ADC testing. Unlike production testing in which fractional frequency is available, only sampling clock of ADC is available for ADC Built-in Self-test (BIST). Triangular stimulus generator controlled by sampling clock of ADC cannot provide enough information because same voltages are sampled in every period. To carry out valid data acquisition, different voltages in different period should be sampled. Instead of generating fractional frequency, a method of introducing delay to every ramp in triangular wave is proposed in this paper. An 8-bit digital to time converter (DTC) is designed to provide needed number of delays. A control scheme is proposed to provide both phase control of triangular stimulus and testing control of BIST. Simulation results show control scheme works well for linearity test and delayed triangular wave provides valid data acquisition for histogram test. Errors in delay affect test results very little.**

I. INTRODUCTION

In ADC testing, two requirements should be met for coherent sampling. The first one is that integer number of periods of input signal should be sampled to avoid energy leakage. The second requirement is that different voltage level should be sampled and repetitive sampling should be avoided. In ADC production test, frequency synthesizer is used to provide fractional frequency for input signal [1]. With easy access to fractional frequency, sine wave is preferred in ADC production test because of low distortion [2].

Considerations are different for ADC BIST application in which everything needs to be implemented on chip. Area is the most important concern in ADC BIST so that circuits should be simple. Triangular wave can be generated by very simple circuits on chip. Besides, triangular wave make data process easy and is easy to be controlled [3]. Research work has been published recently on testing ADC linearity by using nonlinear ramp or triangular wave as stimulus [4]. The method performs very well in production testing and shows great potential to be used in ADC BIST [5]. For good cost efficiency, no extra fractional frequency clock would be generated on chip. Therefore, only sampling clock of ADC is available on chip. Triangular stimulus generator also needs to be controlled by this clock. If each ramp in the triangular wave is started by a signal synchronized with sampling clock, same voltages will be sampled by ADC in every period of triangular stimulus. In this case, a large number of codes will never be hit and some codes will be hit a huge number of times. Such data acquisition is useless for histogram test.

A method of changing the phase of each ramp in triangular stimulus without fractional frequency is proposed in this paper. Because triangular wave is easy to be interrupted and controlled, starting time of each ramp is delayed by certain amount of time. Because of these time delays, different voltages in different period can be sampled. A digital to time converter (DTC) is used to provide different time delays. In addition to phase control, the proposed control scheme is also a practical testing control of ADC BIST. The rest of this paper is organized as following. In section II, how to achieve coherent sampling by introducing delay is described. In section III, circuit design issue of DTC and control circuits are discussed. Simulation results are given in IV.

II. ACHIEVING COHERENT SAMPLING BY DELAY

Different from ADC production test, low cost and small area are properties that ADC BIST scheme should have. Triangular wave generator is more cost efficient than sine wave generator for BIST of ADC static performance. This is because triangular wave generator has simpler structure and is easy to be adjusted. To avoid increasing area and cost, fractional frequency synthesizer should not be built on chip. Sampling clock of ADC is the only clock signal available on chip. If the control signal of triangular wave is generated from this clock, same voltages of different cycles will be sampled by ADC. These samples are useless for ADC testing. A method of delaying every ramp in triangular wave to achieve coherent sampling is discussed in this section.

Fig.1 shows a triangular wave controlled by synchronous signal with sampling clock and the delayed version of it. Vertical broken lines represent clock edges that are also sampling time of ADC. In Fig.1 (a), every ramp of the triangular wave starts at the clock edge. It can be seen that six points are sampled in each cycle, and same points are sampled in other cycles. Only sampling in the first cycle is useful even though four cycles are used. Histogram of these samples gives very bad INL since some codes do not show at all. Fig.1 (b) shows the triangular wave that is delayed at each starting point; original triangle is also shown in gray line for reference. The sampling period is T_s and triangular wave period is $8T_s$, each ramp of the triangular wave starts at time $i \cdot 4 \cdot T_s$ (i=1, 2, 3…). The new triangular wave is

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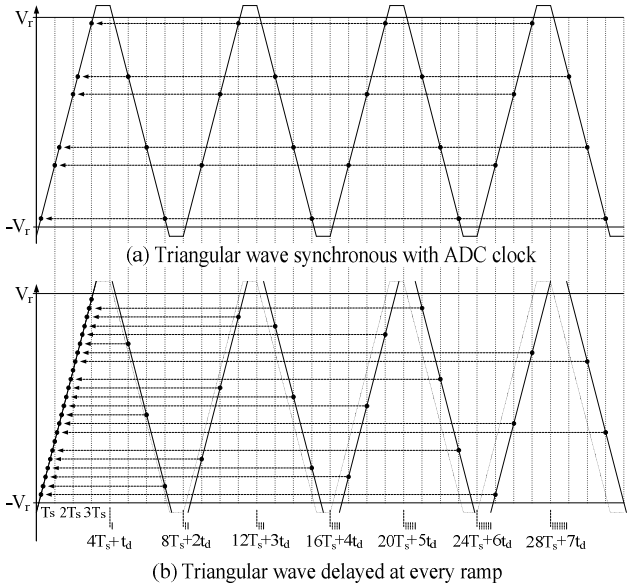


Fig.1. Sampling of triangular wave

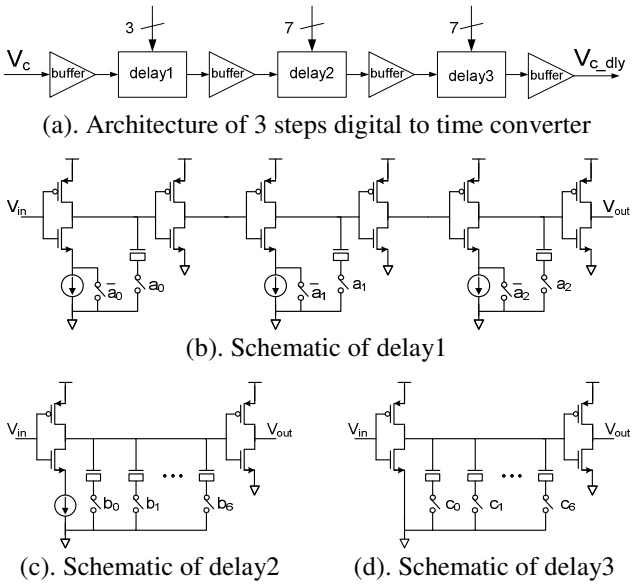


Fig.2. A 3-step digital to time converter

delayed at starting point of every ramp. Denote the first ramp as R_0, the second ramp as R_1, and so on. The delay amount of R_i is $i \cdot t_d$ in which t_d is the delay unit. It can be seen that sampled points are evenly distributed when they are folded into one ramp. Sampling points that occur out of the range of the triangular waveform are discarded in histogram data.

In order to guarantee no repetitive sampling happens and sampled points evenly distribute on one ramp, the value of delay unit t_d should be

$$t_d = j \cdot \frac{T_s}{N_{cyc}} \qquad j = 1,3,5,... \tag{1}$$

in which T_s is the sampling period, j is an odd number, N_{cyc} is the number of triangular wave cycle that is needed to complete the data acquisition. For a given ADC and T_s, N_{cyc} is determined by the period of triangular wave and total number of points needed in histogram. Value of j can be used to adjust delay unit t_d to be a convenient value. In the case shown in Fig.1, j equals to 1, which gives small delay unit and requires small area to generate.

III. CIRCUIT DESIGN

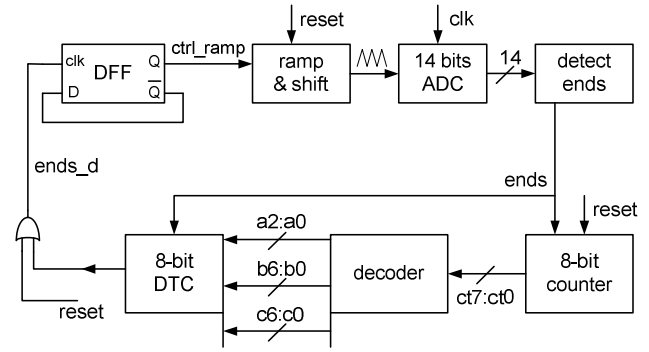
Phase control of triangular wave is mainly realized by two blocks including delay generator and control circuits. For different ADC test, phase control circuit will be different. A phase control circuit is designed for testing of a 14 bits and 100MSamples/s ADC. The delay generator and control circuits are discussed in this section.

A. Digital to Time Converter

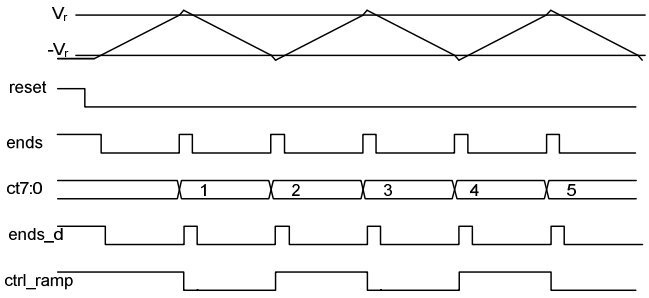
The triangular wave is assumed to be generated by charging and discharging a 10pF capacitor with 1uA current. So the period of triangular wave is about 20us and the time duration of each ramp is about 10us. The sampling period T_s of the ADC mentioned above is 10ns, so that about 2000 points will be sampled in one triangular wave period. For ADC histogram that has 16 hits per code, the total number of samples should be 262144. In order to complete the data acquisition, about 131 periods of triangular wave is needed. For the efficiency of digital decoder, 127 periods are actually realized. Totally, 254 ramps will be generated and 253 time delays are needed.

An 8 bits digital to time converter (DTC) is built to provide 255 time delays. The DTC is realized in 3-step structure as shown in Fig.2 (a). Input of this DTC is a digital signal synchronized with sampling clock. The output is the delayed version of input, which will be used as the start signal of a ramp. The delay is provided by three delay cells, and the delay amount is controlled by 17 bits code which is the output of decoder. Buffers are added after delay cells to reconstruct digital signal. According to equation (1), the delay unit is chosen to be 39ps which requires the smallest area.

Fig.2 (b) shows the schematic of delay1 which is a 2-bit digital to time converter and provides 3 levels of delay amount. Current starving inverter and MOSCAP load works together to generate 2.5 ns time delay. This cell is repeated three times so that the maximum time delay delay1 can generate is 7.5 ns. Fig.2 (c) shows the schematic of delay2 which is a 3-bit digital to time converter and provides 7 levels of delay amount. Current starving and MOSCAP load is used like in delay1. The inverter is always current starving and different delay amount is obtained by enable and disable load capacitors. Fig.2 (d) shows the schematic of delay3 which is a 3-bit digital to time converter and provides 7 levels of delay amount. 7 small capacitors are connected to the output of inverter to generate time delay. Different amount of delay is obtained by enable and disable load capacitors.



(a). Block diagram of phase control



(b) Time sequence

Fig.3. Phase control of triangular wave

Most transistors in the DTC have minimum size except some load capacitors that are only several times larger than minimum size. Therefore layout of the DTC is very compact. No technique is employed to improve linearity of the DTC. Thus this 8-bit 3-step DTC may be very nonlinear and even not monotonic. But nonlinearity and nonmonotonicity will not affect the histogram testing which will be shown in Section IV.

B. Control Circuits

In order to complete data acquisition and testing, control circuit and decoder are needed. The block diagram in Fig.3 (a) shows how the signal generator, ADC, and control circuits work together. The block right after the 14 bits ADC detects if the input signal goes out of reference voltage of the ADC and outputs signal "ends". The signal "ends" becomes high when output of the ADC is all zero or all one. The 8-bit DTC takes "ends" as input and outputs the delayed version "ends_d". The rising edge of "ends_d" controls the charging and discharging circuit. The "ends_d" is converted to wide pulse "ctrl_ramp" by a DFF first, and then the wide pulse opens charging or discharging current. The signal "ends" is also input of the 8-bit counter which counts the number of ramp. Based on the output of the counter, certain amount of time delay is generated by DTC. The decoder block between them converts 8 bits output of counter into 17 bits control signal of DTC.

Time sequence of some important signal is shown in Fig.3 (b). First, output of signal generator is reset to low voltage and counter is cleared. Then the triangular wave

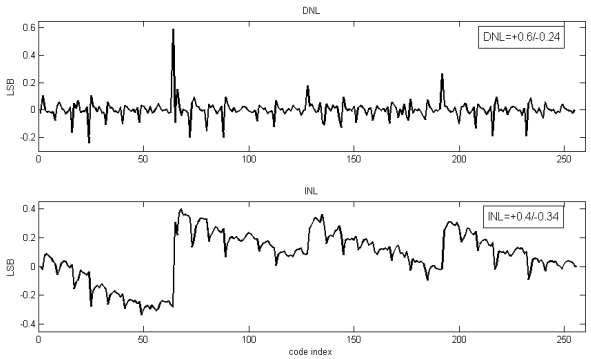


Fig.4. DNL and INL of 8-bit DTC

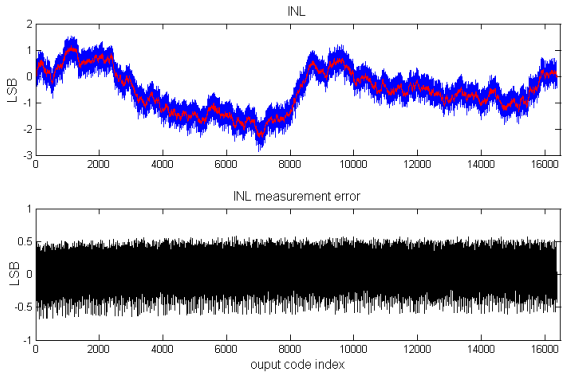


Fig.5. INL estimation using delayed triangle

starts to ramp up. "ends" goes high when the triangular wave becomes higher than reference voltage. Three blocks including detect ends, 8-bit counter, and decoder are synthesized by digital tools. The whole phase and test control circuits needs a number of gates equivalent to about 240 minimum sized inverter gates.

IV. SIMULATION RESULTS

The 8-bit digital to time converter and control circuits have been implemented in AMI 0.6um process. Fig.4 shows the simulation results of the 8-bit DTC that contains DNL and INL curve. Maximum value of DNL and INL of the DTC is 0.6 LSB and 0.4 LSB respectively. 0.4 LSB is about 16 ps in time, and 1.6 uV in voltage according to the ramp slope mentioned in section II. The DTC causes 0.03 LSB input voltage error for 14-bit ADC testing. In both DNL and INL curve, three big jumps can be observed. These jumps happen when delay2 and delay3 are disabled and delay1 is enabled. The reason is that level of delay1 is 2.5 ns and error of this number is large comparing to one LSB. In addition, we can also observe more smaller jumps that caused by transition from delay3 to delay2.

In the simulation of whole control circuits in Fig.3, all blocks are implemented at transistor level except stimulus generator and 14-bit ADC. The purpose is to avoid other non-ideal factors so that control circuits can be better validated. Delayed triangular wave is generated in Cadence and used as stimulus to test a 14-bit ADC in MATLAB. The measured INL curve is shown in Fig.5 in which red curve is

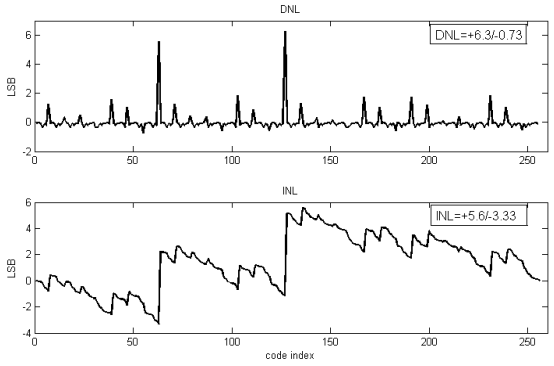
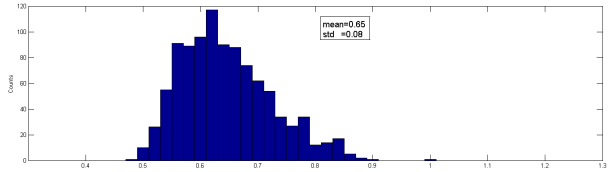
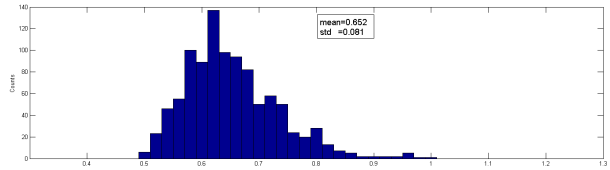


Fig.6. DNL and INL of DTC with worse linearity



(a). Ideal triangle and ideal delay



(b). Ideal triangle and delay with random error

Fig.7. INL estimation error of two cases

the true INL and blue curve is the INL measured from delayed triangular wave. Difference between them is shown in black curve which is also the INL measurement error. The INL measurement error is mainly caused by noise in the stimulus and the maximum value is 0.67LSB.

The 8-bit digital to time converter shows good linearity in simulation because there is no process variation. In reality, process variation of capacitor and current source will make the linearity much worse. In order to investigate how delay variation cause data acquisition and testing accuracy problem, simulations have also been done in MATLAB. A 14-bit flash ADC is modeled as a set of transition levels and randomly generated for testing. The 8-bit 3-step digital to time converter is also modeled in MATLAB and random error is added to each delay. Fig.6 shows the DNL and INL curve of the DTC when random delay error is added to delay1, delay2, and delay3 respectively. These delay errors are Gaussian distributed and the standard deviation is chosen to be 10% of delay amount based on rough consideration of bias current and area. Specifically, standard deviation of the delay error added to delay1, delay2, and delay3 is 0.25 ns, 32ps, and 4ps respectively. Similar to Fig.4, two big jumps are presenting in DNL and INL curve. But jumps are much larger in Fig.6 and jumps generated by disabling delay3 and enabling delay2 are also large.

To show how errors of delay affect the INL estimation accuracy, two different cases are compared. In the first case, 127 periods of triangular wave is used as stimulus in standard histogram testing. Every ramp in the triangular wave is ideally linear and is delayed by ideal amount of time. The second case is similar as the first case, but the difference is that delay error with 10% standard deviation is added to each delay in this case. In both cases, 0.5 LSB additive noise is added to the triangular wave. Fig.7 shows histogram of INL estimation error of each case which is obtained by testing 1000 different ADCs. It can be seen that 10% delay error increases the INL estimation error very little. The INL estimation error and spread of this error is mainly caused by input noise and number of sample per code. More simulation results are shown in Table.1 and Table.2 with different delay error. Table.2 is obtained when nonlinear triangular wave and stimulus error identification and removal (SEIR) method [4] is used to estimate INL. It can be seen from tables that 10% random delay error causes insignificant extra error to INL estimation.

Table.1. INL estimation error in standard histogram testing

delay error	**0%**	**5%**	**10%**	**20%**	**30%**
mean (LSB)	0.65	0.65	0.65	0.67	0.71
std (LSB)	0.08	0.08	0.081	0.084	0.1

Table.2. INL estimation error in SEIR method testing

delay error	**0%**	**5%**	**10%**	**20%**	**30%**
mean (LSB)	0.686	0.691	0.693	0.712	0.738
std (LSB)	0.088	0.084	0.085	0.094	0.102

V. CONCLUSION

In ADC production testing, coherent sampling is realized by accurately controlling the frequency of input signal. However accurate control of frequency is not applicable for ADC BIST due to large area of frequency synthesizer. A phase control scheme is proposed in this paper to realize coherent sampling. The phase is changed by delaying each ramp of the triangular wave. An 8-bit DTC, together with other simple control circuits, is designed for a 14-bit 100MSamples/s ADC INL testing. Simulation results show good measurement accuracy when delayed triangular wave is used as stimulus. Measurement results are very robust to nonlinearity of the DTC.

REFERENCES

[1] IEEE Std 1241-2000. "IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters." 2000

[2] J. Doernberg, H.-S. Lee, and D. A. Hodges, “Full-speed testing of A/D converters,” IEEE J. Solid-State Circuits, vol. SC-19, pp. 820-827, Dec 1984.

[3] M. Renovell, F. Azaïs, S. Bernard, and Y. Bertrand, “Hardware resource minimization for histogram-based ADC BIST,” in Proc. 18th IEEE VLSI Test Symp., 2000, pp. 247-252.

[4] L. Jin, K. Parthasarathy, T. Kuyel, D. Chen and R. L. Geiger, “Accurte Testing of Analog-to-Digital Converters Using Low Linearity Signals With Stimulus Error Identification and Removal,” IEEE Trans. Instrum Meas., vol. 54, pp. 1188 – 1199, June 2005.

[5] J. Duan, D. Chen, R. Geiger, “Cost effective signal generators for ADC BIST,” IEEE International Symposium on Circuits and Systems, pp. 13-16 May, 2009.