

# INL Based Dynamic Performance Estimation for ADC BIST

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**Abstract**—Data acquisition time and accurate instrumentation are the most significant contributors to ADC test cost. For most ADC products, static linearity (INL/DNL) test is required. This paper presents a methodology for estimating an ADC's dynamic performance from its tested INL data, without requiring additional data acquisition or additional accurate sinusoidal sources. The tested INL(k) data is used to compute the power at harmonic frequencies and estimate ADC's dynamic specifications such as THD and SFDR. Memory and computation requirement is very small comparing to that in traditional spectral testing. When combined with a BIST approach for INL testing, this method offers a very low cost BIST solution to ADC dynamic performance testing. Both simulation and experimental results show that the proposed method can estimate THD and SFDR values accurately.

## I. INTRODUCTION

In analog-to-digital converter (ADC) production, linearity and dynamic performances are two major categories of specifications to be tested. The linearity performance, including INL and DNL, is conventionally tested by using the histogram method with either a sine wave or triangular wave input. The dynamic performance, including SNR, THD, and SFDR, is tested by using the FFT method with a single tone sine wave input [1].

To reduce test time, researches have been done to estimate linearity performance of an ADC based on dynamic testing results [2]. As a trade-off for test time, the "high-frequency" details of the INL pattern are lost due to insufficient information on ADC's transition levels. This accuracy limitation will prevent adoption of such methods in real applications. This paper takes another direction to achieve test time reduction by trying to estimate the dynamic performance based on linearity test results. At a first glance, it seems that saving time of dynamic testing is not as attractive as reducing linearity test time. However, it is much more straightforward to compute dynamic parameters very accurately based on the large number of samples already captured for linearity test, as compared to predicting DNL and INL from a limited number of samples. Furthermore, dynamic test time is not negligible in a properly optimized testing procedure, and significantly reducing it will meaningfully reduce the total test cost.

The idea of estimating the dynamic performance using linearity test data becomes more valuable in applications of

ADC built in self test (BIST), where testing circuitry's area is more concerned than test time. Recently, research results have been published on reducing the accuracy requirement on linearity testing signal and simplifying its generation circuitry, which makes it possible to realize ADC linearity test on chip [3, 4]. Using the method developed in this paper, it only takes very little resources to obtain the dynamic performance of an ADC based on BIST results of its linearity. This method eliminates the need of accurate sine wave generation on chip for dynamic test, making ADC BIST one step easier to implement.

In this paper, a method of estimating THD and SFDR based on INL of an ADC is introduced. The method computes THD and SFDR without requiring any additional hardware or data acquisition. Only a small amount of computation is required to estimate THD and SFDR accurately. The rest of this paper is organized as following. In Section II, the INL based dynamic performance estimation method is described. Issues of implementation and computation reduction are also discussed in this section. In Section III, simulation results are given for detailed investigation. Experimental results are given in Section IV.

## II. INL BASED DYNAMIC ESTIMATION

Dynamic performance of ADC includes SNR, THD, and SFDR. The traditional testing of dynamic performance is performed in frequency domain. A single tone sine wave is used as the input of ADC under test, and then the FFT of digital outputs is computed. From the spectrum of output signal, THD and SFDR can be calculated from harmonics power.

Traditional testing method has high requirements on input sine wave generator. Output noise of the generator should be much smaller than the input referred noise of ADC. The generator should be able to generate sine wave with proper frequency so that coherent sampling can be achieved. The sine wave needs to be highly linear to approximate a single tone input. Building such a sine wave generator on chip with low cost is challenging. However, INL can be tested with low overhead by adopting SEIR method. Computing dynamic performance from INL data becomes a good approach, which needs only very small amount of hardware resources. In this section we will show that these parameters can be computed from INL data of the ADC.

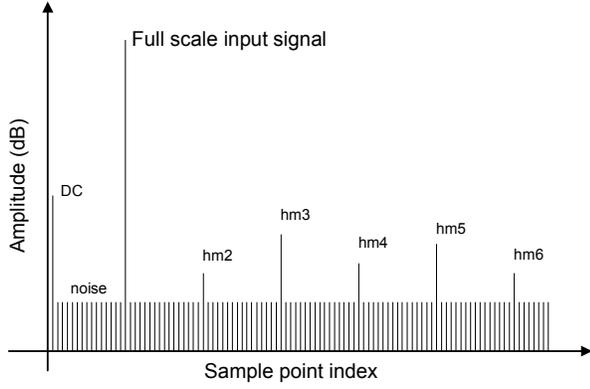


Fig.1. Spectrum of output signal

#### A. Estimating Distortion Power From INL Data

The ADC testing process can be described in a new way as following. The transfer characteristic of a real ADC can be represented by equation (1).

$$V_{in}(t_k) + n(t_k) = T_{C(t_k)} + E_{os} + \frac{C(t_k)}{2^n} E_g + Q(t_k) \quad (1)$$

In this equation,  $t_k$  is the testing time index,  $V_{in}(t_k)$  is the input voltage at time  $t_k$ ,  $n(t_k)$  is the input referred noise including noise from signal source and ADC itself,  $C(t_k)$  is the output code at time  $t_k$ ,  $T_{C(t_k)}$  is the transition voltage corresponding to output  $C(t_k)$ ,  $Q(t_k)$  is the quantization error at time  $t_k$ ,  $E_{os}$  is the offset, and  $E_g$  is the gain error of the ADC. Continuous input signal is represented by discrete transition voltages with error. After INL has been measured, the transition voltage corresponding to output  $C(t_k)$  can be calculated by equation (2)

$$T_{C(t_k)} = C(t_k) \cdot LSB + INL_{C(t_k)} \quad (2)$$

in which,  $INL_{C(t_k)}$  is the INL error of transition level  $T_{C(t_k)}$ . Equation (3) can be obtained by substituting (2) into (1) and switching sides.

$$\begin{aligned} C(t_k) \cdot LSB + \frac{E_g}{2^n} C(t_k) \\ = V_{in}(t_k) + n(t_k) - Q(t_k) - INL_{C(t_k)} - E_{os} \end{aligned} \quad (3)$$

$C(t_k) \cdot LSB$  is the measured data of ADC. All values of  $C(t_k) \cdot LSB$  over the testing time  $0 \leq t_k \leq 1$  represents the input signal which is a single tone sine wave. The dynamic performance is measured by compare spectrum of  $C(t_k) \cdot LSB$  to that of an ideal single tone sine wave.

After Fourier transform, equation (3) becomes

$$\begin{aligned} FT(C(t_k) \cdot LSB) \\ = \left( 1 + \frac{E_g}{2^n} \right) \cdot \left\{ FT(V_{in}(t_k)) + FT(n(t_k) - Q(t_k)) \right. \\ \left. - FT(INL_{C(t_k)}) - FT(E_{os}) \right\} \end{aligned} \quad (4)$$

In this equation,  $FT(C(t_k) \cdot LSB)$  is the Fourier transform of ADC output voltage,  $FT(V_{in}(t_k))$  is the Fourier transform of

input signal,  $FT(n(t_k) - Q(t_k))$  is the noise floor,  $FT(INL_{C(t_k)})$  is the harmonic distortion caused by nonideal ADC, and  $FT(E_{os})$  is the part DC component from ADC offset. Fig.1 shows a typical spectrum of a digitized sine wave contains all components in equation (4). Signal power, harmonic distortion power, and noise power can be computed from the spectrum and eventually SNR, THD, and SFDR can be computed.

It can be observed that all harmonic distortion power in equation (4) is carried by  $FT(INL_{C(t_k)})$  term. Spectrum of INL data contains the same harmonic distortion power as the spectrum of digital output data shown in Fig.1. To achieve the purpose of computing THD and SFDR value, we only need to do Fourier transform of INL instead of output codes. All harmonic distortion power can be calculated from INL spectrum. This computation only needs simple on chip DSP which is available in SoC. In other words, THD and SFDR can be computed from INL without any extra hardware for ADC BIST in SoC. Another advantage of this approach is that noise is much lower than normal digital output because of average effect of histogram testing. The  $FT(INL_{C(t_k)})$  term actually carries both harmonic distortion power and reduced input referred noise which is very small. The input referred noise and SNR may also be computed from INL or DNL as long as how much noise is reduced by histogram test is know.

#### B. Implementation Consideration

In INL testing, either sine wave or triangular wave can be used as stimulus. The common point is that the stimulus is always a low frequency signal. Even if the INL is tested from a high frequency stimulus, average effect of histogram makes all data lie on half period of input signal as if the stimulus has very low frequency. Thus the original INL data carries the distortion information experienced by very low frequency input signal. If INL is tested from a ramp signal, spectrum of original INL data is similar as the spectrum of a ramp signal. Harmonic distortion power cannot be calculated from such spectrum.

For convenient computation, harmonics should distribute with certain distance in the spectrum plot. In traditional dynamic testing, a sine wave with certain frequency is applied to ADC. Distortion information carried by output code is the distortion experienced by the sine wave, which means that the distortion term  $FT(INL_{C(t_k)})$  in equation (4) is the INL experienced by sine wave instead of original INL data. To obtain INL corresponding to the input sine wave, we need to know output code of the ADC, which is not available. Instead, the code is generated by virtual testing of sine wave.

Assume a sine wave has frequency of  $f_0$  and amplitude of 1. An ideal ADC with the same full scale range converts this sine wave into digital codes which can be simply calculated by

$$C(k) = \lfloor N \cdot \sin(2\pi f_0 \cdot t_k) \rfloor \quad k = 1, 2, 3 \dots M \quad (5)$$

in which,  $N$  is the number of transition level of ADC,  $M$  is the total number of samples, and  $C(k)$  is the output code. Now  $C(k)$  can be used as the index to read the value of  $INL_k$  from the original INL data and construct a new data set  $INL_{sin}$ . The new data set has  $M$  points in total and same frequency as sine wave. It is worth noting that  $C(k)$  is different from the actual output code of ADC. The difference will not affect harmonic distortion power. The reason is that  $C(k)$  is only several codes away from  $C(t_k)$  and the value of  $INL_i$  changes very slowly so that  $INL_{C(k)}$  is almost equal to  $INL_{C(t_k)}$ . Even in pipeline ADC, several jumps in INL curve will not affect estimation results.

Constructing a new data set from INL according to sine wave does not change distortion power. Frequency of the sine wave in (5) can be selected to be any value that makes computation convenient. The frequency is selected to be about 20 times smaller than the sampling frequency. Total power of first 20 harmonics can be calculated without large influence and THD and SFDR can be calculated from (6) and (7) respectively

$$THD = 10 \cdot \lg \left( \frac{\sum(P_{hm})}{P_s} \right) \quad (6)$$

$$SFDR = 10 \cdot \lg \left( \frac{P_s}{\max(P_{hm})} \right) \quad (7)$$

In these two equations,  $P_{hm}$  is the harmonics power, and  $P_s$  is signal power which is  $A^2/8$  for full scale input sine wave.

### C. Reducing Computation Requirement

Though the Fourier transform of INL can be easily computed by on chip processor, the computation can be further simplified. To calculate THD and SFDR, we only need distortion power assuming full scale input signal is applied. Instead of implementing FFT algorithm, discrete-time Fourier series (DFS) of INL is computed as (8).

$$X(k) = \frac{1}{N} \sum_{n=0}^{N-1} x(n) \cdot e^{-j \frac{2\pi}{N} n \cdot k} \quad k = 0, 1, 2, \dots, N-1 \quad (8)$$

In which,  $x(n)$  is the value of  $INL_n$ ,  $X(k)$  is the  $k^{th}$  coefficient,  $N$  is the number of points. The coefficient of the fundamental component is given by (9)

$$X(k_1) = \frac{1}{N} \sum_{n=0}^{N-1} x(n) \cdot e^{-j \frac{2\pi}{N} n \cdot k_1} \quad (9)$$

The relation between input signal frequency and sampling frequency is set beforehand, thus value of  $k_1$  is known. Coefficient of  $i^{th}$  order harmonic can be calculated by (10)

$$X(i \cdot k_1) = \frac{1}{N} \sum_{n=0}^{N-1} x(n) \cdot e^{-j \frac{2\pi}{N} n \cdot i \cdot k_1} \quad i = 2, 3, 4 \dots \quad (10)$$

There is no need to calculate fundamental component since it is not the power of input signal or part of distortion power. Only 19 coefficients need to be calculated for good estimation of THD and SFDR. The frequency of input sine

wave is selected by tester so that value of  $k_1$  is always known, and the resolution of ADC is also known. Instead of creating a look up table for exponential term, only the exponential value corresponding to  $n$  needs to be stored on chip and used for DFS coefficient computation.

## III. SIMULATION RESULTS

The method of estimating THD and SFDR from INL data has been investigated and validated by simulations. ADCs under test are 16 bits flash ADCs randomly generated in MATLAB. Fig.2 shows the original ADC INL curve which is tested from a ramp signal with 0.5LSB input noise. Fig.3 shows the constructed new data set from original INL according to sine wave. As shown in equation (5), the sine wave is converted into digital code and the total number of sample is 8192. 165 periods are generated so that first 20 harmonics are distributed within half sampling frequency.

Fig.4 compares the spectrum of traditional FFT testing which is drawn in red line and the spectrum of the constructed data set which is drawn in blue. Fundamental frequency in two cases is set to be identical for convenient comparison. It can be observed from this plot that spectrum of the constructed data set has the same harmonic distortion power as the spectrum of digital output. The zoomed in plot of the 3<sup>rd</sup> harmonic shows more detail of this. Another observation is the noise floor of INL spectrum is much lower than that of FFT testing, which is an advantage of INL based estimation.

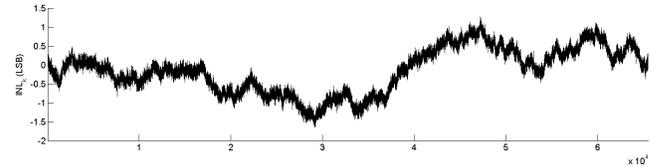


Fig.2. Original INL curve

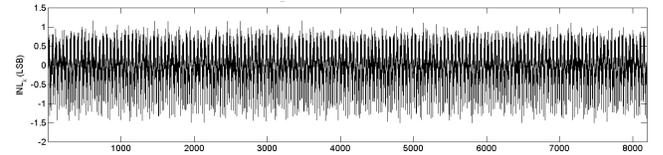


Fig.3. INL experienced by 165 sine wave periods

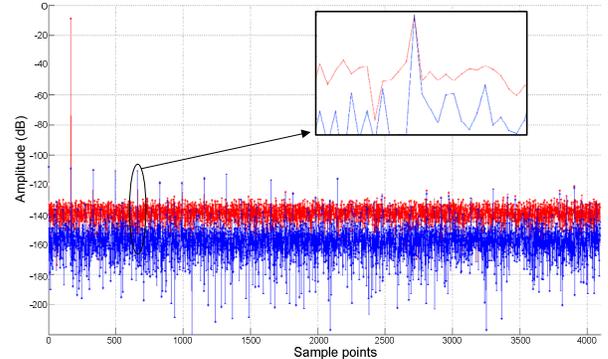


Fig.4. Spectrum of output code and rearranged INL

Table.1. Estimation error of different number of points

Points	512	1024	2048	4096	8192
$\Delta(\text{THD})$ (dB)	-0.06	-0.07	-0.06	-0.01	-0.01
$\Delta(\text{SFDR})$ (dB)	-0.13	0.05	0.013	0.01	-0.04

Table.2. Estimation error of different ADC

INL (LSB)	0.3	0.63	0.95	1.25	1.6
THD (dB)	-106.4	-101.8	-98.6	-96.2	-94.3
$\Delta(\text{THD})$ (dB)	-1.78	-0.45	-0.12	-0.07	-0.04
$\Delta(\text{SFDR})$ (dB)	0.6	0.43	0.03	0.23	0.03

Although the same number of sample as traditional FFT testing is used in Fig.4, only a small number of points are needed in the estimation. Table.1 shows INL based estimation error versus number of points comparing with testing result of 8192 points traditional FFT. The ADC used in these estimations has the following performance, INL is +1.2/-1.7LSB, SNR is 91.85dB, THD is -94.34dB, and SFDR is 100.83. In this table, estimation accuracy becomes worse when a smaller number of points are used, but all cases gives accurate enough estimation.

Table.2 shows estimation errors of THD and SFDR of ADCs with different INL. It can be seen that estimation accuracy of THD becomes better when INL becomes larger or THD becomes worse. The reason is harmonic distortion power becomes larger, the effect of noise becomes smaller.

#### IV. EXPERIMENTAL RESULTS

The INL based method of estimating THD and SFDR has also been validated from measurement. Four different 16 bits SAR ADCs are tested by both traditional testing method and INL based method. All ADCs are tested by 32768 points traditional FFT method which will be regard as the reference. Performances of these four ADCs are listed in Table.3, in which INL varies from 0.9 LSB to 2 LSB and THD varies from -103 dB to -91 dB. ADCs with various performances provide better validation.

The 2<sup>nd</sup> column of Table.4 is the number of samples used in INL based estimation. It can be seen that very good estimation accuracy can be achieved by a number samples that is much smaller than traditional FFT testing. The 3<sup>rd</sup> column is the direct subtraction of THD value tested by INL based method and THD value tested by traditional FFT testing. The 4<sup>th</sup> column is the difference of distortion power acquired in two methods. The 5<sup>th</sup> column is the same as the 3<sup>rd</sup> column but SFDR value. The 6<sup>th</sup> column is the difference of largest harmonic distortion power from two methods.

From Table.4, we can see the same rule as from Table.2, which is the estimation becomes more accurate when distortion becomes worse. The value of  $\Delta(\text{THD})$  of ADC1 is the worst among these four ADCs. But this does not mean the INL based method gives bad estimation for ADC1. The 4<sup>th</sup> column shows that estimation of distortion power of ADC1 is actually very accurate. The noise floor of ADC1 is about -143.51dB, and the effect of total distortion power

Table.3. Performance of four ADCs

	INL(LSB)	SNR(dB)	THD(dB)	SFDR(dB)
ADC1	+0.95/-0.54	92.2	-103.6	106.8
ADC2	+1/-1.27	92	-97.5	102.8
ADC3	+1.83/-1.83	91.8	-90.8	95.1
ADC4	+2.01/-1.98	91.4	-91.3	95.5

Table.4. Estimation error of ADC1 (Unit: dB)

	Points	$\Delta(\text{THD})$	$\Delta(\text{Pd})$	$\Delta(\text{SFDR})$	$\Delta(\text{Ph}_{\text{max}})$
ADC1	1024	-1.33	-119.06	0.09	-144.69
	2048	-1.27	-119.26	0.12	-138.63
	4096	-1.13	-119.74	-0.17	-127.88
ADC2	1024	-0.39	-118.82	-0.32	-121.74
	2048	-0.34	-119.52	-0.30	-121.97
	4096	-0.31	-120.14	-0.46	-120.49
ADC3	1024	-0.12	-124.95	0.52	-114.67
	2048	-0.18	-117.40	0.61	-113.91
	4096	-0.24	-115.18	0.64	-113.63
ADC4	1024	0.07	-114.33	0.02	-121.51
	2048	0.05	-114.72	0.00	-120.76
	4096	0.05	-114.84	0.03	-121.95

from noise is -125.95dB. Besides, noise floor in INL spectrum will also have effect on distortion power estimation, which will increase the effect up to about -123dB. The estimation error in total distortion power is very close to noise effect. On the whole, Table.4 shows that the INL based method gives good enough estimation of THD and SFDR.

#### V. CONCLUSION

Accurate INL testing of an ADC is required by many applications and can be implemented on chip with low cost. Under the condition that INL has been tested, testing dynamic parameters such as THD and SFDR by another round of data collection is not necessary. An INL based method of estimating THD and SFDR is presented in this paper. This method needs no additional hardware resource and little computation. Simulation and experimental results show that the estimation error of THD and SFDR using the proposed method is comparable to noise effects and good enough for real world applications.

#### REFERENCES

- [1] J. Doernberg, H.-S. Lee, and D. A. Hodges, "Full-speed testing of A/D converters," IEEE J. Solid-State Circuits, vol. SC-19, pp. 820-827, Dec 1984.
- [2] F. Adamo, F. Attivissimo, N. Giaquinto and M. Savino, "FFT test of A/D converters to determine the integral nonlinearity," IEEE Trans. Instrum. Meas., vol. 51, pp. 1050, Oct. 2002.
- [3] L. Jin, K. Parthasarathy, T. Kuyel, D. Chen and R. L. Geiger, "Accurate Testing of Analog-to-Digital Converters Using Low Linearity Signals With Stimulus Error Identification and Removal," IEEE Trans. Instrum Meas., vol. 54, pp. 1188 – 1199, June 2005.
- [4] J. Duan, D. Chen, R. Geiger, "Cost effective signal generators for ADC BIST," IEEE International Symposium on Circuits and Systems, pp. 13-16 May, 2009.