Detailed Analyses in Prediction of Capacitive-Mismatch-Induced Offset in Dynamic Comparators

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***Abstract*—Due to the positive feedback and the time varying clock signal, the operating point of each transistor in dynamic comparators is time varying and cannot be analyzed using traditional Op-Amp-based small signal analysis. Until recently, a balanced method is proposed to effectively get the analytical models for random offset caused by variations in process parameters. Meanwhile, it has been shown that mismatches from parasitic capacitors are also significant contributors to overall offset. However, the energy storage and nonlinear feature of capacitor make it even more challenging to analytically predict the capacitive mismatch induced offset. In this work, the previous proposed balance method is generalized and applied to tackle the problem of capacitive mismatch induced offset. The analytical models are derived to explicitly show offsets caused by capacitor mismatch at different internal nodes. The insights are obtained on identifying the sensitive nodes to capacitor mismatch and on how to reduce the offset. The numerical example validates the effectiveness of the analytical models.**

I. INTRODUCTION

Comparators are used in a wide variety of circuit applications, such as analog-to-digital converter, data transmission, switching power regulator, memories, dynamic logic, sensing amplifier, etc. There are mainly three types of comparators: Op-Amp based comparators, pre-amplifier followed by dynamic latch comparators and pure dynamic comparators [1]. Among the three types, dynamic comparators have the merits of fast speed, zero static power consumption, small area, and therefore serve as fundamental building blocks in high performance analog-to-digital converters. Since they are decision-making circuits that compare two analog signals and deliver a logical value at the output, the accuracy, which is often limited by its input referred offset voltage, is essential for the resolution of high performance ADCs.

Neglecting error sources from external circuit, such as timing error of clock signal and variation of reference voltages, the offset voltage in a dynamic comparator is mainly caused by two types of mismatch: (1) static mismatch from variations in process parameters, which are normally dominated by mismatch in μC_{ox} and threshold voltage V_{th}; (2) dynamic mismatch from internal parasitic capacitors' mismatch. In previous work [2], "balanced method" has been introduced to analytically predict the static offset from variations in process parameters. Most literatures are focusing on reducing the static offset. The methods are proposed, such as increasing W and L of transistors, drawing the matching critical pairs as symmetrical as possible [3] [4].

By contrast, dynamic offset caused by mismatch of internal parasitic capacitor is less understood and more challenging to be analytically predicted. However, offset contributed from internal capacitor mismatch is not trivial. In [5]-[7], the authors pointed out 1fF or 2fF can lead up to several tens of milivolts offset. In [5], the authors use a simple two-inverter latch as an example to analyze load capacitor mismatch. For other well known dynamic comparator topologies in [4] [8], the same analyses will be too tedious to apply. Also, the model is only for capacitive mismatch at the output node. However, we observed that, besides the output node, some other internal nodes also contribute significant amount of offset. In previous work [9], some preliminary results from simulations are given to show the considerable offset from capacitive mismatch. Design intuitions to reduce offset are obtained from simulations. One model is developed for mismatch at output node. In this work, we developed an efficient way to establish the analytical models for capacitive mismatch at different nodes and obtained the insights on how to reduce the capacitive-mismatch-induced offset using the analytical model.

In section II, the proposed "balanced method" for static offset analyses is briefly reviewed. A simple example is given to explain how to apply the same approach to address capacitive mismatch induced offset. In section III, a detailed procedure is given on how to analytically evaluate capacitive mismatch offset in "Lewis-Gary" structure. In section IV, numerical example is given to validate the effectiveness of the proposed models. Section V concludes the paper.

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II. BALANCED METHOD

Due to internal positive feedback and time varying clock signal, the operation region of each transistor is time dependent during each clock period, and how it changes depends on input signal level. Therefore, it is a time-varying non-linear system. In this system, predicting offset becomes very challenging. In [2], we proposed the balance method to evaluate offset voltage from mismatch in V_{th} and μC_{ox}. The method can also be applied to predict capacitive-mismatch-induced offset.

We would like to introduce the term of balanced mode and the conditions to realize this mode, because they are the core concepts of the proposed balanced method and significantly simplify the analyses of static offset and also capacitive-mismatch-induced offset.

A. Condtions for balanced mode

A typical dynamic comparator [8] as shown in Fig.1 can be divided into two halves: left half and right half. Each component in left half has its counterpart in the right half to form a pair, for instance, M_5 and M_6 form a pair. Under balanced mode, the two devices within one pair are supposed to be identical in all characteristics including: device type, physics size, process parameters, external bias, operation point, parasitic capacitors, etc. No device mismatch or process variation is presented. Even though dynamic comparators have periodical clock signals and have time varying operation points, under the balance mode, the counterparts in each pair will follow the identical time trajectory of operation points as illustrated in Fig. 1. For instance, time varying node voltage $V_{out+}(t)$, $V_{s7}(t)$, $V_{s5}(t)$ are the same as $V_{out-}(t)$, $V_{s8}(t)$, $V_{s6}(t)$ respectively through the whole clock cycle, where the subscript s means the source of the transistor. Along the time trajectory, we can do linearization and small signal analysis. When the mismatch or small disturbance occurs, ΔV_{in} equal to the input offset voltage is applied to the input terminal to cancel the imbalance effect and to keep the circuit still at or very close the balance mode as no mismatch or variation is presented.

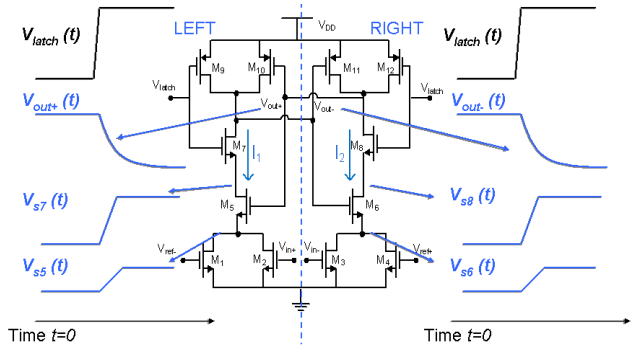

Figure 1. Dynamic comparator under balanced mode.

B. Capacitive mismatch induced offset prediction using balance mode concept

Capacitive mismatch induced offsets are due to internal parasitic capacitor and are only shown during transient process. A four-terminal MOS device includes twelve different parasitic capacitors [10]. The differential equations with respect to time will get involved to analyze the type of offset because capacitor is non-linear and energy storage component. All the above factors make the offset analyses become very challenging. The concept of balance mode can be applied to facilitate the analyses. As the example in Fig.2, ΔC demonstrates the overall equivalent mismatch capacitor at the summing drain nodes of M_3 and M_4. Two KCL (Kirchhoff's Current Law) equations can be expressed as

$$I_L = I_1 + I_2 + \Delta I + I_{cap\_db1} + I_{cap\_dg1} + I_{cap\_db2} + I_{cap\_dg2} \quad (1)$$

$$I_R = I_3 + I_4 + I_{cap\_db3} + I_{cap\_dg3} + I_{cap\_db4} + I_{cap\_dg4} + \Delta C \cdot \frac{dV_{D4}}{dt} \quad (2)$$

where I_1, I_2, I_3, I_4 are channel currents through M_1-M_4, respectively. I_{cap_dbi}, I_{cap_dgi}, I_{cap_dbi}, I_{cap_dgi} (i=1, 2, 3, 4) are capacitor charging currents through the parasitic capacitor between two terminals of the transistor M_1-M_4. They can be calculated through the following way

$$I_{cap\_dbi} = C_{dbi} \cdot \frac{d(V_d - V_b)}{dt} \quad i = 1,2,3,4 \quad (3)$$

where d and b mean drain and substrate terminal of a transistor M_i, respectively. I_{cap_dgi}, I_{cap_dbi}, I_{cap_dgi} (i=1, 2, 3, 4) can be found using the similar way.

Under the balance mode, it is satisfied that

$$I_L = I_R, I_1 = I_3, I_2 = I_4 \quad (4)$$

$$I_{cap\_db1} = I_{cap\_db3}, \; I_{cap\_db1} = I_{cap\_db3}$$

$$I_{cap\_db2} = I_{cap\_db4}, \; I_{cap\_dg2} = I_{cap\_dg4} \quad (5)$$

Subtract (2) from (1) and apply the conditions (4)-(5)

$$\Delta I = \Delta C \cdot \frac{dV_{D4}}{dt} + (I_3 + I_4) - (I_1 + I_2) \approx \Delta C \cdot \frac{dV_{D4}}{dt} \quad (6)$$

Since $\Delta I = G_{m2} \cdot \Delta V_{in} + g_{ds2} \cdot \Delta V_{ds} \approx G_{m2} \cdot V_{os}$ (7)

The finite output impedance in (7) is neglected to simplify the derivation. From (6) and (7), the offset voltage can be solved as

$$V_{os} = 1/G_{m2} \cdot \Delta C \cdot dV_{D4}/dt \quad (8)$$

where G_{m2} is the transconductance of M_2. Note that G_{m2} and dV_{D4}/dt have certain time trajectory within the clock cycle. Here we use G_{m2} and dV_{D4}/dt values under the balanced mode at the moment when V_{latch} is just rising up to V_{DD}. That moment is also supposed to be the time when differential output nodes are released from reset value V_{DD} and begin to drop. Once the time point is determined, G_{m2}, which is comprised of process parameters, aspect ratios and bias point, can be calculated using the approach in [2]. The dV_{D4}/dt value can be obtained by measuring the slope of V_{D4} during the short time period right after V_{latch} rises up to V_{DD}.

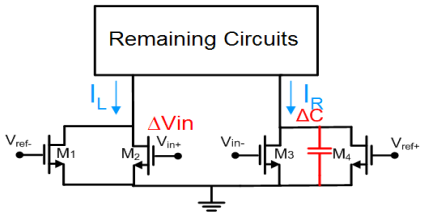

Figure 2. Mismatch from internal capacitor

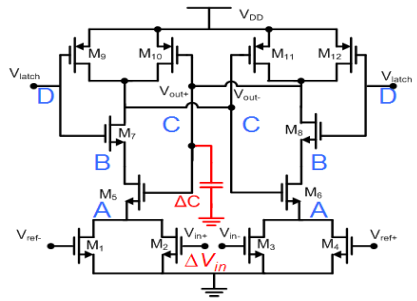

Figure 3. "Lewis-Gary" structure within internal paracitic capacitor

III. CAPACITIVE MISMATCH INDUCED OFFSET IN "LEWIS-GRAY" STRUCTURE

The method in section II can be applied to analyze capacitive mismatch in each internal node in more complex structure. As "Lewis-Gary" structure shown in Fig. 3 [8], there are mainly four pairs of internal nodes: *A*, *B*, *C* and *D*. First, consider the capacitive mismatch occur at differential output nodes V_{out+} and V_{out-}. ΔC in Fig. 4 is the equivalent total mismatch capacitor at the pair of nodes *C*. Assume that there is no other mismatch component. Apply KCL at the source of M5 and M6, respectively.

$$\Delta I + I_1 + I_2 + C_{db1}\cdot\frac{dV_{s5}}{dt} + C_{gd1}\cdot\frac{d(V_{s5}-V_{ref-})}{dt} + C_{gd2}\cdot\frac{d(V_{s5}-V_{in+})}{dt}$$
$$= I_5 + C_{bs5}\cdot\frac{d(0-V_{s5})}{dt} + C_{gs5}\cdot\frac{d(V_{out+}-V_{s5})}{dt} \quad (9)$$

$$I_3 + I_4 + C_{db3}\cdot\frac{dV_{s6}}{dt} + C_{gd3}\cdot\frac{d(V_{s6}-V_{in-})}{dt} + C_{gd4}\cdot\frac{d(V_{s6}-V_{ref+})}{dt}$$
$$= I_6 + C_{bs6}\cdot\frac{d(0-V_{s6})}{dt} + C_{gs6}\cdot\frac{d(V_{out-}-V_{s6})}{dt} \quad (10)$$

Under balance mode, it is satisfied that

$$I_1 = I_3,\ I_2 = I_4,\ I_5 = I_6 \quad (11)$$

$$C_{db1} = C_{db3}, C_{gd1} = C_{gd3}, C_{gd2} = C_{gd4}, C_{bs5} = C_{bs6}, C_{gs5} = C_{gs6} \quad (12)$$

$$V_{ref-} = V_{in-},\ V_{in+} = V_{ref+},\ V_{out+} = V_{out-} \quad (13)$$

The condition that $V_{out+} = V_{out-}$ is imposed because when the mismatch component and compensation voltage ΔV_{in} at the input are both present, the circuit is supposed to realize $V_{out+} - V_{out-} = 0$. Subtract (10) from (9) using (11)-(13)

$$\Delta I \approx -(C_{db1} + C_{gd1} + C_{gd2} + C_{bs5} + C_{gs5})\cdot\frac{d(V_{s5}-V_{s6})}{dt} \quad (14)$$

Then apply KCL at node V_{out+} and V_{out-} respectively.

$$\Delta C\cdot\frac{dV_{out+}}{dt} + C_{gs5}\cdot\frac{d(V_{out+}-V_{s5})}{dt} + I_8 + C_{db8}\cdot\frac{dV_{out+}}{dt} + C_{dg8}\cdot\frac{d(V_{out+}-V_{latch})}{dt}$$
$$= C_{sg10}\frac{d(V_{DD}-V_{out+})}{dt} + C_{db11}\frac{d(V_{DD}-V_{out+})}{dt} + C_{gd11}\frac{d(V_{out-}-V_{out+})}{dt} + C_{gd12}\frac{d(V_{latch}-V_{out+})}{dt} \quad (15)$$

$$C_{gs6}\cdot\frac{d(V_{out-}-V_{s6})}{dt} + I_7 + C_{db7}\cdot\frac{dV_{out-}}{dt} + C_{dg7}\cdot\frac{d(V_{out-}-V_{latch})}{dt}$$
$$= C_{sg11}\frac{d(V_{DD}-V_{out-})}{dt} + C_{db10}\frac{d(V_{DD}-V_{out-})}{dt} + C_{gd10}\frac{d(V_{out+}-V_{out-})}{dt} + C_{gd9}\frac{d(V_{latch}-V_{out-})}{dt} \quad (16)$$

$$C_{gs5} = C_{gs6}, C_{db8} = C_{db7}, C_{dg8} = C_{dg7}, C_{sg10} = C_{sg11}, C_{db11} = C_{db10}$$
$$C_{gd11} = C_{gd10}, C_{gd12} = C_{gd9}, I_8 = I_7, V_{out+} = V_{out-} \quad (17)$$

Subtract (16) from (15) using the condition (17)

$$\Delta C\cdot\frac{dV_{out+}}{dt} = C_{gs5}\cdot\frac{d(V_{s5}-V_{s6})}{dt} \quad (18)$$

Combine (14) and (17)

$$\Delta I \approx \frac{-(C_{db1} + C_{gd1} + C_{gd2} + C_{bs5} + C_{gs5})}{C_{gs5}}\cdot\Delta C\cdot\frac{dV_{out+}}{dt} \quad (19)$$

Therefore, the dynamic offset caused by capacitor mismatch ΔC at output node is

$$|V_{os\_C}| \approx \frac{C_{db1} + C_{gd1} + C_{gd2} + C_{bs5} + C_{gs5}}{C_{gs5}\cdot G_{m2}}\cdot\Delta C\cdot\frac{dV_{out+}}{dt} \quad (20)$$

From (20), it can be concluded that: first, the analytical model identifies the parasitic capacitors contributing the offset voltage; second, offset is linear proportional to the mismatch capacitor value Δ*C*; third, from the term dV_{out+}/dt, it is known that the faster V_{out+} changes since V_{latch} signal is rising up to V_{DD}, the larger offset will be induced.

Figure 4 illustrate the most time-efficient way to find dV_{out+}/dt. Under the condition that the circuit is at the balanced mode without any types of mismatch, V_{out+} or V_{out-} node time trajectory are identical and plotted in Fig.4. The estimated dV_{out+}/dt is the slope value measured at the moment when V_{latch} signal is just rising up to V_{DD}. The method only requires one time short transient analysis less than one clock cycle for the circuit at the balanced mode without any mismatch.

Similarly, offset caused by mismatch capacitor Δ*C* at other pairs of nodes A, B and D can be derived as follows

$$|V_{os\_A}| \approx \frac{\Delta C}{G_{m2}}\cdot\frac{dV_{s5}}{dt},\ |V_{os\_B}| \approx \frac{\Delta C}{G_{m2}}\cdot\frac{dV_{s7}}{dt},\ |V_{os\_D}| \approx 0 \quad (21)$$

IV. A NUMERICAL EXAMPLE AND SIMULATION RESUTLS

"Lewis-Gary" structure is implemented in Spectre to validate the effectiveness of the proposed analytical model.

10fF capacitor is used as the mismatch capacitor and added at nodes *A*, *B*, *C* and *D* respectively. The predicted offsets for each pair of nodes can be calculated using (21). Figure 5 gives a comparison between predicted values and results from time-consuming transient simulation using BSIM3v3 model. From Fig. 5, they are showing reasonable agreement. The deviation is mainly due to the approximations made, such as neglect of channel length modulation. The output nodes are the most sensitive nodes to capacitive mismatch. Based upon the analytical model (20), if the speed requirement can be easily meet, some precisely-matched capacitor can be added simultaneously at V_{out+} and V_{out-} node to reduce dV_{out+}/dt and therefore reduce offset. Meanwhile, it is still critical to do well-balanced layout including matching of metal routings, via locations and placement of neighbor components so that conditions like (17) can be met as close as possible. Nodes *D* are insensitive to capacitive mismatch. Figure 6 verifies the observed linear relationship between mismatch capacitor ΔC and offset predicted by (20).

TABLE I. KEY VALUES FOR THE DYNAMIC COMPARATOR IN 0.6µ

Process	0.6µm CMOS
Power supply	V_{DD}=3V, V_{SS}=0V
Transistor sizing	$(W/L)_{1,2,3,4}$=16u/1.2u
	$(W/L)_{5,6,7,8}$=16u/1.2u
	$(W/L)_{10,11}$=16u/1.2u
V_{ref}	V_{ref+}=1.6V, V_{ref-}=1.2V
Clock signal V_{latch}	High=3V;Low=0V
	Rise and fall time = 0.3ns
	Pulse width=20ns; Freq=10MHz
Switch (PMOS)	$(W/L)_{9,12}$=16u/1.2u

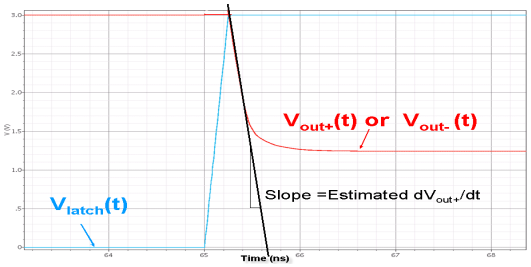

Figure 4. The method to find dV_{out+}/dt value

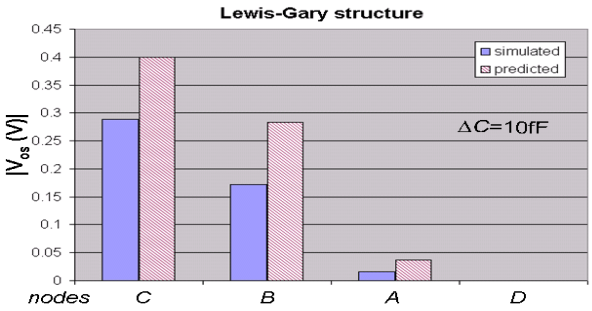

Figure 5. Comparison between simulated and predicted offset

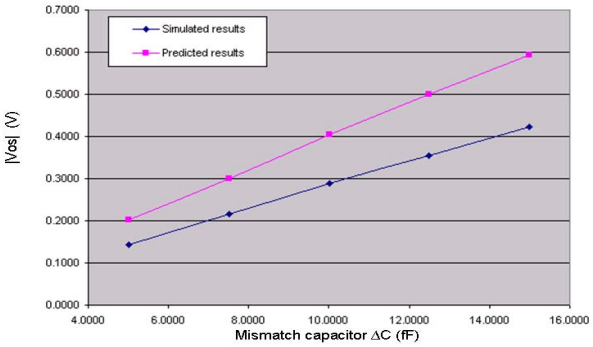

Figure 6. Vos vs. capacitor mismatch ΔC at output nodes

V. CONCLUSIONS

In this work, we apply "balanced mode" concept to analyze the capacitive mismatch at different nodes in a dynamic comparator. With the aid of balanced mode concept, the time-varying non-linear problem can be simplified and easy to be analyzed. The analytical models are derived to demonstrate offsets caused by capacitor mismatch in each pair of nodes. The models show good indications on the nodes that are sensitive to capacitive mismatch and on how to reduce the offset.

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