New Calibration Technique for Current-Steering DACs

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Abstract—Attaining high matching property of the current sources is very important for the design of high-speed high-accuracy current-steering DACs. This paper presents a novel calibration technique—complete-folding, which achieves the high matching accuracy by selectively regrouping current sources into a fully binary-weighted array based on the current comparisons after chip fabrication. The implementation only requires an analog current comparator and some digital circuitry. The minimum requirement of analog circuits makes the complete-folding calibration suitable for the DAC design in the low-voltage process. Statistical results with a behavioral model of a 14-bit segmented DAC in MATLAB show that complete-folding calibration can reduce the total gate area of current sources by a factor of almost 1200 compared to that using intrinsic-accuracy method. Additional results also show that the new calibration technique has the superior performance in compensating random mismatch errors compared with state-of-the-art.

I. Introduction

High-speed high-accuracy current steering DACs are extensively used in the modern communication systems. For these applications, high matching accuracy of the current sources is required. According to [1], for a 14-bit DAC, the relative standard deviation of a unit current source should not exceed 0.21% in order to achieve a yield of 99.7% with INL < 0.5LSB in the 0.18μm CMOS process. Attaining such a high matching requirement by employing intrinsic-accuracy method [2][3] is very difficult, since the gate area of the current sources becomes extremely or unacceptably large for the high-resolution DAC design. Additionally, large area deteriorates the parasitic and gradient effects, which are very hard to compensate, and significantly degrade the SFDR at the high input frequencies. Therefore, calibration techniques become more and more attractive to the high-resolution DAC design since it has the advantage of smaller area and better dynamic performance [4].

Yet the scaling of CMOS technologies keeps shrinking the feature size and power supply voltage, many conventional calibration techniques [5][6] suffer dramatically from the reduced power supply and become unfeasible for the DAC design in the low-voltage technologies. Consequently, low-voltage calibration techniques become highly demanded today. There are two leaders in this area, which are self-calibration [4] and switching-sequence post-adjustment (SSPA) calibration [1]. Both techniques are very effective to random mismatch error compensation in the low-voltage process but with different methodologies.

Self-calibration technique employs a very accurate ADC to digitize the current errors corresponding to each input code. These error codes will be stored in a RAM to control a calibration DAC. During the conversion time, the calibration DAC will output the corresponding current based on the error code from the RAM that is addressed by the digital inputs. At the end, this current will be summed up with the current in the main DAC to become the final output current. The block diagram of this technique is shown in Fig. 1. Compared to the DAC without any calibration, this method reduces the total gate area of the current source array by a factor of more than 500 [4].

SSPA calibration technique achieves the good static accuracy by adjusting the switching sequence of the current sources in the unary-coded array after fabrication. It uses an accurate current comparator to rank all the current sources. The best switching sequence is determined based on these ranks. Fig. 2 illustrates the block diagram for the SSPA calibration. According to [1], SSPA method lessens the requirement of the current sources' gate area by a factor of 10. However, most importantly, instead of using complicated calibration circuits (ADC-DSP-DAC), SSPA substantiates the potential of calibrating a DAC with good performance by using only minimum requirement of analog circuits and some digital circuitry. This approach is much preferred in the very-low-voltage-process.

In this paper, a novel low-voltage calibration technique—complete-folding, which enhances the DAC's matching property by dynamically combining the current sources into a fully binary-weighted array based on the current comparisons after chip fabrication, is presented. Statistical results show that complete-folding calibration can cut the overall gate area of current sources by a factor of almost 1200 for a 14-bit DAC. Furthermore, complete-folding technique requires a low overhead in calibration circuits, which only contain an analog current comparator and some digital circuitry.

This paper is organized as follows. In Section II, the principle of complete-folding calibration is presented, while the MATLAB behavioral model of complete-folding calibration is shown in section III. Finally, conclusion is drawn in section IV.

II. Complete-Folding Calibration Technique

Complete-folding calibration technique is very similar to the SSPA calibration; however, it actually converts a unary-coded array into a binary-weighted array by recombining current sources rather than changing the switching sequence of current sources in the unary-coded array. In order to understand the principle of complete-folding calibration, the single-folding operation is explained at first.

Fig. 3 (a) illustrates the three steps of the single-folding

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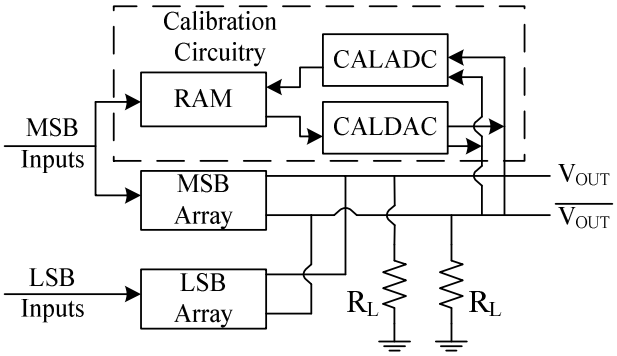

Fig.1 Block diagram of self-calibration technique

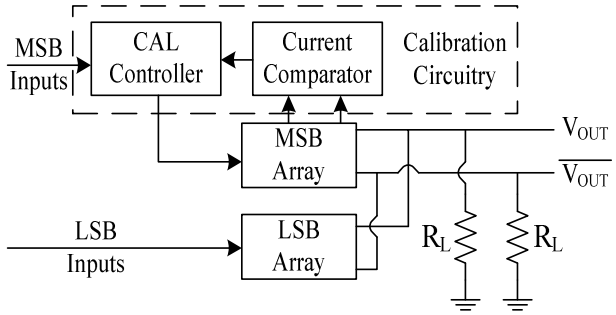

Fig.2 Block diagram of SSPA calibration technique

operation for a 3-bit unary-coded array that has 7 current sources in total. The rectangle in the figure is denoted as the current value of each current source with random variations. At the beginning, all the current sources will be sorted in the ascending order based on the outputs of the current comparator. Next, the smaller current is grouped with the bigger current, and the current in the middle is left behind. Finally, two currents in each group are summed together, and the last single current is moved to the end of the new sequence. By doing so, the first three currents are approximately two times larger than the last current, which implies that the original 3-bit unary-coded array is transformed into a 2-bit unary-coded with 1-bit binary-weighted.

Founded on this, with the single-folding an n-bit unary-coded array can be converted into an (n-1)-bit unary-coded with 1-bit binary-weighted. If we continue to employ the single-folding to the new unary-coded array produced by the previous operation, eventually the n-bit unary-coded array will become an n-bit binary-weighted array. This process is what we called—complete-folding. In other words, complete-folding is to implement (n-1)-time single-folding in an n-bit unary-coded array. In our original example of the 3-bit unary-coded array, only 2-time single-folding is required to ensure the complete-folding. Fig. 3(b) shows the second single-folding process. It is noted that only three current sources are left at the end but with the difference by a factor of 2 off each other.

Complete-folding calibration is feasible in the very-low-voltage-process, since it only requires an accurate current comparator in the analog domain. Meanwhile, the complexity of the digital circuitry is much relaxed compared to that for

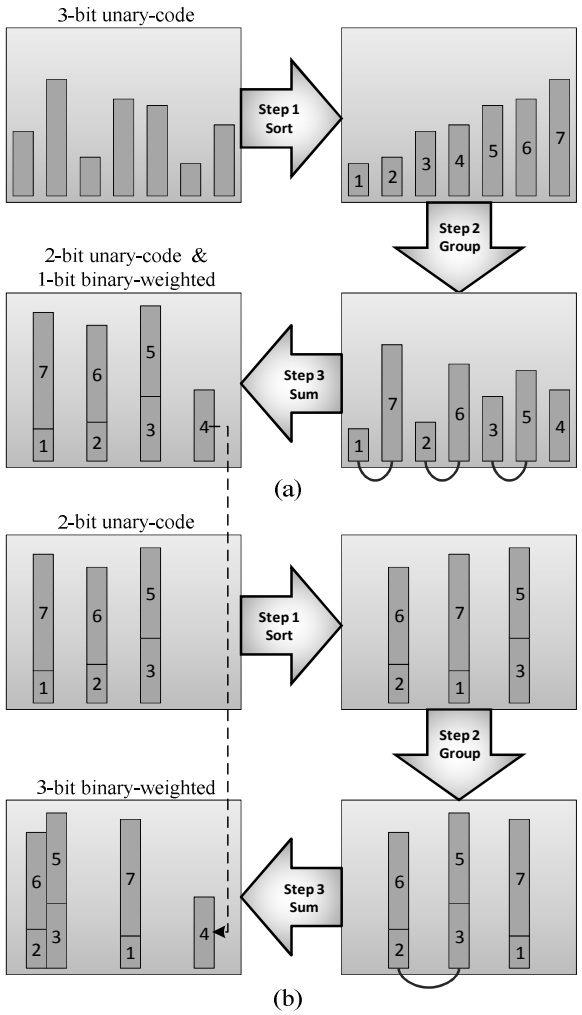

Fig.3 (a) 1st single-folding for 3-bit unary-code array (b) 2nd single-folding for 3-bit unary-code array

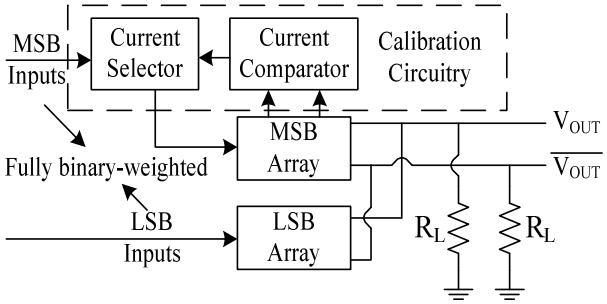

Fig.4 Block diagram of complete-folding calibration technique

SSPA calibration. This is because that complete-folding calibration uses binary-weighted as the decoding scheme rather than unary-coded. Fig. 4 shows the block diagram for the complete-folding calibration.

III. MATLAB Behavioral Model

In order to demonstrate the complete-folding calibration technique and compare the results with state-of-the-art, a

behavioral model of a 14-bit current-steering DAC with 7-7 segmentation has been built in MATLAB. Calibration techniques, which are (a) SSPA calibration, (b) self-calibration, and (c) complete-folding calibration, are considered. All three methods are separately implemented in the 7-bit unary-coded MSB array, while the 7-bit binary-weighted LSB array is realized by intrinsic-accuracy method. The following paragraphs explain the setup for our DAC behavioral model. Meanwhile, in the following discussions, LSB is always referred to the 14-bit level.

Our behavioral model only includes the random mismatch error which is determined by the inherent matching properties of a given technology. At here, we borrowed the yield estimation data of a 14-bit DAC from [1], where the relative standard deviation σ_u has to be less than 0.21% in order to achieve a yield of 99.7% with INL < 0.5LSB in the 0.18μm process. The corresponding area for the unit current source can be defined as A_u, and hence the total gate area of the intrinsic 14-bit DAC can be expressed as follows:

$$A_{intrinsic} = (2^{14} - 1)A_u = 16383A_u \quad (1)$$

We can use (1) as a reference to compare the area reduction by employing different calibration techniques.

Generally, after calibration, both residual errors of calibrated MSB array and intrinsic errors of LSB array will contribute to the overall errors of the DAC. In our behavioral model, we conservatively assume that the two error sources contribute to a half of the total error budget (0.25LSB) and they are uncorrelated.

Based on the yield model in [7], in order to achieve a yield of 99.7% with INL < 0.25LSB for the 7-bit LSB array, the relative standard deviation of the unit current source can be about $4\sqrt{2}$ times greater than that of uncalibrated 14-bit DAC, i.e. σ_{u_LSB} = 1.245%. The relaxed requirement gives reduction in the gate area of current sources by a factor of 32. Thus, the total gate area of the current sources in the LSB array after calibration can be expressed in the following way:

$$A_{LSB_{Cal}} = (2^7 - 1) * \left(\frac{A_u}{32}\right) = 3.97A_u \quad (2)$$

So as to determine the relative standard deviation of the unit current source in the MSB array (σ_{u_MSB}) for different calibration techniques, statistical simulations are performed in MATLAB. First, we will assume that the gate area of the unit current source in MSB array is 2^7 times larger than that in the intrinsic LSB array for all three calibration techniques, then σ_{u_MSB} is reduced by a factor of $\sqrt{2^7}$ compared to σ_{u_LSB}, i.e. σ_{u_MSB} = 0.105%. Then, we can run a set of statistical simulation to decide how to adjust σ_{u_MSB} value to achieve the desired yield requirement for each calibration technique.

Before going into the simulation results, it is worth to mention the different setup for each calibration technique. On one hand, in the self-calibration both errors from CALADC and CALDAC are limited to 0.25LSB. Therefore, CALADC is set to have 16-bit resolution and accuracy while CALDAC has 8-bit resolution [4]. On the other hand, 20 extra current

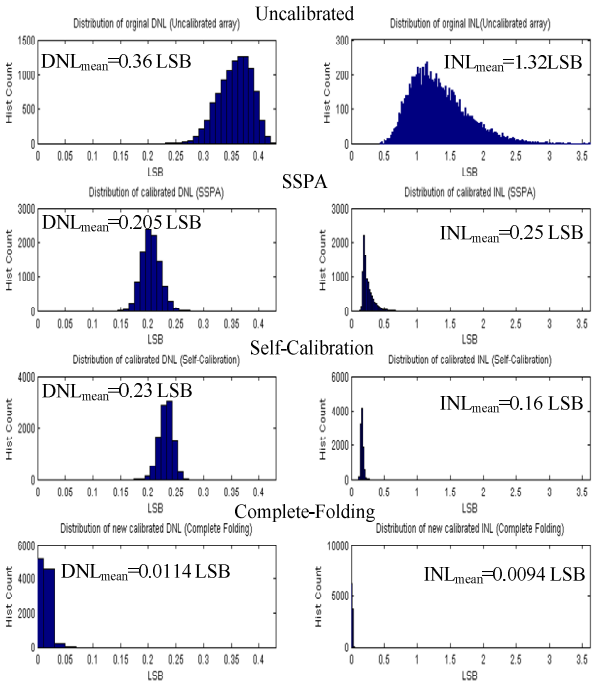

Fig.5 DNL/INL distributions for using different calibration methods

Table 1 σ_{u_MSB} of different methods for the desired yield

Method	σ_{u_MSB}
SSPA	0.0457%
Self-Calibration	0.594%
Complete-Folding	0.817%

sources are added for both SSPA calibration and complete-folding calibration (6-time single-folding in this case), since these extra current sources are effective to eliminate the possible large defects in the current sources and can improve the overall static performance [1]. However, only 127 current sources will be used during the conversion time.

Fig. 5 shows the DNL and INL statistical distributions of 10,000 randomly generated MSB array using different calibration techniques when σ_{u_MSB} = 0.105%. From the graph, σ_{u_MSB} can be increased for both self-calibration and complete-folding calibration, while σ_{u_MSB} for SSPA calibration needs to be reduced slightly to achieve the desired yield. It is also noted that complete-folding calibration has better overall performance in compensating random errors than the other two techniques. After these observations, we can run various statistical simulations to obtain the corresponding σ_{u_MSB} for each calibration technique where it will achieve the yield of 99.7% with INL < 0.25LSB. Table 1 summarizes the σ_{u_MSB} value for each calibration technique.

From these σ_{u_MSB} values, the total gate area of current sources in the MSB array for different calibration techniques can be calculated as follows:

$$A_{MSB_{SSPA}} = (2^7 - 1 + 20) * 2^7 * \left(\frac{A_u}{32}\right) * \left(\frac{0.105\%}{0.0457\%}\right)^2$$

$$= 3103.48A_u \quad (3)$$

Table 2 Area comparison of different methods for the 14-bit DAC

Method	Total Area	Area Reduction
Intrinsic-Acuuray	16383A_u	1
SSPA	3107.45A_u	5.27
Self-Calibration	19.85A_u	825.34
Complete-Folding	13.68A_u	1197.6

Table 3 Improvement of static accuracy after each single-folding

Method	DNL improvement factor	INL improvement factor
Uncalirated	1	1
1st single-folding	10.75	16.69
2nd single-folding	20.85	52.17
3rd single-folding	25.87	90.38
4th single-folding	28.73	119.82
5th single-folding	30.31	134.47
6th single-folding	30.96	139.06

$$A_{MSB_{SelfCal}} = (2^7 - 1) * 2^7 * \left(\frac{A_u}{32}\right) * \left(\frac{0.105\%}{0.594\%}\right)^2 = 15.88A_u \quad (4)$$

$$A_{MSB_{CompFold}} = (2^7 - 1 + 20) * 2^7 * \left(\frac{A_u}{32}\right) * \left(\frac{0.105\%}{0.817\%}\right)^2 = 9.71A_u \quad (5)$$

Combining (2) (3) (4) and (5) provides us the total gate area of current sources for the 14-bit DAC with different calibration techniques. Table 2 shows the calculation results. From the table, the complete-folding achieves the most area reduction factor, which is 1198!

To find more insight in complete-folding calibration, we break up the process by 6 steps in this case. Fig. 6 shows the DNL and INL distributions of 10,000 randomly generated 7-bit MSB array after each single-folding. Table 3 concludes the improvement factor after each single-folding compared to the original static accuracy. It is shown that each single-folding will improve the overall DNL and INL, and the most improvement comes from the first three single-folding operations. Even though 3-time single-folding may appear to have comparable performance to complete-folding, complete-folding is still much superior to 3-time single-folding, not only because it attains the slightly better accuracy performance, but it also has less complexity in the digital circuitry due to the fully binary-weighted operation.

Furthermore, applying complete-folding to more bits of DAC will result in more reduction of the analog area and better overall linearity. Nonetheless, complete-folding still requires some digital circuits to group the corresponding current sources and they may get complicated with the increase of number of bits. Therefore, there still exists a tradeoff between area and linearity.

IV. Conclusion

In this paper, a novel calibration technique—complete-folding, which enhances the static accuracy by selectively rearranging the current sources into a fully binary-weighted array based on the current comparisons after chip fabrication, is presented. Complete-folding is compared with the other two competing calibration techniques using our MATLAB behavioral model. For the same yield requirement, complete-folding is substantiated to have the most area reduction factor. A prototype 14-bit DAC is under the development and will be fabricated. The test results will be reported shortly.

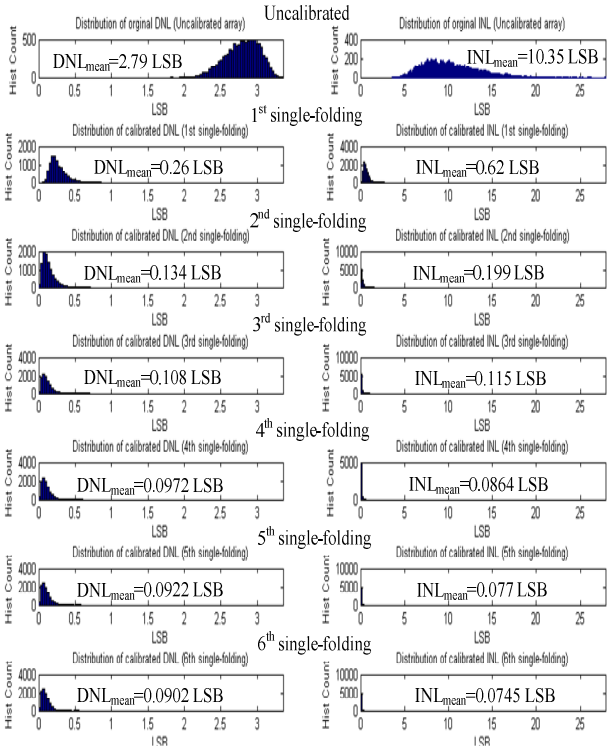

Fig.6 DNL/INL distributions after each single-folding for 7-bit MSB

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