Output Impedance Linearization Technique for Current-Steering DACs

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Abstract—Code and voltage dependence of the finite output impedance is a major contributor to current-steering DACs' nonlinearity. This paper introduces a novel output impedance linearization technique that very effectively reduces this code and voltage dependence. The linearization is achieved by using a small linearization DAC switched with control signals opposite to those for the main DAC. The area and power overhead is less than 5% of the main DAC. Simulation results with a 14-bit segmented current-steering DAC in standard 0.18µm CMOS process show that the DAC's integral nonlinearity due to finite output impedance is improved by almost 5 bits. Additional results also show that the linearization technique is very robust to random mismatch errors.

I. Introduction

Digital-to-analog converters (DACs) are the crucial building blocks for many signal processing and telecommunication systems. In the regard of high-speed high-accuracy applications, current-steering DACs are almost exclusively used. With different selection methods—binary-weighted, unary-coded, and segmented, current steering DACs are implemented by an array of matched current sources. Their performance is generally limited by non-idealities such as random mismatch, finite output impedance, gradient effect, finite settling time, glitch energy, timing skew etc. Among all of these, finite output impedance is one of the bigger concerns that could degrade DACs' both static and dynamic linearity [1]{2]. Moreover, gaining adequate output impedance becomes one of the major challenges for integrating high-performance DACs into the low-voltage CMOS technologies. In this paper, a novel output impedance linearization technique is presented. This technique uses the control signals that are opposite to those for the main DAC to run a very small linearization DAC, whose area and power overhead is less than 5% of the main DAC. By doing so, the code and voltage dependence of finite output impedance can be effectively reduced. Simulation results show that the INL due to the finite output impedance can be improved by nearly 5 bits.

This paper is organized as follows. In Section II, a brief overview of the finite output impedance is discussed. Then, the principle of output impedance linearization technique is presented in section III, while the simulation results are shown in section IV. Conclusion is drawn in section V.

II. Overview

For a high-resolution current-steering DAC design, finite output impedance of the current source is one of the limiting factors to the high performance. When the DACs' output experiences a various change between zero and full scale, the number of current sources also differs based on the corresponding digital code, thus different impedance are shown up at the output node. As Fig. 1 illustrates, k current sources are driven to the load resistor R_L, and then,

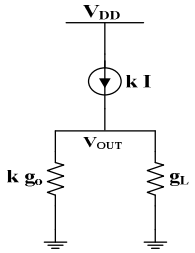

Fig. 1 Equivalent circuit model for current-steering DAC

$$V_{out} = kI/\,(kg_o + g_L) \tag{1}$$

where g_o is the output conductance for a single current source. From this, INL expression for single-ended output can be obtained by using end-point fit line method. Set α to equal to g_o/g_L, and assume that the output conductance g_o is so small that $\alpha k \ll 1$, then,

$$INL_s(k) = \alpha k(N-k)\ LSB \tag{2}$$

where N is the total number of current sources. In this case, the maximum INL is approximately equal to $\alpha N^2/4\ LSB$ occurring at the middle-scale. Therefore, to attain INL < 0.5LSB for a 14-bit DAC, the output impedance has to be greater than 3.36 GΩ assuming R_L is 50Ω!

Nevertheless, the requirement could be lessened by using fully differential output. A similar analysis could be applied, and the new INL can be expressed as follows:

$$INL_d(k) = \alpha^2 k\left(\frac{N}{2}-k\right)(N-k)\ LSB \tag{3}$$

The maximum INL is roughly equal to $\sqrt{3}\alpha^2 N^3/36\ LSB$ when k is equal to $\left(3 \pm \sqrt{3}\right)N/6$. Thus, for the same accuracy requirement as mentioned previously, the minimum output impedance can be reduced to be 32.5 MΩ, which is 100 times lesser than that using single-ended output.

Even though using fully differential output configuration can relax the requirement for the output impedance, it still has great challenges to meet the high accuracy requirement by only single transistor. Thus, adding a cascode stage is necessary to enhance the output impedance of current sources [2]. Yet the scaling of CMOS technologies keeps reducing in

size of the feature dimension and power supply voltage, for a certain supply voltage adding cascode stages could raise the following concerns: (a) reduction of voltage headroom, (b) degradation in matching accuracy and immunity against noise and voltage fluctuation [3], (c) limitation of achievable output impedance by device leakage. Consequently, it becomes unfeasible to attain high output impedance using multiple cascode stages in the low-voltage technologies.

Besides, the scaling of CMOS technologies yields additional problems that degrade the overall output impedance—soft switching effect and voltage dependence of output impedance. These two factors are usually ignored in the analysis (2) and (3); however, they play significant roles in altering the output impedance in the low-voltage process. Therefore, the required output impedance obtained by (3) might be not sufficient to achieve the desired accuracy level.

Soft switching is commonly used in today's DAC designs [4]-[7]. It uses a reduced voltage swing for the switch signals in order to avoid the charge injection due to the parasitic coupling between the gate of the switch and output node. Generally, the off-switch operates in the subthreshold region, where it no longer holds relatively high impedance in the low-voltage technologies, and in some cases, it becomes comparable with the on-side impedance, and hence degrades the overall output impedance at the output node.

Voltage dependence of output impedance is a well-known phenomenon. As DACs' output varies from zero to full scale, the equivalent output impedance for each current source also fluctuates due to the different drain-to-source voltage of switch transistors. This effect deteriorates as the supply voltage shrinks down, since the DAC's full scale voltage could easily range from 1/3 to 2/3 of the power supply. Thus, the nonlinearity due to the finite output impedance is worsening.

Based on the discussion above, attaining high output impedance becomes unfeasible and/or ineffective to meet the high accuracy requirement for the DAC designs in the low-voltage process. The next section presents a novel output impedance linearization technique, which can improve the accuracy by compensating the code and voltage dependence of output impedance with the use of a linearization DAC.

III. Output Impedance Linearization Technique

The principle of the output impedance linearization technique is conceptually illustrated in Fig. 2. The n-bit main DAC and linearization DAC are both controlled by the switch signals but in the opposite manners. The transistor-level routing is shown in Fig. 3. In this configuration, when k current sources are switched on in the left side of the main DAC, N-k current sources are turned on in the left side of the linearization DAC, and vice versa, where $N = 2^n - 1$. By doing so, the linearization DAC is able to compensate errors due to the finite output impedance in the main DAC; however, a constraint must be placed to the linearization DAC, which is that its area and power consumption should not exceed 5% of those for the main DAC. Otherwise, it becomes cost ineffective and could lead to other problems.

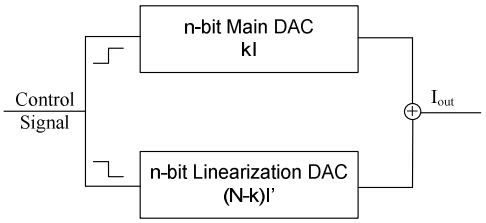

Fig. 2 Block diagram for output impedance linearization

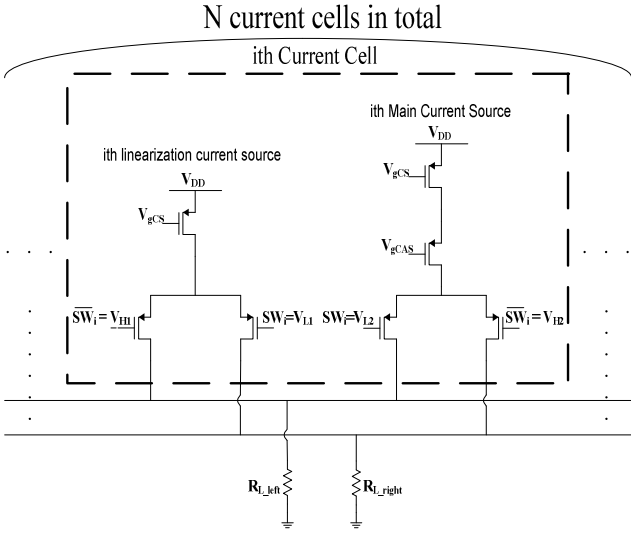

Fig. 3 Transistor-level routing for the linearization and main DAC

In order to understand how the linearization DAC can compensate the nonlinearity due to finite output impedance, mathematical analysis has been performed for the INL after using the linearization technique. Fig. 4 shows the circuit model that our analysis is based on. For simplicity, we ignored the output impedance at the off-side. This will not contribute much difference at the end.

In Fig. 4, I is denoted as the nominal current of the main DAC, while I' is the nominal current of the linearization DAC, and $I' < 0.05I$. In addition, g_o and g_o' are the output conductance of the current source in the main DAC and linearization DAC respectively, and g_L is the load conductance. Then, the output voltages are:

$$V_{out} = \frac{kI + (N-k)I'}{kg_o + (N-k)g_o' + g_L} \tag{4}$$

$$\overline{V_{out}} = \frac{(N-k)I + kI'}{(N-k)g_o + kg_o' + g_L} \tag{5}$$

For the single-ended output, INL can be obtained by end-point fit line method, where

$$INL_S(k) = V_{out} - V_{fit\_single}$$

$$= \frac{k(N-k)(g_o - g_o')}{kg_o + (N-k)g_o' + g_L}\left(\frac{I}{Ng_o + g_L} - \frac{I'}{Ng_o' + g_L}\right) \tag{6}$$

Using the similar analysis, we can also get the INL expression for the fully differential output:

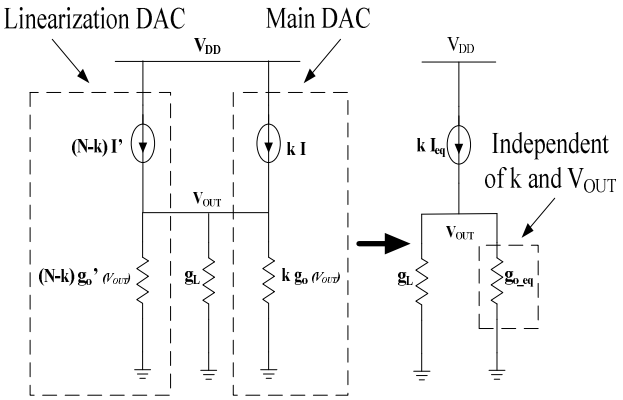

Fig. 4 Equivalent circuit model for output impedance linearization

$$INL_d(k) = V_{diff} - V_{fit\_diff}$$

$$= \frac{k(N-k)(N-2k)(g_o - g_o')^2}{(kg_o + (N-k)g_o' + g_L)\big((N-k)g_o + kg_o' + g_L\big)}\left(\frac{I}{(Ng_o + g_L)} - \frac{I'}{(Ng_o' + g_L)}\right) \quad (7)$$

Based on (6) and (7), when g_o=g_o', the nonlinearity due to finite output impedance can be cancelled. This is because that the total output impedance will always fix to be Ng_o rather than varying with the digital code. Thus, properly sizing the linearization DAC can lead to the code dependence compensation. Nonetheless, not only the code dependence is important, but voltage dependence also plays a significant role in altering the output impedance. The linearization DAC is able to reduce the voltage dependence as well. To see how this could happen, the voltage dependence of output impedance is included in the following INL analysis. For simplicity, only first-order voltage dependence is considered.

$$g_o = g_o(k) = g_o + k\Delta_{g_o} \quad (8)$$

$$g_o' = g_o'(k) = g_o + k\Delta_{g_o'} \quad (9)$$

Replacing g_o and g_o' in (4) and (5) with (8) and (9) produces the following new expressions for the output voltages:

$$V_{out} = \frac{kI + (N-k)I'}{kg_o + (N-k)g_o' + k^2\Delta_{g_o} + (N-k)k\Delta_{g_o'} + g_L} \quad (10)$$

$$\overline{V_{out}} = \frac{(N-k)I + kI'}{(N-k)g_o + kg_o' + (N-k)^2\Delta_{g_o} + (N-k)k\Delta_{g_o'} + g_L} \quad (11)$$

By the same means, new INL expressions can be derived for both single-ended output (12) and fully differential output (13), and they are illustrated at the bottom of the page. In the single-ended output case, the linearization DAC needs to have as the same nominal output impedance as the main DAC and it must also track the exact changes in output impedance to ensure the code and voltage dependence cancellation. It is very tricky to meet such two strict requirements; however, achieving one or falling somewhere in-between is quite simple to do. This will lead some improvements to the DAC's linearity, but they are very limited because of the indefeasible terms due to the incapability of matching the two DACs' nonlinearities. In the fully differential output case, it only requires matching the variations in output impedance for very good nonlinearity compensation. If Δ_{g_o} and $\Delta_{g_o'}$ are matched, most terms in the INL expression is removed. Therefore, linearization DAC with fully differential output can very effectively reduce the code and voltage dependence of the finite output impedance.

In short, the linearization DAC needs to follow the nonlinearity of the main DAC caused by finite output impedance, and obtaining about the same nonlinearity with small current becomes the design goal for the linearization DAC. Since the current is fixed, there are only two degrees of freedom left—size of linearization switches and voltage swing of linearization switch signals. By controlling these two factors, we can increase the drain-to-source saturation voltage of the switch transistors to gain the desired nonlinearity for the linearization DAC.

IV. Simulation Results

In order to demonstrate this new technique, a 14-bit segmented current-steering DAC, which has a full-scale output of 1V and the load resistance of 50Ω, is simulated in the standard 0.18μm CMOS process (1.8V power supply). Since the static performance of a segmented DAC strongly relies on the linearity of the MSBs, we employ this technique only to the 6-bit unary-coded MSB array that has a nominal current of 312.5μA.

Fig. 5(a) shows the original INL due to the finite output impedance of the 6-bit MSB array for the single-ended and fully differential outputs. From the plot, the INLs in both cases do not meet the 14-bit accuracy. Meanwhile, it is also noted that the fully differential output structure does not help much with the linearity as (3) suggests. This is expected since soft switching effect and voltage dependence of output impedance worsen in the low-voltage technologies.

$$INL_{s_{new}}(k) = \frac{k(N-k)}{kg_o + (N-k)g_o' + k^2\Delta_{g_o} + (N-k)k\Delta_{g_o'} + g_L}\left(\left(g_o - g_o' + k\left(\Delta_{g_o} - \Delta_{g_o'}\right)\right)\left(\frac{I}{Ng_o + N^2\Delta_{g_o} + g_L} - \frac{I'}{Ng_o' + g_L}\right) + N\left(\frac{I\Delta_{g_o}}{Ng_o + N^2\Delta_{g_o} + g_L} - \frac{I'\Delta_{g_o'}}{Ng_o' + g_L}\right)\right) \quad (12)$$

$$INL_{d_{new}}(k) = \frac{k(N-k)(N-2k)}{\big(kg_o + (N-k)g_o' + k^2\Delta_{g_o} + (N-k)k\Delta_{g_o'} + g_L\big)\big((N-k)g_o + kg_o' + (N-k)^2\Delta_{g_o} + (N-k)k\Delta_{g_o'} + g_L\big)}\left(\left(\left(g_o - g_o' + N\Delta_{g_o}\right)^2 + (N-k)k\left(\Delta_{g_o} - \Delta_{g_o'}\right)^2\right)\left(\frac{I}{Ng_o + N^2\Delta_{g_o} + g_L} - \frac{I'}{Ng_o' + g_L}\right) + \left(\Delta_{g_o} - \Delta_{g_o'}\right)\left(\frac{I(Ng_o' + g_L)}{Ng_o + N^2\Delta_{g_o} + g_L} - \frac{I'\left(Ng_o + N^2\Delta_{g_o} + g_L\right)}{Ng_o' + g_L}\right)\right) \quad (13)$$

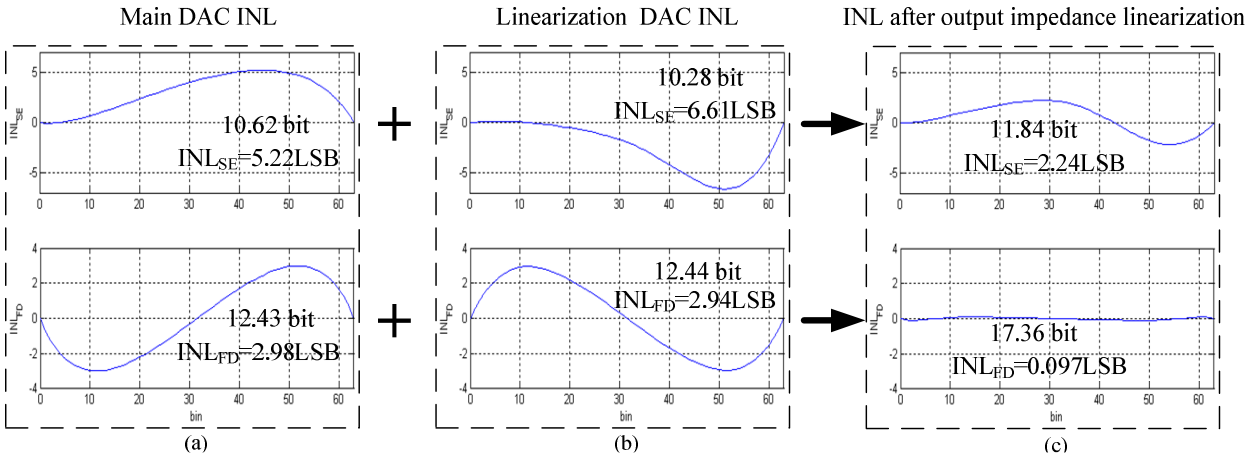

Fig. 5 (a) Main DAC INL for single-ended and fully-differential outputs (b) Linearization DAC INL for single-ended and full-differential outputs (c) Main DAC INL for single-ended and fully-differential outputs after output impedance linearization

So as to improve the accuracy, a linearization DAC has been designed and added to the main DAC. Fig. 5(b) illustrates the systematic INLs for the designed linearization DAC, while Fig. 5(c) shows the final INL results of the main DAC after adding the linearization DAC. The improvements can be easily observed. The INL for the single-ended output is 1 bit better than before. In contrast, the INL for the fully differential output is improved by almost 5 bits. In both cases, the current and gate area of current sources for the linearization DAC are about 3.5% of those for the 6-bit MSB DAC. With such little price to pay, code and voltage dependence of finite output impedance are significantly reduced. Furthermore, Fig. 6 shows that with some variations in the linearization switch sizes the improved accuracy level varies gradually. This substantiates that our technique is very robust to the random mismatch errors, and the performance will not change much after fabrication.

To sum up, output impedance linearization is a systematic-error cancellation technique. After the chip fabrication, random mismatch and gradient effect still exist in the main DAC, and can be compensated by calibration techniques [6][7] and special layout patterns [4][5] respectively.

V. Conclusion

In this paper, a novel output impedance linearization technique has been presented. It uses a linearization DAC with the control signals opposite to those for the main DAC to compensate the code and voltage dependence of finite output impedance. With small area and power consumption, this technique has been proved to be an effective solution to the systematic errors. Perhaps, it will ease the job in integrating high performance DACs into the low-voltage technologies. Furthermore, this technique could lead to some possible improvements for the DAC's dynamic performance, since it can reduce the effect of nonlinear RC time constant by making the output impedance linear. However, this is still under the investigation.

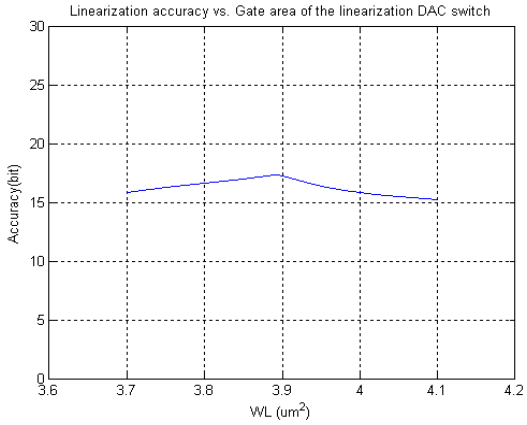

Fig. 6 Linearization accuracy vs. variation in linearization switch sizes

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