A linear differential output of threshold-based CMOS temperature sensor with enhanced signal range

Chen Zhao, Jun He, Sheng-Huang Lee, Karl Peterson
Dept. of Electrical and Computer Engineering
Iowa State University
Ames, IA, 50010
zhaochen@iastate.edu, sirenehe@iastate.edu,
alexlsh@iastate.edu, petersok@iastate.edu

Randall Geiger, Degang Chen
Dept. of Electrical and Computer Engineering
Iowa State University
Ames, IA, 50010
rlgeiger@iastate.edu, djchen@iastate.edu

***Abstract*—This work focuses on a new compact 6-transistor CMOS temperature sensor with improved flexibility for achieving target temperature linearity with small die area and low power consumption. The temperature information is provided in a differential output voltage that is based upon the linear dependence of threshold voltage on temperature. Implemented in a 0.18µm process, simulation results indicate the temperature linearity is at the 0.03°C level over the temperature range of -20 °C ~100 °C without any trimming. Over the standard process corners, the untrimmed structure has temperature nonlinearity at the 0.11°C level and Monte Carlo simulation shows the mean nonlinearity with both process and mismatch is also around 0.11°C. Current consumption of this design is around 40µA and active area is approximately 40 µm².**

I. INTRODUCTION

In modern VLSI circuit design, the trend continues for more complexity, increased speed, and higher levels of integration. Invariably, in high-performance computational systems, these trends increase power consumption to levels that tradeoffs must be made between performance and system lifetime. Thermal monitoring of die temperature or die temperatures is widely used as a critical input to power management in processor systems. Because of the highly nonlinear relationship between temperature and mean time to failure (MTTF), substantial benefits in system performance can be achieved if accurate die temperature measurements are made. Placing accurate temperature sensors at multiple sites on a die provides even more potential for improving processor performance. High accuracy, process compatibility and low-power consumption are key requirements for multi-site on-chip temperature sensors. Traditionally, the temperature-dependent characteristics of the pn junction have been used to sense temperature [2]-[6]. However, the area and power consumed by pn-junction are not attractive and in deep sub-micron processes, the availability of good, well-characterized pn-junctions is uncertain. A new structure based on the temperature dependence of the threshold voltage of a MOS transistor was proposed in [1]. This five-transistor Widlar-type circuit shows some advantages over existing approaches such as high temperature linearity, voltage supply independence, low power consumption, and a small active area.

In this paper, a new accurate six-transistor temperature sensor suitable for thermal monitoring on processers is introduced. In this sensor, temperature information is encoded in a differential output voltage that varies linearly with temperature. In this design, the voltage scale can be designed to provide a practical voltage range suitable for interfacing with the input to an analog to digital converter (ADC) thus providing a digital output that varies linearly with temperature. The new design provides good robustness in temperature linearity to both global process parameter variations and local mismatch effects.

In Section II, the two outputs of the new temperature sensor are analytically characterized. The two outputs have different temperature coefficients and different offsets. The differential output performance is discussed in Section III. In section IV, an implementation of the circuit in a 0.18µ CMOS process is presented. Simulations results are given that show both the thermal linearity and voltage range potential of this structure. Finally, Section V concludes this work.

II. CIRCUIT DESCRIPTION

The new six-transistor temperature sensor is shown, exclusive of the start-up circuit, is shown in Fig. 1. A simple square-law model of the devices is useful for analytically predicting the basic performance. Simulation results will be shown later to validate the analytical derivations.

If channel length modulation and output conductance effects are neglected, it follows from the basic square-law model that the drain currents for the devices in this circuit can be expressed as:

$$I_1 = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_1 (V_{o3} - V_{o2} - V_{th1})^2 \qquad (1)$$

$$I_2 = \frac{\mu_n C_{ox}}{2} \cdot (\frac{W}{L})_2 (V_{o3} - V_{o1} - V_{th2})^2 \quad (2)$$

$$I_2 = \frac{\mu_n C_{ox}}{2} (\frac{W}{L})_3 (V_{o1} - V_{th3})^2 \quad (3)$$

$$I_1 = \frac{\mu_n C_{ox}}{2} (\frac{W}{L})_4 (V_{o2} - V_{th4})^2 \quad (4)$$

$$I_2 = M \cdot I_1 \quad (5)$$

In these equations, M is the gain of current mirror (M5, M6). Solving this set of 5 equations is straightforward and it can be readily shown that the outputs V_{o1} and V_{o2} can be expressed as,

$$V_{o1} = \frac{(V_{th1} - V_{th2})}{1 + \sqrt{\frac{(W/L)_3}{(W/L)_2}} - \sqrt{\frac{\mu_n (W/L)_3}{M \cdot \mu_p \cdot (W/L)_4}} - \sqrt{\frac{(W/L)_3}{M \cdot (W/L)_1}}} + \frac{(\sqrt{\frac{(W/L)_3}{(W/L)_2}} - \sqrt{\frac{\mu_n (W/L)_3}{M \cdot \mu_p \cdot (W/L)_4}} - \sqrt{\frac{(W/L)_3}{M \cdot (W/L)_1}}) \cdot V_{th3} + V_{th4}}{1 + \sqrt{\frac{(W/L)_3}{(W/L)_2}} - \sqrt{\frac{\mu_n (W/L)_3}{M \cdot \mu_p \cdot (W/L)_4}} - \sqrt{\frac{(W/L)_3}{M \cdot (W/L)_1}}} \quad (6)$$

$$V_{o2} = \frac{\sqrt{\frac{\mu_n (W/L)_3}{M \cdot \mu_p \cdot (W/L)_4}} \cdot (V_{th1} - V_{th2})}{1 + \sqrt{\frac{(W/L)_3}{(W/L)_2}} - \sqrt{\frac{\mu_n (W/L)_3}{M \cdot \mu_p \cdot (W/L)_4}} - \sqrt{\frac{(W/L)_3}{M \cdot (W/L)_1}}} - \frac{\sqrt{\frac{\mu_n (W/L)_3}{M \cdot \mu_p \cdot (W/L)_4}} \cdot V_{th3} - (1 + \sqrt{\frac{(W/L)_3}{(W/L)_2}} - \sqrt{\frac{(W/L)_3}{M \cdot (W/L)_1}}) \cdot V_{th4}}{1 + \sqrt{\frac{(W/L)_3}{(W/L)_2}} - \sqrt{\frac{\mu_n (W/L)_3}{M \cdot \mu_p \cdot (W/L)_4}} - \sqrt{\frac{(W/L)_3}{M \cdot (W/L)_1}}} \quad (7)$$

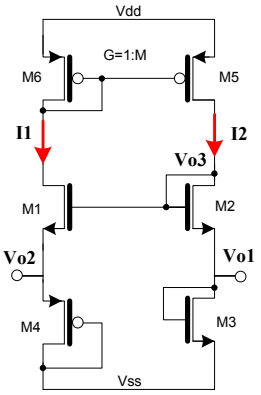

Figure 1. Schematic of proposed temperature sensor

where function 6 and function 7 are both linear functions in the threshold voltages and where the coefficients of these linear equations are independent of V_{DD}. Further, when the mobility appears in the coefficients in these equations, it appears only as a mobility ratio which is independent of temperature of the n-channel mobility and the p-channel mobility has the same temperature dependence. Here, the threshold voltages V_{th1}~V_{th3} are NMOS threshold voltages and V_{th4} is the PMOS threshold voltage. With the assumption that the n-channel mobility and the p-channel mobility have the same temperature dependence, it thus follows that V_{o1} and V_{o2} can be expressed simply as,

$$V_{o1} = a_1 V_{tn} + b_1 V_{tp} + c_1 \quad (8)$$

$$V_{o2} = a_2 V_{tn} + b_2 V_{tp} + c_2 \quad (9)$$

where the parameters $a_1, a_2, b_1, b_2, c_1, c_2$ are all temperature and V_{DD} independent constants dependent only upon device ratios and the mobility ratio. V_{thn} has positive temperature coefficient and V_{thp} has negative, as depicted in Fig. 2 and as expressed in (10) and (11). In these equations, $\alpha, \beta, V_{thn0}, V_{thp0}$ are all positive constants.

$$V_{thn} = \alpha T + V_{tn0} \quad (10)$$

$$V_{thp} = -\beta T - V_{tp0} \quad (11)$$

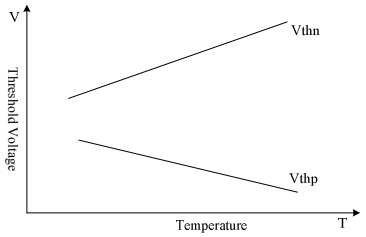

Figure 2. Threshold voltage of PMOS and NMOS temperature characteristics

Substituting equations (10) and (11) into (8) and (9), V_{o1} and V_{o2} can be expressed as

$$V_{o1} = (a_1\alpha - b_1\beta)T + (a_1 V_{thn0} - b_1 V_{thp0} + c_1) \quad (12)$$

$$V_{o2} = (a_2\alpha - b_2\beta)T + (a_2 V_{thn0} - b_2 V_{thp0} + c_2) \quad (13)$$

where the temperature dependence is explicitly shown. $\alpha, \beta, V_{thn0}, V_{thp0}$ are process parameters and $a_1, a_2, b_1, b_2, c_1, c_2$ can be designed through sizing of the W/L ratios of the transistors. If appropriate sized, this circuit can provide two linear temperature dependent outputs. The signs of temperature coefficients can be either positive or negative depending on requirements. In next section, we will show an implementation where V_{o1} has a positive temperature coefficient and V_{o2} has a negative temperature coefficient.

The proposed 6 transistor circuit has more degrees of freedom than the 5 transistor temperature sensor circuit [1], and has the positive temperature coefficient from the p-channel device M5. This extra degree of freedom is useful for minimizing the effects of second-order thermal nonlinearities introduced by the output conductance effects while providing for an enhanced output voltage variation over the desired temperature operating range. Since the additional transistor M4 is in series with M1, the additional transistor does not increase the power dissipation of the circuit.

III. DIFFERENTIAL OUPUTS OF PROPOSED STRUCTURE

In this section, emphasis is placed upon the differential output of the sensor. Although most reported temperature sensors have a single-ended output, from a practical viewpoint, differential output signals are equally suitable as inputs to many ADC architectures. The differential outputs of the temperature sensor will help reduce the effects caused by a rather large common-mode temperature-independent output voltage that is typical in single-ended output sensors. If the desired temperature range is over the interval [T_1, T_2], it follows from (14) and (15) that the two outputs can be expressed as

$$V_{o1} = \varphi_1 (T - T_1) + \varphi_2 \quad (14)$$

$$V_{o2} = \varphi_3 (T - T_1) + \varphi_4 \quad (15)$$

where φ_2, φ_4 are the values of V_{o1} and V_{o2} at temperature T_1 as shown in Fig. 3. The differential output $V_d = V_{o1} - V_{o2}$ is also linear with temperature, and is given by

$$V_d = (\varphi_1 - \varphi_3) T + \left[(\varphi_2 - \varphi_4) - T_1 (\varphi_1 - \varphi_3) \right] \quad (16)$$

The performance requirements of the ADC can be relaxed if the temperature-dependent range of V_d is large and covers an appreciable portion of the ADC input range. Assuming the extreme case where the ADC input range is $[V_{ss}, V_{dd}]$, two requirements should be met: a) $(\varphi_2 - \varphi_4)$ is larger than but closed to V_{ss}; b) $(\varphi_1 - \varphi_3)$ is smaller but closed to $\frac{Vdd - Vss}{T_2 - T_1}$. The necessity keeping all devices in saturation over process and temperature variations actually restricts the range on V_{01} and V_{02} to a much smaller value.

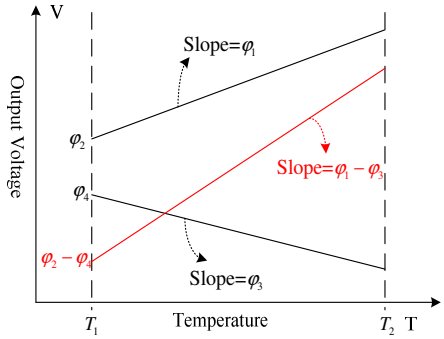

Figure 3. Differential outpus scales versus temperature

IV. IMPLEMENTATION OF THE DIFFERENTIAL TEMPERATURE SENSOR

The following design was obtained in a standard 0.18µ CMOS process. Details of the design process are somewhat tedious and not presented in this paper.

Table 1 Design Variables in 0.18µ CMOS

		M1	M2	M3	M4	M5,M6
Typical State	**W/L**	**2µ/1µ**	**1.2µ/4µ**	**0.8µ/5µ**	**16µ/1µ**	**5.05µ/1µ**
Processes Variation	**W/L**	**0.4µ/1µ**	**3.6µ/1µ**	**0.315µ/3µ**	**4.5µ/1.015µ**	**5.085µ/1µ**

The design to modify output stage is shown in Fig. 4. Simulation results for the output voltages V_{01}, V_{02}, and V_d for a total supply voltage of 1.8V are shown in Fig. 4 using Typical/Typical model parameters. The voltage scale range on the differential output is 140mV compared to the much smaller ranges of 85mV and 45mV on V_{01} and V_{02}.

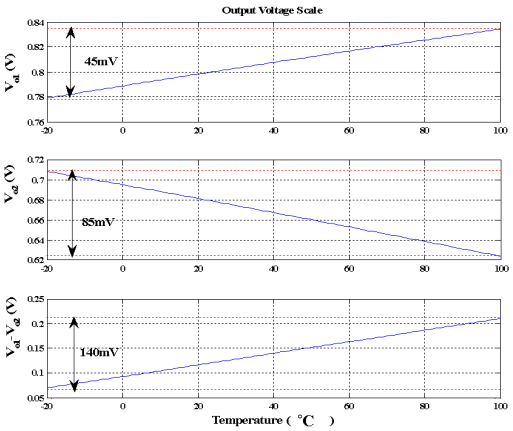

Figure 4. Simulation results of differential output voltage scales .

The design at the typical state is to get best temperature linearity. Its simulation result of this design is shown in the Fig. 5. These simulation results show a nonlinearity of 0.03 °C over a 120 °C range from -20 °C to 100 °C.

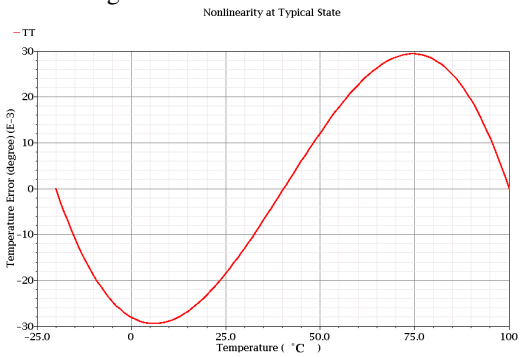

Figure 5. Temperature Error at typical condition

Robustness to process variations is of concern in any temperature sensor, particularly if expensive multi-temperature trims that correct for temperature nonlinearities are to be avoided. This structure was simulated at the four process corners, SS, FS, SF, and FF. These results are shown in Fig. 6. These results show a worst-case nonlinearity of approximately 0.1°C over the same operating range with no trimming. Although somewhat worse than what was obtained in the TT design, this linearity is still better than what has been reported for MOS-based temperature sensors. A Monte Carlo simulation was also run to test for not only corner variations, but for mismatch effects as well. In this simulation, mobility,

threshold voltage, and C_{OX} were all assigned uncorrelated variances of 10% of the nominal value. Results for 300 Monte Carlo simulations are summarized in Fig. 7 which is a histogram of the magnitude of the worst-case nonlinearity for each sample. These Monte Carlo simulations show no nonlinearities above 0.5°C. The mean value of the maximum temperature error is 0.104 °C, and the standard deviation is about 0.065 °C.

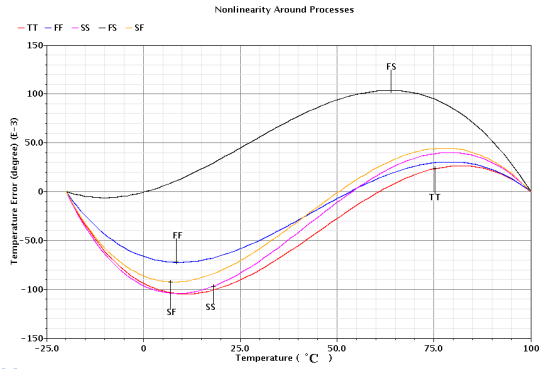

Figure 6. Temperature Error at different process corners (TT: typical; FF: fast NMOS fast PMOS; FS: fast NMOS slow PMOS; SS: slow NMOS slow PMOS; SF: slow NMOS fast PMOSnf

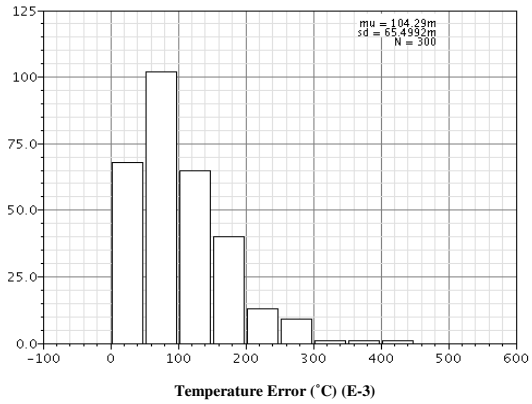

Figure 7. Temp Error at process and mismatch combined Monte Carlo simulation

Although the simulation results suggest no calibration is necessary to compensate for temperature nonlinearity if performance at the 0.5°C level is required, there are shifts in the level of the output and shifts in the slope with process variations. A single point calibration for offset and a batch calibration for slope would be needed to obtain reasonable overall accuracy or, depending upon slope variations within a batch, a two-temperature calibration may be needed to compensate for both offset and slope variations.

Finally, Table II provides the performance summary of this differential output temperature sensor.

It must be emphasized that the results presented here are based upon computer simulations and are dependent upon how well temperature effects are modeled in a commercial 0.18µ process. Experimental results will be presented at a later date.

V. CONCLUSIONS

In this work, a new compact V_{DD}-independent threshold-based differential output CMOS temperature sensor was proposed. The circuit has a very small active area and very low power dissipation. Simulation results in a 0.18µ CMOS process show a thermal nonlinearity of only 0.03°C using TT models and a nonlinearity of about 0.1°C over process corners without linearity trimming.

TABLE II SUMMARY OF PERFORMANCE

Parameters	Values
Process	1P6M 0.18µm
Power Supply	1.8V
Power Dissipation	72µW
Active Area	40µm²
Nonlinearity at Typical state (worst temperature error)	0.03°C
Nonlinearity around all the processes (worst temperature error)	0.11°C
Nonlinearity in Monte Carlo 300 times Simulation (worst temperature error)	0.11°C
Calibration	No

REFERENCES

[1] He, J., Zhao, C., Lee, A. and Peterson, K., "A linear very compact untrimmed on chip temperature sensors with second and third order temperature compensation", submitted to MWSCAS 2010.

[2] Bakker, A. and Huijsing, J., "Micropower CMOS Temperature Sensor with Digital Output", IEEE Journal of Solid State Circuits, pp. 933-937, July 1996

[3] Bakker, A.,"CMOS Smart Temperature Sensors – An Overview", Proc. IEEE Sensors Conference, pp 1423-1427, Vol. 2, 2002

[4] Pertijs, M., Makinwa, K., an dHuijsing, J., "A CMOS Smart Temperature Sensor with a 3σ Inaccuracy of ±1oC from -55oC to 125oC", IEEE Journal of Solid State Sircuits, PP. 2805-2815, Dec. 2005..

[5] M. Tuthill, "A switched-current, switched-capacitor temperature sensor in 0.6-um CMOS," IEEE J. Solid-State Circuits, vol. 33, no. 7, pp. 1117–1122, Jul. 1998.

[6] Masahiro, S., Member, Makoto, Ikeda, Member, IEEE, and Kunihiro Asada, Member, IEEEBakker, A.,"CMOS Smart Temperature Sensors – An Overview", Proc. IEEE Sensors Conference, pp 1423-1427, Vol. 2, 2002