Systematic Characterization of Subthreshold-MOSFETs-Based Voltage References for Ultra Low Power Low Voltage Applications

Jun He
Department of Electrical and Computer Engineering
Iowa State University
Ames, Iowa 50010, USA
sirenehe@iastate.edu

Degang Chen and Randall Geiger
Department of Electrical and Computer Engineering
Iowa State University
Ames, Iowa, 50010, USA
djchen@iastate.edu and rlgeiger@iastate.edu

***Abstract*—For low power low voltage, low area applications, voltage references based on MOS transistors operating in sub-threshold offer some attractive advantages over conventional bandgap-based structures. The lack of closed-form explicit expressions for the relationship between output and temperature for most subthreshold-based references makes it difficult to optimize performance and make quantitative comparisons with the performance of standard bandgap circuits. In this paper, a systematic and explicit characterization of the temperature characteristics for some of the basic sub-threshold-based voltage references is presented. A quantitive comparison of the performance of the basic sub-threshold references with that of the basic bandgap references is presented which shows that the temperature coefficient of the two structures are comparable. It is shown that the explicit characterization of the subthreshold-based references is useful for assessing the performance potential of these structures.**

I. INTRODUCTION

Driven by battery operated applications such as mobile communication systems, implantable biomedical products, and smart sensor networks, there is increasing pressure to decrease the supply voltage and power dissipation of the basic building blocks internal to the integrated circuits that enable these products. Voltage and current references are one of the most fundamental and critical building blocks in many of these integrated circuits. There is considerable demand for high-performance references that are physically small and that operate at very low power and low voltage levels.

It is well-known that some of the electrical properties of CMOS transistors operating in subthreshold are comparable to those of bipolar transistors but the subthreshold CMOS devices are often operated at much lower power levels [1]. Traditional bandgap references can provide very accurate outputs but their power consumption is generally substantially larger than reported in subthreshold MOSFETs based references [2]-[7]. Moreover, the area required for the parasitic BJT devices used in bandgap circuits built in standard CMOS technology occupy a large chip area [7]. Although several authors have introduced subthreshold-based CMOS references [5]-[7], few have focused on characterizing how design parameters influence basic performance characteristics of the references such as the inflection point, the curvature, the magnitude of the output voltage at a desired operating temperature, and the temperature coefficient (TC). In this work, a systematic approach is used to characterize the performance of some basic low power, low voltage references that express, in the output voltage, model parameters of MOS transistors operating in the subthreshold region. Specifically, an explicit analytical model for the references involving only process and model parameters will be developed. From the resulting output voltage expression, insights are provided on how the process parameters and design variables influence the temperature-dependent behavior of the reference voltage.

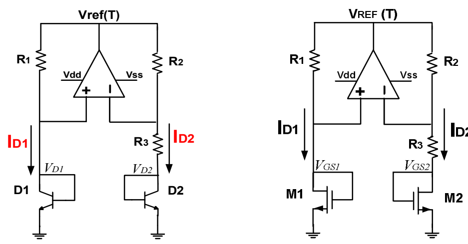
In Section II, the characterizations of the classic Kujik bandgap structure is reviewed using a systematic characterization approach [2] [9] [10]. In Section III, a subthreshold reference is obtained by replacing the bipolar elements in Kujik's circuit with MOS transistors operating in the subthreshold region. An explicit characterization of this subthreshold reference is also developed. In Section IV, an explicit characterization of another well known sub-threshold reference is presented. This explicit model makes it possible to quantitavely compare the performance of this reference with that of the bipolar and MOS variants of the Kujik structure. Section V is comprised of a summary of this work.

II. REVIEW OF BANDGAP RFERENCES CHARCTERIZATIONS

The classic bandgap voltage reference circuit proposed by Kujik is shown in Fig. 1(a) [2]. Assuming the Op Amp and resistors are ideal, a set of five equations can be written that completely characterize the circuit [9]

$$V_{ref}(T) = I_{D1}R_1 + V_{D1} \tag{1}$$

This work was sponsored, in part, by the National Science Foundation and the Semiconductor Research Corporation.



(a) (b)

Figure 1. Kujik's bandgap reference and its subthreshold counterpart

$$V_{D1} = V_{D2} + I_{D2}R_3 \tag{2}$$

$$I_{D2} = [V_{ref} - V_{D1}]/R_2 \tag{3}$$

$$V_{D1} = V_T \ln(I_{D1}) + V_{GO} - V_T[\ln(J_{sx} A_1) + m \ln T] \tag{4}$$

$$V_{D2} = V_T \ln(I_{D2}) + V_{GO} - V_T[\ln(J_{sx} A_2) + m \ln T] \tag{5}$$

where J_{sx} and m are the process parameters and independent of temperature, V_{GO} is bandgap voltage, A_1 and A_2 are the area factors for diode D_1 and D_2 respectively, V_T is thermal voltage equal to kT/q, k is Boltzman's constant, T is temperature in Kelvin, and q is the charge of an electron.

The general explicit expression for output voltage of Kujik's circuit can be obtained by eliminating the four unknowns I_{D1}, I_{D2}, V_{D1}, V_{D2} from (1)-(5).

$$V_{ref}(T) = a + bT - cT\ln(T) \tag{6}$$

where $a = V_{G0}$ (7)

$$b = \frac{k}{q}\left(\frac{R_2}{R_3}\ln\left(\frac{R_2}{R_1}\cdot\frac{A_2}{A_1}\right) + \ln\left(\frac{R_2 \cdot \ln\left(\frac{R_2}{R_1}\cdot\frac{A_2}{A_1}\right)\cdot\frac{k}{q}}{R_3 \cdot R_1 \cdot J_{sx} \cdot A_1}\right)\right) \tag{8}$$

$$c = \frac{k}{q}(m-1) \tag{9}$$

Equation (6) is a general formulation for the characterizations of bandgap voltage. From (6), four important specifications: the inflections point, the curvature, the magnitude of output voltage at the inflection point and the temperature coefficient TC can be readily obtained.

The inflection point can be found by differentiating V_{ref} with respect to temperature T, letting the derivative equal to 0 and solving T to determine the inflection point T_{inf}.

$$\frac{\partial V_{ref}}{\partial T} = b - c(1 + \ln T) = 0 \tag{10}$$

Solving (10), we obtain $T_{\text{inf}} = e^{b/c-1}$ (11)

Although it may appear that T_{inf} is dimensionless, the exponentiation is in units of K. Curvature can be found by computing the second derivative of the reference voltage evaluated at the inflection point. It serves as a measure of how rapidly the reference curvature opens up away from the inflection point.

$$\frac{\partial^2 V_{ref}}{\partial T^2}\Big|_{T=T_{\text{inf}}} = -\frac{c}{T}\Big|_{T=T_{\text{inf}}} = -\frac{c}{T_{\text{inf}}} = \frac{(1-m)k}{qT_{\text{inf}}} \tag{12}$$

It follows from (6) and (10) that the output voltage can be written as

$$V_{ref}(T_{\text{inf}}) = a + cT_{\text{inf}} = V_{G0} + \frac{kT_{\text{inf}}}{q}(m-1) \tag{13}$$

The thermal stability of reference circuits is often defined by temperature coefficient (TC). The definition of the TC in ppm is [3]

$$TC_{ppm} = \frac{V_{\max} - V_{\min}}{V_{ref}(T_{\text{inf}}) \cdot \Delta T} \cdot 10^6 \tag{14}$$

where V_{max} and V_{min} are respectively the maximum voltage and minimum voltage within the temperature range ΔT.

If the reference has a single inflection point, near the inflection point neighborhood, TC can be approximated as follows using second order Taylor series expansion

$$TC_{ppm} \approx \frac{1}{V_{ref}(T_{\text{inf}})}\frac{\partial^2 V_{REF}}{\partial T^2}\Big|_{T=T_{\text{inf}}} \cdot \frac{\Delta T}{8} \cdot 10^6 \tag{15}$$

From (12), (13) and (15), the TC of reference circuit can be expressed as

$$TC_{ppm} = \frac{-c}{a + c \cdot T_{\text{inf}}} \cdot \frac{\Delta T}{8 \cdot T_{\text{inf}}} \cdot 10^6 = \frac{(1-m)k/q}{V_{G0} + [(m-1)k/q] \cdot T_{\text{inf}}} \cdot \frac{\Delta T \cdot 10^6}{8 \cdot T_{\text{inf}}} \tag{16}$$

It is important to note that in (16), there are no design parameters and thus the designer has no control over the curvature in this structure.

III. CHARACTERIZATIONS OF SUBTHRESHOLD MOSFETS BASED KUJIK'S REFERENCE

In this section, we will apply a similar systematic approach to characterize the performance of the sub-threshold MOSFETs based references circuits. In Fig. 1(b), the diode elements D_1, D_2 in Fig. 1(a) are replaced by CMOS transistors operating in the sub-threshold region. A similar structure was used by Lo *et al* [7]. The I-V characteristics of the MOS transistor in sub-threshold can be modeled by (17) [8].

$$I_D = \eta\mu C_{ox} V_T^2 \frac{W}{L}\exp\left(\frac{V_{GS} - V_{th}}{nV_T}\right)\left[1 - \exp\left(-\frac{pV_{DS}}{nV_T}\right)\right] \approx \mu C_{ox} V_T^2 \frac{W}{L}\exp\left(\frac{V_{GS} - V_{th}}{nV_T}\right) \tag{17}$$

where I_D is the channel current through the MOS device, μ is the electron mobility in the channel, C_{ox} is the oxide capacitance per unit area, V_{th} is the threshold voltage, V_T is the thermal voltage, and n is the sub-threshold slope factor. For V_{DS}>0.1, current I_D is almost independent of V_{DS}. η is process parameter approximately equal to 1 in our process.

Assuming an ideal operational amplifier and resistors, the output voltage V_{REF} can be expressed as

$$V_{REF}(T) = V_{GS1} + I_{D1} \cdot R_1 \tag{18}$$

When R_1 and R_2 are equal, and when the threshold voltages of M_1 and M_2 are matched, it follows that

$$I_{D1} = I_{D2} = \frac{V_{GS1} - V_{GS2}}{R_3} = \frac{1}{R_3} \cdot nV_T \ln \frac{S_2}{S_1} \tag{19}$$

where S_1 *and* S_2 are the transistor aspect ratios W/L. The temperature dependence of mobility μ and threshold voltage V_{th} can be described by [11] [12]

$$\mu = \mu_0 T^{\alpha_\mu} \tag{20}$$

$$V_{th} = V_{th0} + \alpha_{Vt} T \tag{21}$$

where μ_0,V_{th0} , and α_{vt} are process parameters. It is assumed that these process parameters are constant and independent of temperature.

Combining (17)-(21), it follows that $V_{REF}(T)$ can be expressed as

$$V_{REF}(T) = a_{sub1} + b_{sub1} T - c_{sub1} T \ln T \tag{22}$$

where $a_{sub1} = V_{th0}$ (23)

$$b_{sub1} = n\frac{k}{q} \cdot \ln\left[\frac{n \cdot \ln(S_2 / S_1)}{R_3 \cdot \mu_0 \cdot C_{ox} \cdot S_1 \cdot k / q} \cdot \left(\frac{S_2}{S_1}\right)^{R_1/R_3}\right] + \alpha_{Vt} \tag{24}$$

$$c_{sub1} = n\frac{k}{q}(\alpha_\mu + 1) \tag{25}$$

The functional form of (22) is identical to that of the bandgap reference in (6). It thus follows (22)-(25) and the analysis in the previous section that the design variables in b_{sub1} must be set to obtain the desired inflection point from the equation

$$b - c(1 + \ln T_{\inf}) = 0 \tag{26}$$

The curvature of sub-threshold based Kujik's circuit can be expressed as

$$\frac{\partial^2 V_{REF}}{\partial T^2}\Big|_{T=T_{\inf}} = -\frac{c_{sub1}}{T}\Big|_{T=T_{\inf}} = -\frac{c_{sub1}}{T_{\inf}} = -\frac{n \cdot k \cdot (\alpha_\mu + 1)}{qT_{\inf}} \tag{27}$$

Similarly, the output voltage can be written as

$$V_{REF}(T_{\inf}) = a_{sub1} + c_{sub1} T_{\inf} = V_{th0} + n\frac{k}{q}(\alpha_\mu + 1) \cdot T_{\inf} \tag{28}$$

The TC can be expressed as

$$TC_{ppm} = \frac{-c_{sub1}}{a_{sub1} + c_{sub1} \cdot T_{\inf}} \cdot \frac{\Delta T \cdot 10^6}{8T_{\inf}} = \frac{-n(\alpha_\mu + 1)k / q}{V_{th0} + [nk / q \cdot (\alpha_\mu + 1)] \cdot T_{\inf}} \frac{\Delta T \cdot 10^6}{8 \cdot T_{\inf}} \tag{29}$$

It can be observed from (29) that there are no design parameters in the expression for the temperature coefficient. Thus, as was the case for the corresponding bandgap circuit of Fig. 1(a), the designer has no control over the TC of the subthreshold reference circuit of Fig. 1(b). Also, it can be easily shown by substituting (24) and (25) into (26) that $T_{\inf}$ is dependent upon the design parameters S_1, S_2, R_1, R_2, and R_3.

Fig. 2 shows how the inflection point changes with R_3 under the assumption that R_1=R_2 and $4S_1$=S_2 based upon both the analytical formulation and based upon Spectre simulations.

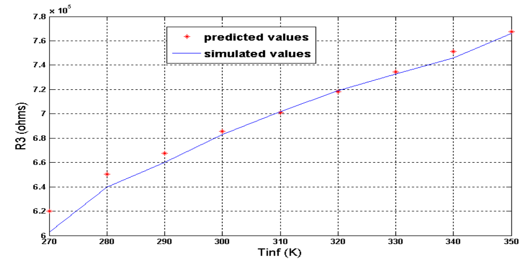


Figure 2. Inflection points of circuit in Fig. 2 changing with R_3

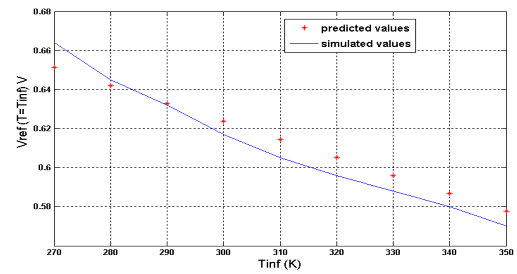


Figure 3. Output reference voltage changing with inflection points

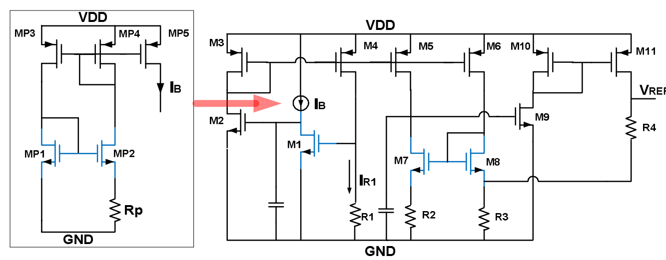


Figure 4. A well-known subthreshold based reference circuit [5]

A typical 0.18μ CMOS process was used with values of R_1=R_2=5MΩ, L_1=L_2=20μ, W_1=160μ, W_2=640μ. Correspondingly, the changing of the output voltage with the inflection point as obtained from both the analytical formulation and Spectre simulations is shown in Fig. 3. The comparisons show close correlation between the analytical formulation presented in this section and the Spectre simulations which use a much better model for the devices. A comparison of the thermal stability of the bandgap circuit of Fig. 1(a) and the subthreshold reference of Fig. 1(b) can be made by simply taking the ratio of the two temperature coefficients. If follows from (16) and (29) that

$$\frac{TC_{BG}}{TC_{sub}} = \frac{-c/(a + c \cdot T_{\inf})}{-c_{sub1}/(a_{sub1} + c_{sub1} \cdot T_{\inf})} = \frac{(1 - m)}{-n(\alpha_\mu + 1)} \frac{V_{th0} + [nk / q \cdot (\alpha_\mu + 1)] \cdot T_{\inf}}{V_{G0} + [(m - 1)k / q] \cdot T_{\inf}} \tag{30}$$

Using the typical 0.18 μm process parameters m= 2.3, n= 2.5, α_μ=-1.5, the ratio of TCs of the two types of structures is equal to -0.7. It suggests that the TCs of the two types are at the similar order but opposite sign at the same $T_{\inf}$.

IV. CHARACTERIZATIONS OF ANOTHER WELL KNOWN SUBTHRESHOLD BASED STRUCTURE

Another well known sub-threshold reference proposed by G. Giustolisi *et al* is shown in Fig.4 [5]. The reference circuit is made up of two main sub-circuits. The first sub-circuit is formed by bias current I_B and transistors M1-M4 and provides temperature dependent voltage V_{GS1}. The second sub-circuit is made by M5-M8 and generates a PTAT component. Transistors MP1- MP5 provides bias current I_B for the main sub-circuits. The sub-threshold transistors MP1, MP2, M1, M7 and M8 are highlighted in a different color from the remaining transistors. The output voltage V_{REF} can be expressed by

$$V_{REF}(T) = \alpha \cdot V_{GS1} + \beta \cdot V_T \tag{31}$$

where $\alpha = (\frac{R_4}{R_3}+1)\frac{S_5}{S_4}\frac{R_2}{R_1} - \frac{R_4}{R_1}\frac{S_6}{S_4}$, $\beta = n \cdot (\frac{R_4}{R_3}+1) \cdot \ln(\frac{S_8}{S_7} \cdot \frac{S_5}{S_6})$ (32)

Up to this point, V_{GS1} in (31) is still not written in an explicit form, making it hard to determine the actual circuit performance in terms of models parameters and temperature. Using the model in (17), V_{GS1} can be given as

$$V_{GS1} = nV_T \cdot \ln\frac{I_B}{\mu C_{ox} V_T^2 (W/L)_1} + V_{th} \tag{33}$$

where I_B is a PTAT current generated by MP1-MP5 and given by

$$I_B = \frac{1}{R_p} nV_T \cdot \ln(\frac{S_2}{S_1} \cdot \frac{S_3}{S_4}) \tag{34}$$

Combining (31)-(34), assume M1 is Fig.4 has the same threshold voltage as that of the transistors in Fig. 1 (b), the general explicit expression for the output reference voltage can be written as

$$V_{REF}(T) = a_{sub2} + b_{sub2} \cdot T - c_{sub2} T \cdot \ln T \tag{35}$$

where $a_{sub2} = \alpha \cdot V_{th0}$ (36)

$$b_{sub2} = \alpha \cdot n \cdot \frac{k}{q} \ln(\frac{n \ln(S_2/S_1)}{\mu_0 C_{ox} \cdot S_1 \cdot K_B T_0 / q \cdot R_p}) + \alpha \cdot \alpha_{Vt} + \beta \cdot k/q \tag{37}$$

$$c_{sub2} = \alpha \cdot n \cdot \frac{k}{q}(\alpha_\mu + 1) \tag{38}$$

The general formulation (35) again has exactly the same functional form that of the previous two circuits. The performance of sub-threshold based reference circuit can be easily obtained by using the previous standard procedure. The curvature of this sub-threshold reference can be expressed as

$$\frac{\partial^2 V_{REF}}{\partial T^2}|_{T=T_{\inf}} = -\frac{c_{sub2}}{T}|_{T=T_{\inf}} = -\frac{c_{sub2}}{T_{\inf}} = -\frac{\alpha \cdot n \cdot k \cdot (\alpha_\mu + 1)}{qT_{\inf}} \tag{39}$$

Similarly, $V_{REF}(T_{\inf}) = a_{sub2} + c_{sub2} T_{\inf} = \alpha[V_{th0} + n\frac{k}{q}(\alpha_\mu + 1) \cdot T_{\inf}]$ (40)

By comparing the performance of basic sub-threshold voltage reference of Fig. 1(b) with that in Fig. 4, it may appear that the designer has control over the curvature since the design parameter α appears in (39). But, in contrast to the previous circuit, the same design parameter α also appears in (40). It thus follows from (16) that the parameter α cancels in the expression for the TC and thus the designer has no control over the TC in this circuit either. A comparison of the curvature of the circuits of Fig. 1(b) and that of Fig.4 can be readily made. It follows that

$$\frac{TC_{sub2}}{TC_{sub1}} = \frac{\dfrac{-c_{sub2}}{a_{sub2} + c_{sub2} \cdot T_{\inf}}}{\dfrac{-c_{sub1}}{a_{sub1} + c_{sub1} \cdot T_{\inf}}} = \frac{-\alpha \cdot n \cdot \frac{k}{q}(\alpha_\mu + 1)}{\alpha[V_{th0} + n \cdot \frac{k}{q}(\alpha_\mu + 1) \cdot T_{\inf}]} \Bigg/ \frac{-n\frac{k}{q}(\alpha_\mu + 1)}{V_{th0} + n\frac{k}{q}(\alpha_\mu + 1) \cdot T_{\inf}} = 1 \tag{41}$$

Thus, at least based upon using device models presented here, the circuit of Fig. 4 demonstrates a TC that is identical to that of the circuit of Fig. 1(b) given the same process.

V. CONCLUSIONS

The performance of two voltage references using MOS transistors biased in the subthreshold region was compared with that of one of the most basic bandgap circuits. It was shown that, based upon the device models used, the functional form of the temperature dependence of the reference voltages are identical. It was also shown that the two subthreshold structures which appear to have fundamentally different architectures have identical temperature coefficients. Finally, explicit analytical expressions that characterize the temperature dependence of the subthreshold references were developed and this formulation is useful for design and optimization of the subthreshold references.

REFERENCES

[1] E. A. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operation," *IEEE J. Solid-State Circuits*, vol. SC-12, pp. 224–231, June 1977.

[2] K. Kuijk, "A Precision Reference Voltage Source", IEEE Journal of Solid State Circuits, Vol. 8, pp. 222-226, June 1973.

[3] P. Brokaw, " A Simple Three-Terminal IC Bandgap Reference", IEEE Journal of Solid State Circuits, Vol. 9, pp.388-393, Dec.1974

[4] H. Watanabe, S. Ando, M. Dainin, Y.J. Chun, and K. Taniguchi, "CMOS voltage reference based on gate work function differences in poly-si controlled by conductivity type and impurity concentration," IEEE J. Solid-State Circuits, vol.38, no.6, pp.987–994, June 2003.

[5] G. Giustolisi *et al.*, "A low-voltage low-power voltage reference based on subthreshold MOSFETs," *IEEE J. Solid-State Circuits*, vol. 38, pp. 151–154, Jan. 2003.

[6] G. De Vita and G. Iannaccone, "A sub-1-V, 10 ppm/C, nanopower voltage reference generator," *IEEE J. Solid-State Circuits*, vol. 42, no. 7, pp. 1536–1542, Jul. 2007.

[7] T. Lo, C. Huang, M. Ismail, "CMOS voltage reference based on threshold voltage and thermal voltage," Analog Integrated Circuits and Signal Processing, SpringerLink, June 2009.

[8] R.M. Swanson and J.D. Meindl, "Ion-implanted complementary MOS transistor in low-voltage circuits," IEEE J. Solid-State Circuits, vol.SC-7, pp.146-153, April 1972.

[9] J. He, R. Geiger and D. Chen, "A detailed analysis of nonideal effects on high precision bandgap voltage references," 51st Midwest Symposium on Circuits and Systems, pp. 382-385, Aug 2008

[10] X. Dai, D.Chen and R. Geiger, "Explicit characterization of bandgap references," in Proc. ISCAS 2006, 4 pp.573-576, May 2006

[11] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*. New York: McGraw-Hill, 1987

[12] K. R. Laker and W. M. C. Sansen, *Design of Analog Integrated Circuits and Systems*. New York: McGraw-Hill, 1994.