SNR Measurement Based on Linearity Test for ADC BIST

Jingbo Duan, Degang Chen
Department of Electrical and Computer Engineering
Iowa State University, Ames, IA 50011

Abstract —**Linearity and spectral performance test contributes most cost of ADC test. This paper presents a new method for testing an ADC's SNR from its linearity test data. The method does not require additional data acquisition or accurate sinusoidal stimulus. Data collected for linearity test is used to compute the input noise power and test ADC's SNR. Both simulation and experimental results show that the proposed method can estimate SNR value accurately.**

I. INTRODUCTION

Linearity and spectral performances are two major categories of specifications that are measured in analog-to-digital converter (ADC) test. The linearity performance, including INL and DNL, is tested by using the histogram method with either a sine wave or triangular wave input. The spectral performance, including SNR, THD, and SFDR, is tested by using the FFT method with a single tone sine wave input [1].

Test cost of ADC consists of high precision equipments and data acquisition time. To reduce test time, methods have been proposed to estimate linearity performance of an ADC based on FFT testing results [2, 3]. However, due to the loss of "high-frequency" details of ADC's transition levels, these methods are unacceptable in real applications in which transition levels matter. In application such as measurement instrumentation, auto motive control, and high resolution imaging, accurate linearity test is required. Estimating spectral performance based on linearity test data is an effective way of reducing test cost. For accurate spectral testing, both data acquisition time and computation time in traditional methods are significant. Significantly reducing this cost will meaningfully reduce the total test cost. An accurate and low cost method of estimating THD and SFDR of ADC based on INL data has been presented in authors' former work [4]. A method of estimating SNR from linearity test data is discussed in this paper.

Sine wave with high purity is required for spectral testing [5], which is a major challenge, especially for on-chip Built-In Self-Test (BIST). Removing this challenge is a giant step toward enabling BIST of deeply embedded ADCs. The idea of estimating the spectral performance using linearity test data becomes more valuable in applications of ADC BIST, where testing circuitry's area is more concerned than test time. A BIST scheme for testing SNR of a sigma-delta ADC is presented in [6]. The paper tries to replicate stand alone production test scheme on chip, which requires pure sine wave stimulus. Recently, research results have been published on reducing the accuracy requirement on linearity testing signal and simplifying its generation circuitry, which makes it possible to realize ADC linearity test on chip [7, 8]. Based on BIST results of its linearity, this method eliminates the need of accurate sine wave generation on chip for spectral test, making ADC BIST one step easier to implement.

In this paper, a method of estimating SNR based on linearity test of ADC is introduced. The method estimates SNR without requiring any additional hardware or data acquisition. Only a small amount of computation is required to estimate SNR. The rest of this paper is organized as following. In Section II, the relation between input noise power and noise contained in DNL test data is investigated first. The method of calculating input referred noise from DNL is then described. Simulation and experimental results are given in Section III and IV for validation.

II. NEW MTHOD OF ESTIMATING SNR

Conventional testing of spectral performance including SNR, THD, and SFDR is performed in frequency domain. A single tone sine wave is used as the input of ADC under test, and then the FFT of digital output codes is computed [5]. From the spectrum of output codes, SNR can be calculated from signal and noise power.

Standard testing method of spectral performance has high requirements on input sine wave generator. The generator should be able to generate sine wave with proper frequency so that coherent sampling can be achieved. The sine wave needs to be highly linear to approximate a single tone input. Building such a sine wave generator on chip with low cost is challenging. However, transfer curve linearity can be tested with low overhead by adopting stimulus error identification and removal (SEIR) method [7]. Computing spectral performance from linearity test data becomes a good approach, which needs only very small amount of hardware resources. In this section, the new method of estimating SNR from linearity test data is described.

A. Relation between input noise and DNL noise

Linearity performance including INL and DNL of an ADC is tested by histogram method using linear ramp as input. The noise contained by DNL comes from input referred noise but reduced by the histogram process. The

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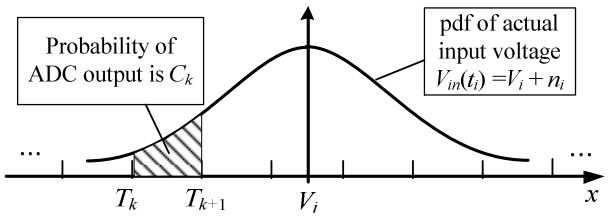

Fig.1. Noise effect in sampling

following statistical analysis investigates the relation between input noise and noise in tested DNL or code width.

Fig.1 shows the input voltage is sampled by the ADC at time t_i, in which V_i is the nominal input voltage, and n_i is input referred noise that added to input voltage. T_k and T_{k+1} are transition levels of the ADC. If the actual voltage sampled by the ADC is within the range $[T_k, T_{k+1})$, the ADC generates digital code C_k. The total input voltage V_{in} at time t_i is a random variable with normal distribution. The probability density function (pdf) $V_{in}(t_i)$ is

$$f(V_{in}(t_i) \mid x) = \frac{1}{\sigma_n \sqrt{2\pi}} \exp\left(-\frac{(x - V_i)^2}{2\sigma_n^2} \right) \tag{1}$$

In this equation, σ_n is the standard deviation of input noise; V_{in} the actual input voltage value of the ADC at time t_i. Due to noise of the ADC, the input voltage at time t_i could be converted into several different codes. If we look at the range of $[T_k, T_{k+1})$, the probability of input voltage actually sampled as a value within this range is given by (2), which is also the probability of ADC generates C_k at time t_i.

$$P_k(i) = \frac{1}{2} erf\left(\frac{T_{k+1} - V_i}{\sigma_n \sqrt{2}} \right) - \frac{1}{2} erf\left(\frac{T_k - V_i}{\sigma_n \sqrt{2}} \right) \tag{2}$$

Consider histogram based linearity test of an ideal n-bit ADC, the number of transition levels is the 2^n-1 and total number of samples is M. During the test, the value of i in (1) and (2) goes from 1 to M. We define a random variable as following

$$X_k(i) = \begin{cases} 1 & V_{in}(t_i) \in [T_k, T_{k+1}) \\ 0 & other \end{cases} \tag{3}$$

From (2) we know that the probability of $X_k(i)$ equals to 1 is $P_k(i)$. After the data acquisition is finished, the number of hits of C_k is

$$h_k = \sum_{i=1}^{M} X_k(i) \tag{4}$$

Denote the code width value of code C_k as $W_i(k)$. As mentioned above, the ADC under test is assumed to be ideal, so $W_i(k)$ equals to 1. However, tested value of $W_i(k)$ is not 1. From histogram linearity test, the value of $W_i(k)$ is calculated as

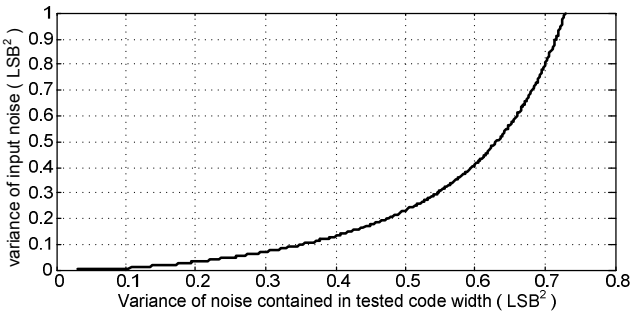

Fig.2. Relation between input noise and noise in DNL

$$\hat{W}_i(k) = \frac{h_k}{\bar{h}} = \frac{1}{\bar{h}} \sum_{i=1}^{M} X_k(i) \tag{5}$$

where h_k is the number of hits of code C_k and $\bar{h}$ is the average number of hits per code. Due to input noise, $\hat{W}_i(k)$ is a random variable and its variance is

$$\sigma^2\left(\hat{W}_i(k)\right) = \frac{1}{\bar{h}^2} \sum_{i=1}^{M} \mathrm{var}\left(X_k(i)\right) \tag{6}$$

From (2) and (3), (6) can rewrite as

$$\sigma^2\left(\hat{W}_i(k)\right) = \frac{1}{\bar{h}^2} \sum_{i=1}^{M} P_k(i)\left(1 - P_k(i)\right) \tag{7}$$

Above analysis gives the relation between input noise and noise contained in tested code width values, however it is difficult to obtain explicit expression of the relationship due to M integrals of error function. Instead, write the relation as a generic form

$$\sigma^2\left(\hat{W}_i(k)\right) \cdot \bar{h} = f\left(\sigma_n^2\right) \tag{8}$$

Equation (8) can be solved numerically by using (2) and (7) and it is shown that input referred noise can be calculated from noise contained in code width data. For ADC with reasonably performance, a look up table with several hundred items can provide enough accuracy. Since only average number of hits per code shown in the relation, the look up table can be used for different resolution ADCs. Fig.2 shows the look up table when $\bar{h}$ equals to 1.

If coherent sampling condition is satisfied and the linear ramp has proper overdrive, $\left\{\hat{W}_i(k) \mid k = 1, 2 \ldots 2^n - 2\right\}$ are independent and identical distributed (iid) random variables. $\hat{W}_i(k)$ has the same variance as shown in (7) when k goes from 1 to 2^n-2. After all code width values of 2^n-2 codes are measured, we have 2^n-2 samples of these iid random variables. Before measurement, code width of 2^n-2 codes are iid random variables theoretically. After an actual measurement, a set of samples are acquired. Denote the set of samples as $\left\{\hat{w}_i(k) \mid k = 1, 2 \ldots 2^n - 2\right\}$. Sample variance of the measured code width values is

$$S^2_{\hat{w}_i} = \frac{1}{2^2-3}\sum_{k=1}^{2^2-2}\left(\hat{w}_i(k)-\overline{\hat{w}_i}\right)^2 \quad (9)$$

in which $\overline{\hat{w}_i}$ is the mean value of $\hat{w}_i(k)$. Sample variance $S^2_{\hat{w}_i}$ calculated from all code width values is the unbiased estimation of the variance of $\sigma^2\left(\hat{W}_i(k)\right)$. Therefore $S^2_{\hat{w}_i}$ is used (8) and the lookup table to obtain input noise power. The relation between code width and DNL is very simple as shown in (10). Code width values can be substitute by corresponding DNL values after static linearity testing.

$$\hat{DNL}(k) = \hat{w}_i(k) - 1 \quad (10)$$

B. Removing Effect of DNL of real ADCs

Analyses in part *A* are based on an ideal ADC, which means the code width *W*(*k*) is 1. Real ADCs have nonzero code width values. Code widths of a real ADC $\{W(k) \mid k = 1,2...2^n-2\}$ are random variables at design stage. For well-designed ADC, code width variation comes from process variation. It can be assume that they have identical distribution. After fabrication, true code widths of the ADC are fixed and 2^n-2 samples of these random variables. Denote the true values of all code widths of the ADC after fabrication as $\{w(k) \mid k = 1,2...2^n-2\}$. Similar to (9), the unbiased estimation of $\sigma^2(W(k))$ is S^2_w from $w(k)$. Combine with analyses in part *A*, tested $\hat{W}(k)$ contains two parts. One is the true value of *W*(*k*) which is a sample of a random variable. The other is noise coming from input noise *NW*(*k*). Suppose *W*(*k*) and *NW*(*k*) are independent, the variance of tested code width value is

$$\sigma^2\left(\hat{W}(k)\right) = \sigma^2(W(k)) + \sigma^2(NW(k)) \quad (11)$$

$\sigma^2\left(\hat{W}(k)\right)$ is what can be estimated from 2^n-2 measured code widths as shown in (9). $\sigma^2(NW(k))$ is what can be used to test input noise of the ADC according to Fig.2. $\sigma^2(W(k))$ is unwanted term.

To obtain the value of $\sigma^2(NW(k))$, the output codes collected for linearity test can be split into two groups. Denote these collected output codes as $\{D(i) \mid i = 1,2...M\}$. After splitting, one group is the original data set containing *M* points. The other group could be either $\{D(i) \mid i = 1,3...M-1\}$ or $\{D(i) \mid i = 2,4...M\}$ containing *M*/2 points. Histograms are performed on these two groups of output codes and 2 different sets of code width test data are obtained. Average number of hits per code of these two histogram are $\overline{h_1}$ and $\overline{h_2}$ respectively. From the first group, 2^n-2 code width $\{w_1(k) \mid k = 1,2...2^n-2\}$ of the ADC is tested. Sample variance of these code width values is

$$S^2\left(\hat{W}_1(k)\right) = S^2(W(k)) + \frac{1}{\overline{h_1}} f\left(\sigma_n^2\right) \quad (12)$$

Similarly, from the second group data, 2^n-2 code width $\{w_2(k) \mid k = 1,2...2^n-2\}$ of the ADC is tested. Sample variance of these code width values is

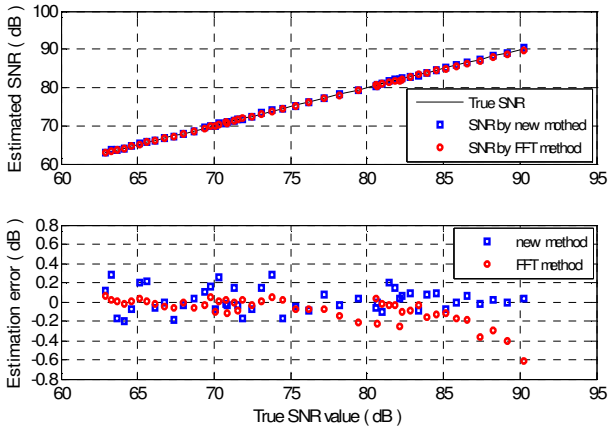

Fig.3. SNR tested by FFT method and the new method

$$S^2\left(\hat{W}_2(k)\right) = S^2(W(k)) + \frac{1}{\overline{h_2}} f\left(\sigma_n^2\right) \quad (13)$$

From (12), (13) and the lookup table shown in Fig.2, variance of input referred noise can be obtained as shown in (14). And full scale SNR of the ADC is calculated by (5).

$$\hat{\sigma}_n^2 = f^{-1}\left(\overline{h_1}\cdot\overline{h_2}\cdot\frac{S^2\left(\hat{W}_1(k)\right) - S^2\left(\hat{W}_2(k)\right)}{\overline{h_2}-\overline{h_1}}\right) \quad (14)$$

$$\hat{SNR} = 20\log_{10}\left(\frac{FS^2/8}{\hat{\sigma}_n^2 + 1/12}\right) \quad (15)$$

The assumption of code width of the fabricated ADC is random variable may not be totally true in real ADCs. In some ADC structures such as pipeline and SAR, DNL has several large values caused by MSBs of the ADC. Fortunately number of these large values is small so that they can be excluded when $S^2\left(\hat{W}_1(k)\right)$ and $S^2\left(\hat{W}_2(k)\right)$ are calculated.

III. Simulation Results

The method of estimating SNR from linearity test data has been investigated and validated by simulations. ADCs under test are modeled as a set of transition levels and randomly generated in MATLAB. 48 different ADCs with resolution 12 bits, 14 bits, and 16 bits are randomly created. Gaussian noise with standard deviation changing from 0.2 LSB to 2LSB is added to the input signal to model the input referred noise from ADC itself. SNR is measured by both traditional 32768 points FFT method and the new method. In the new method, linearity is first tested by histogram method with linear ramp. 32 hits per code are used in the histogram test so the total number of points is 2^{n+5}. Output codes are divided into 16 groups so that total number of points in each group is 2^{n+1}. Equivalently, the linearity is tested 16 times with 2 hits per code histogram. The input referred noise is calculated according to (12)-(16). Fig.3

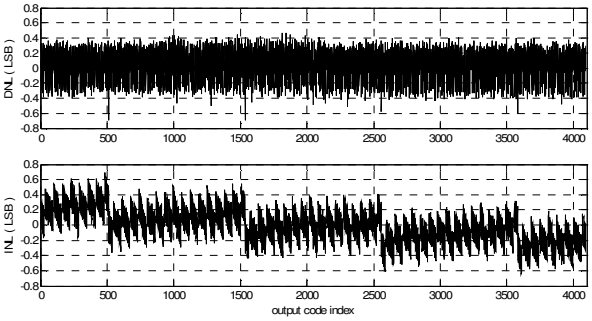

Fig.4. DNL and INL of ADC1

Table.1. Performance of four ADCs

	ADC1	ADC2	ADC3	ADC4
DNL(LSB)	+0.47/-0.69	+0.45/-0.67	+0.51/-0.68	+0.49/-0.75
INL(LSB)	+0.69/-0.65	+0.59/-0.63	+0.64/-0.65	+0.77/-0.71
SNR(dB)	72.07	72.24	72.14	71.98
THD (dB)	-86.8	-85.6	-84.8	86.4

Table.2. Estimation results of the proposed method

	ADC1	ADC2	ADC3	ADC4
var(DNL) (LSB^2)	0.0303	0.0197	0.0237	0.0326
SNR_FFT (dB)	72.07	72.24	72.14	71.98
SNR_new (dB)	72.27	72.09	72.13	72.27
Δ(SNR) (dB)	0.2	-0.15	-0.01	0.29

compares measurement results of two methods, in which, black curve is the true value of SNR, red circles are SNR values measured by traditional FFT method, and the blue squares are SNR values estimated by the new method. From the plot, estimation errors of traditional FFT method are smaller 0.2dB when SNR is low. It increases when SNR increases due to harmonic distortion effect. Estimation errors of the new method are smaller than 0.4dB. The estimation error decreases when resolution increases because more number of samples is available.

IV. Experimental Results

The method of estimating full scale SNR value from linearity test data has also been validated from measurement. Four different 12-bit SAR ADCs are tested by both traditional method and the new method. All ADCs are tested by 32768 points traditional FFT method which will be regarded as the reference. Performances of these four ADCs are listed in Table.1.

Linearity is tested by histogram method using sine wave stimulus. Fig.4 shows the DNL and INL of ADC1. 80 hits per code are used in the histogram test so the total number of points is 80×2^{12}. Output codes are divided into 32 groups so that total number of points in each group is 10240. Equivalently, the linearity is tested 32 times with 2.5 hits per code histogram. To obtain two variances of tested DNL required in (12) and (13). DNL is divided into two groups. One is the middle half from 1024^{th} point to 3072^{th} point, and the other one is the combination of two ends. The middle part corresponds to the region $[\pi/4, 3\pi/4]$ of cosine wave input, in which number of hits per code is smaller. Then the input referred noise is calculated according to (13)-(16).

Table.2 compares estimation results of the new method to traditional method. The 2^{nd} row is variance of true DNL obtained from (14) the unit of which is LSB^2. The 5^{rd} row is the direct subtraction of SNR dB value tested by the new method and SNR value tested by traditional FFT method. All differences are very small, which means very good estimation accuracy can be achieved by the new method. The 6^{th} column is the difference of noise power measured in two methods.

V. Conclusion

A method of testing SNR based on linearity test data is presented in this paper. Accurate linearity test of ADC is required by many applications and can be implemented on chip with low cost. Under the condition that linearity has been tested, testing spectral performance by another round of data collection is not necessary. This method only needs small amount of computation to estimate SNR. It eliminates hardware and data acquisition time cost of spectral performance test. Simulation and experimental results show that the estimation accuracy of SNR value using the proposed method is comparable to traditional FFT method.

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