Fast & Accurate Algorithm for Jitter Test with a Single Frequency Test Signal

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***Abstract*— A fast and accurate algorithm for jitter test is presented. The proposed method uses a single test with a high frequency input sine wave. Elimination of the need of a 2nd low frequency test required in the IEEE standard test offers significant savings on both hardware and data acquisition time. The new method is computationally efficient since it requires only one FFT together with some simple time domain computation. Furthermore, there are no nonlinear operations involved, avoiding errors inherently associated with such operations. Theoretical analysis, extensive simulation results, and experimental results validated the computational efficiency and test accuracy. The new algorithm is also shown to be robust with respect to harmonic and non-harmonic distortions. The algorithmic simplicity and the relaxed hardware requirement make the new method well suited for built-in self test.**

***Index Terms*—Fast Fourier Transform (FFT), jitter, spectral testing.**

I. Introduction

The jitter is an important specification of Analog-to-Digital Converters (ADCs) or other sampling circuits, which characterizes the random variation in the sampled instant caused by the variations in the sampling clock or sampling circuitry itself. This parameter is of special importance as the signal frequency and data rate become more and more high. In some applications, the jitter has become the ultimate limit of system performance. The reference [1] shows that, because of the uncertainty in the sampling instant due to jitter, the resolution of ADC falls by about 1 bit for every doubling of the sampling rate at sampling rates ranging from 2 MS/s to 4 GS/s.

Many jitter measurement methods have been presented in prior works such as in IEEE standard 1057 [2][3], Analog Device Inc. [4], and Texas Instruments Inc. [5] and so on. And these methods have been serving community well, especially in characterization test. A common characteristic in the methods mentioned above is that all of them require both a low frequency and a high frequency signal tests, and the two frequencies should have sufficient separation. As it's well known that ADC test needs some expensive ATEs (Automated Test Equipments), high-precision synthesizers, high performance signal generators, etc [6], compared with a single frequency test, the dual frequencies test increases the test cost greatly. Furthermore, for on-chip test, dual frequencies test with sufficient frequency separation can be many times more than a single frequency test because the low frequency on-chip test needs large capacitors and inductors which consume large die area. Therefore, the dual frequencies test methods are challenging to be built on chip.

In order to reduce test cost and make on-chip jitter test possible, a fast and accurate algorithm for jitter test is proposed in this paper. The proposed method requires only a single test with a high frequency input sine wave. Compared with the conventional dual frequencies test, the new method cuts the test time by 1/2. In the proposed method, the ADC output data is collected with a given high frequency input signal. Then FFT is used to estimate the fundamental, harmonic, inter-modulation distortion and DC components. The error sequence is obtained by removing the fundamental, harmonic, inter-modulation distortion and DC components from the original data. Then the error sequence is sorted into two sets according the identified fundamental's phase. Finally, the root mean square (RMS) jitter is estimated from the difference between the two sets. The proposed method requires only a single test with a high frequency input sine wave. Both hardware and data acquisition time are saved significantly due to the elimination of the need of 2nd low frequency test required in IEEE standard test, ADI and TI method.

Compared to the method in the reference [7] which requires a single frequency signal test, the new method is computationally efficient since it requires only one FFT together with some simple time domain computation. Furthermore, there are no nonlinear operations involved, avoiding errors inherently associated with such operations. Thereby the proposed method is robust to harmonic and non-harmonic distortions.

It should be stressed that the measurement result of the proposed method, similar to IEEE standard method, TI and ADI method, includes the jitter of the sampling clock generator, the jitter of input signal generators and the ADC internal aperture jitter. The jitter of any one of these elements can be accurately measured as long as the jitter introduced by the other two elements is substantially lower than that of the element under test, since jitter combines on an root-sum-

square (rss) basis [8]. Furthermore, the proposed method is not only limited to ADC jitter test, but it is also suited to test the jitter in other sampling circuits, such as a Sample and Hold (S/H) circuit (followed by a analog signal digitizer) or any other clocked sampling element that is subject to jitter.

The rest of this paper is organized as follows. In the next section, the fast and accurate algorithm for jitter test is proposed, which requires only a single test with a high frequency input sine wave. The simulation and experimental results that validate the proposed algorithm are reported in Section III and IV respectively. Finally some conclusions about the presented work are extracted in Section V.

II. Fast and Accurate Jitter Test

In this section, a fast and accurate jitter test method is proposed in detail. Let Vin(t) denote the input signal of an ADC. The output of the ADC is a sequence of samples x_n with length M, given by

$$\begin{aligned} x_n &= V_{in}(nT_s+\delta t_n)+V_{hd}(nT_s)+V_{im}(nT_s) \\ &+V_{noise}(nT_s)+V_q(nT_s),\ \text{n=0,1,2,3,..., M-1} \end{aligned} \tag{1}$$

In (1), T_s represents the ideal sampling period for the ADC, δt_n is a random timing variable representing the total jitter, $V_{hd}(nT_s)$ represents the harmonic distortion component, $V_{im}(nT_s)$ represents the inter-modulation distortion component (sometimes the inter-modulation between input signal and the sampling clock signal may exist, it can be seen from the latter experimental result in Section IV), $V_{noise}(nT_s)$ represents the equivalent input noise of ADC which includes the internal noise in ADC and the noise carried by the input signal, $V_q(nT_s)$ represents quantization error of ADC. Our goal is to identify the techniques to estimate the variance of the random variable δt_n.

According to Taylor formula, equation (1) can be easily converted to

$$\begin{aligned} x_n &\approx V_{in}(nT_s)+\frac{dV_{in}}{dt}\delta t_n \\ &+V_{hd}(nT_s)+V_{im}(nT_s)+V_w(nT_s) \end{aligned} \tag{2}$$

here $V_w(nT_s)=V_{noise}(nT_s)+V_q(nT_s)$. From (2) we can see that the jitter δt_n is modulated by signal slope when it is converted to noise.

For sine wave input,

$$V_{in}(t)\approx A\sin(2\pi ft+\varphi) \tag{3}$$

In (3), A, f and φ are the amplitude, frequency, and initial phase of sine wave respectively. The slope of the input signal is given by

$$\frac{dV_{in}}{dt}\approx 2\pi fA\cos(2\pi ft+\varphi) \tag{4}$$

From (4) we can see that signal slope depends on frequency, amplitude and time. Substituting (3) and (4) into (2), we get

$$\begin{aligned} x_n &\approx A\sin(2\pi fnT_s+\varphi) \\ &+2\pi fA\cos(2\pi fnT_s+\varphi)\delta t_n \\ &+V_{hd}(nT_s)+V_{im}(nT_s)+V_w(nT_s) \end{aligned} \tag{5}$$

In (5), the deterministic components are the fundamental and harmonic, inter-modulation distortion components, which can be identified with reasonable accuracy. The component V_w is expected to remain at the same power level regardless the signal level. The jitter related term has a coefficient depending on the fundamental's phase.

From FFT of the raw data x_n, the fundamental, harmonic and inter-modulation distortion components can be estimated with reasonable accuracy. Subtracting the estimated fundamental, harmonic, inter-modulation distortion components from the raw data x_n, we can get the error sequence e_n

$$e_n\approx x_n-\hat{A}\sin(2\pi\hat{f}(n-1)T_s+\hat{\varphi})-\sum\hat{V}_{hdi}-\sum\hat{V}_{imj} \tag{6}$$

In (6), $\hat{A}$, $\hat{f}$, $\hat{\varphi}$, $\hat{V}_{hdi}$ and $\hat{V}_{imj}$ are the estimated values of A, f, φ, the i-th harmonic component V_{hdi} and the j-th inter-modulation distortion component V_{imj} respectively. Combining (5) and (6), we get

$$e_n\approx 2\pi\hat{f}\hat{A}\cos(2\pi\hat{f}nT_s+\hat{\varphi})\delta_{tn}+V_w(nT_s) \tag{7}$$

Equation (7) quantifies the well-known concept that when an ADC is sampling a sinusoidal input, the contribution of its jitter is much more pronounced when the sampling instant coincides with the zero-crossing of the input (where $\cos(2\pi\hat{f}nT_s+\hat{\varphi})$ is large), and has very little impact on the output noise when the sampling instant coincides with the top or bottom of the input sine wave (where $\cos(2\pi\hat{f}nT_s+\hat{\varphi})$ is small). Therefore, we can make use of this concept in jitter test.

Let θ be the fundamental's phase

$$\theta=2\pi\hat{f}nT_s+\hat{\varphi} \tag{8}$$

Then the phases of the zero-crossing of the input are given by

$$\{\theta_H\}=\{\theta\,|-\frac{\pi}{4}+i\pi\le\theta\le\frac{\pi}{4}+i\pi, i=0,\pm1,\pm2,\pm3,...\} \tag{9}$$

The phases of the top or bottom of the input are given by

$$\{\theta_L\}=\{\theta\,|\,\frac{\pi}{4}+i\pi<\theta<\frac{3\pi}{4}+i\pi, i=0,\pm1,\pm2,\pm3,...\} \tag{10}$$

Note that $\{\theta_H\}$ and $\{\theta_L\}$ are two equal sets with length M/2, thus $\{e_n\}$ is sorted into two equal sets $\{e_{Hn}\}$ and $\{e_{Ln}\}$ with length M/2 according to the identified fundamental's phase.

$$e_{Hn}\approx 2\pi\hat{f}\hat{A}\cos(\theta_H)\delta_{tn}+V_w \tag{11}$$

$$e_{Ln}\approx 2\pi\hat{f}\hat{A}\cos(\theta_L)\delta_{tn}+V_w \tag{12}$$

Note for all e_n's in $\{e_{Hn}\}$, the absolute value of the coefficient $\cos(\theta_H)$ is larger than $1/\sqrt{2}$, and for all e_n's in $\{e_{Ln}\}$, the absolute value of the coefficient $\cos(\theta_L)$ is less than or equal to $1/\sqrt{2}$. As a example, Fig. 1 illustrates that $\{e_n\}$ is sorted into $\{e_{Hn}\}$ and $\{e_{Ln}\}$ according to the identified

fundamental's phase. The lower one shows that a 9-bit ADC output codes in time domain. It should be pointed out that he input signal frequency is near Nyquist frequency. The upper one shows that $\{e_n\}$ is sorted two distinguished sets $\{e_{Hn}\}$ and $\{e_{Ln}\}$.

Then the power of e_{Hn} and e_{Ln} can be derived as following

$$P_{e_H} = \left(2\pi \hat{f}\,\hat{A}\right)^2 \left(\frac{1}{2}+\frac{1}{\pi}\right)\sigma_{\delta t}^2 + \sigma_w^2 + \varepsilon_H \tag{13}$$

$$P_{e_L} = \left(2\pi \hat{f}\,\hat{A}\right)^2 \left(\frac{1}{2}-\frac{1}{\pi}\right)\sigma_{\delta t}^2 + \sigma_w^2 + \varepsilon_L \tag{14}$$

Where $\sigma_{\delta t}^2$ is the variance of jitter δ_{tn}, σ_w^2 is the power caused by the noise and quantization errors, ε_H and ε_L are due to the residual harmonic and inter-modulation components error presents in e_{Hn} and e_{Ln} respectively. ε_H and ε_L can be eliminated if we only consider the power coming from the noise floor in FFT of $\{e_{Hn}\}$ and $\{e_{Ln}\}$. Additionally, it is obvious that P_{e_H} is larger than P_{e_L}.

From (13) and (14), we can get the total jitter variance

$$\sigma_{\delta t}^2 = \frac{P_{e_H} - P_{e_L}}{8\pi(\hat{f}\hat{A})^2} \tag{15}$$

Therefore, the RMS total jitter is

$$\sigma_{\delta t} = \sqrt{\frac{P_{e_H} - P_{e_L}}{8\pi(\hat{f}\hat{A})^2}} \tag{16}$$

where P_{e_H} and P_{e_L} are easily obtained by computing the variance of of $\{e_{Hn}\}$ and $\{e_{Ln}\}$ respectively

$$P_{e_H} = VAR\{e_{Hn}\} \tag{17}$$

$$P_{e_L} = VAR\{e_{Ln}\} \tag{18}$$

The procedure of the fast and accurate algorithm for jitter test can be outlined in the following six steps.

a) With given input and clock signal, collect data x_n with record length M (even).

b) Use FFT to estimate fundamental, harmonic, intermodulation distortion and DC components.

c) Subtract the estimated fundamental, harmonic, inter-modulation distortion and DC components from data x_n to form error sequence e_n.

d) Use identified fundamental's phase to sort e_n into two equal sets (e_{Hn} and e_{Ln}) with length M/2.

e) Compute P_{e_H} and P_{e_L} using equation (17) and (18) respectively.

f) Compute RMS jitter using equation (16).

In the proposed method, only a single test with a high frequency input sine wave is required. Compared with IEEE standard method, TI and ADI method which require another low frequency test, the proposed method saves on both hardware and data acquisition time. In the new method, the only FFT on data x_n may be required for computing other dynamic parameters, such as SNR (Signal-to-Noise Ratio),

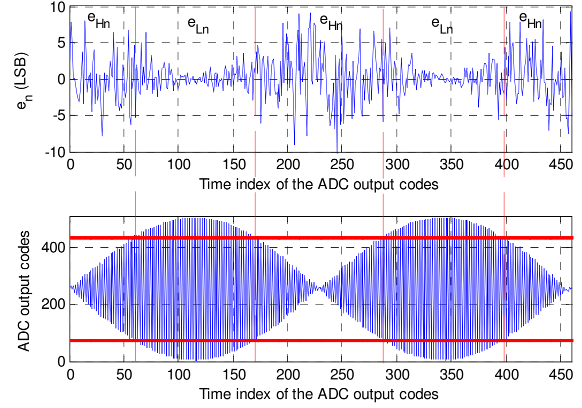

Fig. 1 $\{e_n\}$ is sorted into $\{e_{Hn}\}$ and $\{e_{Ln}\}$ according to the identified fundamental's phase

THD (Total Harmonic Distortion), SFDR (Spurious Free Dynamic Range), SIAND (Signal-to-Noise-and-Distortion Ratio), ENOB (Effective Number of Bits), etc [9]. In the introduced method, no nonlinear operation is involved and the harmonic and inter-modulation distortion components are excluded. So it is accurate and robust to harmonic and non-harmonic distortion. Therefore, the proposed method is cost-effective and computationally efficient, and it is potential to be built on chip.

III. Simulation Results

In order to validate the theoretical analysis presented in Section II, some simulations in MATLAB were developed, where a known amount of jitter is taken into account.

Specifically, the simulation environment is set up as follows. ADC is modeled as a set of transition levels. Its nonlinearity error is chosen to be a Gaussian random variable with zero mean and a given standard deviation σ_{DNL}. Three ADCs are simulated in the simulations. The first one is a 9-bit ADC with σ_{DNL}=0.07 LSB (least significant bit); the second one is a 12-bit ADC with σ_{DNL}=0.02 LSB; the third one is a 14-bit ADC with σ_{DNL}=0.008 LSB. The input of ADC is a pure sine wave whose amplitude was set at 96% of the full scale range of the converter. The additive measurement noise is introduced at the input node of the ADC under test. And it is a Gaussian distribution with zero mean and a standard deviation σ_{noise}=1 LSB. A sine signal generator is used to generate a high frequency pure sine wave. The jitter is a random error added to the ideal sampling time. It is a Gaussian distribution with zero mean and standard deviation $\sigma_{\delta t}$.

Table I shows the estimated RMS jitter by the proposed algorithm under different cases. In Table 1, N represents the resolution of the ADC, f_{clk} is the frequency of sampling clock, f_{sig} is the frequency of input signal. In each case, the number of collected data x_n is 4096 and the data is coherent. As expected, from Table 1 we can see that the estimated RMS jitter is very close to the ideal RMS jitter.

Fig. 2 shows the spectrum of the simulated 14-bit 200 MS/s ADC's output when the frequency of input signal is

364.306641 MHz. In Fig. 2, the two largest bins are the signals aliased into Nyquist zone. The noise floor is about -88 dB, which seems not consistent with that of a reasonable 14-bit ADC. In general, the noise floor of a reasonable 14-bit ADC should be about -120 dB when the number of collected data x_n is 4096 [2]. The rise of the noise floor is due to the jitter. Because the frequency of input signal is much higher than Nyquist frequency, the jitter is very large.

The spectrums of e_{Hn} and e_{Ln} are shown in Fig. 3. The upper one and the lower one are the spectrums of e_{Hn} and e_{Ln} respectively. From Fig. 3 we can see that the noise floor of e_{Hn} is larger than that of e_{Ln}. The reason is that e_{Hn} corresponds to many zero-crossing sampling points, where the input signal slope is very steep. As we have known that the jitter is modulated by the signal slope when it is converted to noise. So the noise floor of e_{Hn} is large.

Therefore, the simulation results show that the proposed algorithm requiring only a single test with a high frequency input sine wave can estimate the jitter accurately.

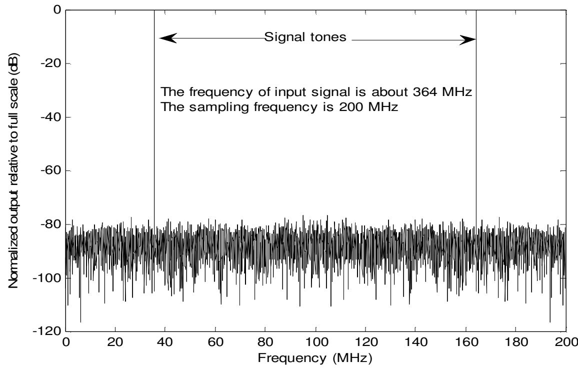

Fig. 2 The spectrum of simulated 14-bit ADC output

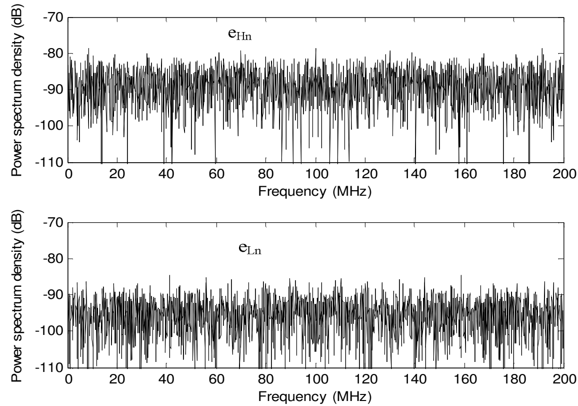

Fig. 3 The spectrums of simulated e_{Hn} and e_{Ln}

TABLE I. THE COMPUTED RMS JITTER UNDER DIFFERENT CASES

N/bits	f_{clk} */MHz*	f_{sig} */MHz*	*Ideal* $\sigma_{\delta t}$ /ps	*Computed* $\sigma_{\delta t}$ /ps
9	1000	249.755859	2	2.01
9	1000	498.291016	5	5.02
12	400	187.207031	2.5	2.50
12	400	187.207031	5	5.01
14	200	198.486328	1	1.01
14	200	298.486328	1	0.98
14	200	364.306641	1	1.01

IV. Experimental Results

The proposed method has been implemented on a commercial 9-bit 800 MS/s time-interleaved pipeline ADC.

In jitter test with a single frequency test signal, the sampling frequency is generally set for the maximum allowable and the frequency of input signal is also set high, where the effects of clock and aperture jitter on the ADC output errors are noticeable. Depending on the ADC, the frequency of input signal may be as high as Nyquist frequency. In this test, the sampling frequency is 800MS/s. The input is a sine wave with full scale amplitude and its frequency is about 399MHz, which is near Nyquist frequency. The collected data x_n is coherent with a data record length of 16384. The ADC is actually made of two 400MS/s time-interleaved ADCs together to achieve 800MS/s. For the timing skew between the two channels of the combined ADC causes non-harmonic errors that are not due to jitter, we prefer to use one of the time-interleaved ADC rather than the combined ADC for jitter test. Therefore, the collected data x_n was broken into two separate subsets: the first one contains the odd numbered samples, and the second one contains the even numbered samples. The proposed algorithm is then implemented on one of the two subsets (8192 samples). According the procedure of the proposed method in Section II, firstly, FFT is performed on one of the two subsets, then the fundamental, harmonic, inter-modulation distortion and DC components are identified. After that $\{e_n\}$ is obtained by removing the identified fundamental, harmonic, inter-modulation distortion and DC components. Then $\{e_n\}$ is sorted into two equal set $\{e_{Hn}\}$ and $\{e_{Ln}\}$ with length of 4096 according to the identified fundamental's phase. The computed P_{e_H} and P_{e_L} are 4.887862×10^{-6} and 4.245829×10^{-6} respectively. It should be pointed out that the values of P_{e_H} and P_{e_L} are relative to the FS (full scale) of ADC, here FS is equal to 2. As the identified the fundamental's amplitude by FFT is 0.9442, the identified fundamental's frequency is 398.974609 MHz, in the end, using equation (16), the estimated RMS jitter is 0.424 ps.

In order to verify the result obtained by the proposed algorithm, ADI method is implemented on the jitter test by adding a low frequency input signal measurement in our experiment. Here, the input signal is set about 2 MHz. The estimated RMS jitter by ADI method is 0.480 ps, which is close to the result computed by the proposed method. In fact, the estimated RMS jitter by the proposed method is smaller than that of the latter. In the proposed method, the harmonic components are excluded. Therefore, the difference of the two values results from spurious components, which could be inter-modulation distortion components, definitely not be harmonic components. Indeed, if the spurious components are excluded manually in ADI method, the estimated RMS jitter is 0.438 ps, which is more close to the result estimated by the proposed method. The comparative results by different methods are summarized in Table II.

Fig.4 shows the spectrum of commercial 9-bit ADC output when the frequency of input signal is about 399 MHz. From Fig.4 we can see that the output of ADC comprises many significant harmonic and non-harmonic components.

Fig.5 shows the spectrums of e_{Hn} and e_{Ln}. The upper one and the lower one are the spectrums of e_{Hn} and e_{Ln} respectively. From Fig.5 we can see that the average power spectrum density of e_{Hn} is larger than that of e_{Ln}, which validates the previous derivation in Section II.

TABLE II. THE COMPUTED RMS JITTER BY DIFFERENT METHODS

	Number of frequencies	Efficiency	cost	Estimated jitter
ADI method	two	low	high	0.480 ps
ADI method with spurious exclusion	two	low	high	0.438 ps
Proposed method	one	high	low	0.424 ps

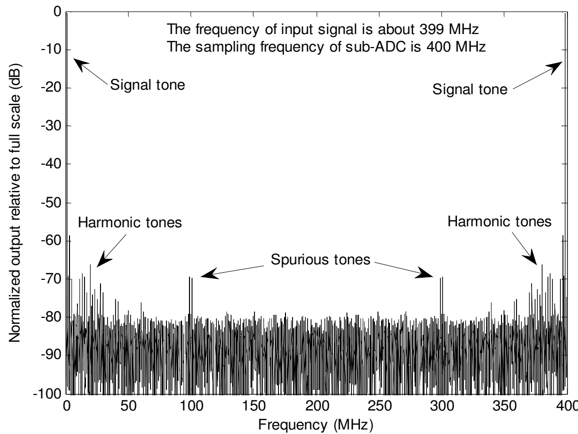

Fig. 4 The spectrum of commercial 9-bit ADC output

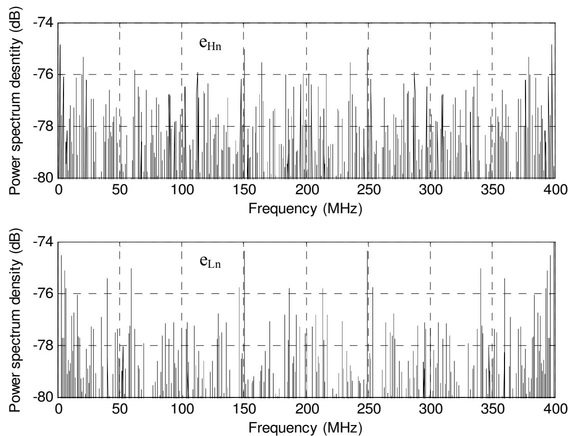

Fig. 5 The spectrums of actual e_{Hn} and e_{Ln}

From the experiment we can see that only a single test with a high frequency input sine wave are performed in the proposed method. Elimination of the need of 2nd low frequency test required in IEEE standard test, TI, and ADI method makes the proposed method saves on both hardware and data acquisition time significantly. Furthermore, the experimental results show that the proposed method is robust to harmonic and non-harmonic distortion, and is more accurate and faster than conventional two frequencies jitter test methods.

V. CONCLUSIONS

In this paper, a simple algorithm for jitter test is developed, justified theoretically, and validated by means of both simulation and experimental results. In particular, the proposed method requires only a single test with a high frequency input sine wave. Compared with IEEE standard method, TI, and ADI method which require another low frequency test, the introduced method saves on both hardware and data acquisition time. Since FFT is performed only once and only some simple time domain computation is involved, the new method is computationally efficient. Robustness to harmonic and non-harmonic distortions is also built into the algorithm. The experimental results have shown that the proposed method is more accurate and faster than the ADI method. Therefore, the presented method is cost-effective and potential to be built on chip.

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