Multi-Threshold Transistors Cell for Low Voltage Temperature Sensing Applications

Sheng-Huang Lee, Chen Zhao, Yen-Ting Wang
Dept. of Electrical and Computer Engineering
Iowa State University
Ames, IA, 50010
alexlsh@iastate.edu, zhaochen@iastate.edu,
yentingw@iastate.edu

Degang Chen, Randall Geiger,
Dept. of Electrical and Computer Engineering
Iowa State University
Ames, IA, 50010
djchen@iastate.edu, rlgeiger@iastate.edu

***Abstract*—A new Low Voltage CMOS temperature sensor with low supply sensitivity is introduced. Though operation over a large temperature range is possible, this structure is particularly useful in power/thermal management applications where a rather narrow temperature band is of most concern. The sensor is based upon a multi-threshold 4 transistors cell and uses the temperature dependence of the threshold voltages to sense temperature. The low headroom requirement of the structure allows for very low voltage operation or practical cascoding at nominal supply voltages to further reduce the supply voltage sensitivity. With proper device sizing, a very linear relationship between output voltage and temperature is achieved. Simulation results show that the temperature linearity is robustness to process variations and the cascoded implementation has excellent insensitivity to the power supply voltage. The circuit has been implemented in a 65nm digital process with multiple threshold voltages devices. Simulation results show a temperature nonlinearity of less than 0.5°C over the temperature range of 100~150°C.**

I. INTRODUCTION

As feature sizes in new CMOS processes continue to decrease and circuit complexities increase, packaging densities and local power densities of many integrated circuits (ICs) are increasing. This increases the temperature either locally or across the die and causes changes in circuit performance. If the temperature becomes too high, the IC will fail and/or lifetime will be degraded. To manage these problems, on-chip power/thermal management that includes continuous on-chip monitoring of temperature at multiple critical locations on a die is becoming commonplace. Low cost, small die area, good accuracy, low power dissipation, and negligible self-heating are key requirements in these integrated temperature sensor arrays. Inherent in these requirements is minimal dependence on variations in the power supply voltage.

There are several methods to build an on-chip temperature sensor. The most tradition and most common approach exploits the temperature-dependent electrical characteristics of the pn-junction to generate a voltage or a current that varies with temperature[1]. Many of those reported consume substantial silicon area and have significant power requirements. Temperature sensors that utilize the temperature dependence of the threshold voltage of MOS transistors have also been discussed in the literature [2][3]. Recently, a time-to-digital-converter based approach to measuring temperature was introduced. Those in this class discussed in [4] utilize the temperature dependence of both the CMOS threshold voltage and mobility to obtain the thermal information. The linearity of the time-to-digital converter based temperature sensor structures that have been reported is modest and the area required for the implementations is substantial.

In previous work [2] by the authors, a highly linear compact on-chip threshold voltage based temperature sensor using the inverse Widlar current mirror was introduced. An implementation of this structure in which a device sizing strategy that reduced 2nd and 3rd order temperature nonlinearity in the temperature transfer characteristics was discussed. Although the structure has low supply voltage sensitivity, it could be improved by increasing the output impedance of the current sources and cascoding the outputs is the most common way of doing this. Unfortunately, in low-voltage processes, there is not enough headroom in this structure for cascoding.

A low-voltage supply-insensitive 4-transistor CMOS threshold-based temperature sensor that relies on the temperature dependence of two NMOS (or PMOS) transistors with different threshold voltages that are native in newer digital processes is presented in this paper. The temperature sensor is implemented in a 65nm digital process with native multiple threshold MOS devices. In contrast to most other threshold-based references and temperature sensors, the 4-transistor sensor has a single stable equilibrium point and thus does not require a start-up circuit. When operating at the nominal supply voltage of 1.2V in a 65nm process, the structure has enough excess voltage headroom for full cascoding. With cascoding, the 8-transistor (excluding biasing transistors) temperature sensor has even better supply insensitivity.

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Architecturally, the 4-transistor dual-threshold cell has been used to realize a low voltage strong-inversion/weak-inversion temperature insensitive current reference [5].

In Section II, the transfer characteristics of the proposed circuit are described. A design example for high temperature sensing application along with simulation results comprises Section III. This work is concluded in Section IV.

II. THRESHOLD VOLTAGE REFERENCE CIRCUIT

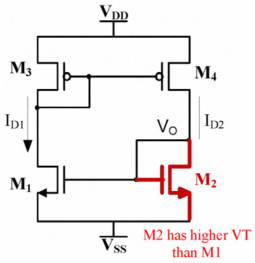


Figure 1. Schematic of proposed dual-V_T temperature sensor circuit

The proposed temperature sensor is shown in Fig. 1. This circuit is made functional by having two different threshold voltages in either the n-channel transistor pair or the p-channel transistor pair. In the following discussion, it will be assumed that the n-channel devices have different threshold voltages.

A. *Circuit Architecture Transfer Characteristics*

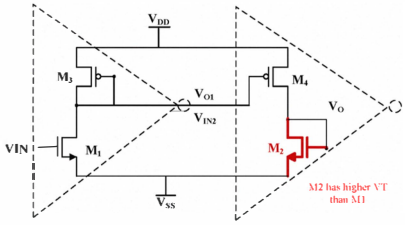


Figure 2. Cascade of n-channel/p-channel input inverters

The circuit in Fig. 1 can be viewed as two cascaded inverters in a loop. In order to determine the stable operating point of the circuit, the loop can be broken at the V_O node, as shown in Fig. 2, and the analytical transfer characteristics of the cascaded inverter pair can be obtained. If the loop is broken between M_3 and M_4, similar transfer characteristics (referenced to V_{DD}) can be observed.

Using the ideal square-law device model and neglecting the output conductance effects, a straightforward analysis of the first inverter stage yields the following analytical expressions in the three possible operation regions:

M_1 cutoff, M_3 saturated

$$V_{O1} = V_{DD} + V_{Tp} \quad \text{for} \quad V_{IN} < V_{Tn1} \tag{1}$$

M_1 saturated, M_3 saturated

$$V_{O1} = -\frac{V_{IN}}{\sqrt{\theta_1}} + V_{DD} + V_{Tp3} + V_{Tn1}\left(\frac{1}{\sqrt{\theta_1}}\right) \quad \text{for} \quad V_{Tn1} + (V_{DD} + V_{Tp3})\left(\frac{\sqrt{\theta_1}}{1+\sqrt{\theta_1}}\right) > V_{IN} > V_{Tn1} \tag{2}$$

M_1 triode, M_3 saturated; V_{O1} satisfies the equation

$$V_{O1}^2\left(\frac{1+\theta_1}{2}\right) + V_{O1}\left(V_{Tn1} - V_{IN} - \theta_1\left[V_{DD} + V_{Tp3}\right]\right) + \left(\frac{\theta_1}{2}\left[V_{DD} + V_{Tp3}\right]^2\right) = 0 \tag{3}$$

$$\text{for} \quad V_{IN} > V_{Tn1} + (V_{DD} + V_{Tp3})\left(\frac{\sqrt{\theta_1}}{1+\sqrt{\theta_1}}\right)$$

Where the parameter θ_1 is defined as

$$\theta_1 = \frac{W_3 L_1}{W_1 L_3}\frac{\mu_p}{\mu_n} \tag{4}$$

Similarly, the second inverter stage with an input $V_{IN2}=V_{O1}$ is governed by the following operation regions:

M_4 cutoff, M_2 saturated

$$V_O = V_{Tn2}, \quad \text{for} \quad V_{IN2} > V_{DD} + V_{Tp4} \tag{5}$$

M_4 saturated, M_2 saturated

$$V_O = -\frac{V_{IN2}}{\sqrt{\theta_2}} + V_{Tn2} + (V_{DD} + V_{Tp4})\left(\frac{1}{\sqrt{\theta_2}}\right) \tag{6}$$

$$\text{for} \quad V_{DD} + V_{Tp4} > V_{IN2} > V_{Tp4} + V_{Tn2}\left(\frac{\sqrt{\theta_2}}{1+\sqrt{\theta_2}}\right) + V_{DD}\left(\frac{1}{1+\sqrt{\theta_2}}\right)$$

M_4 triode, M_2 saturated; V_O satisfies the equation

$$V_O^2(1+\theta_2) + V_O\left(-2\theta_2 V_{Tn2} - 2V_{IN2} + 2V_{Tp4}\right) + \left(-2V_{DD}\left[\frac{V_{DD}}{2} - V_{IN2} + V_{Tp4}\right] + \theta_2 V_{Tn2}^2\right) = 0$$

$$\text{for} \quad V_{IN2} < V_{Tp4} + V_{Tn2}\left(\frac{\sqrt{\theta_2}}{1+\sqrt{\theta_2}}\right) + V_{DD}\left(\frac{1}{1+\sqrt{\theta_2}}\right)V_{DD} \tag{7}$$

where the parameter θ_2 is defined as

$$\theta_2 = \frac{W_2 L_4}{W_4 L_2}\frac{\mu_n}{\mu_p} \tag{8}$$

The loop gain, A_{VL}, of the cascaded inverter pair is the product of the small signal voltage gain of each stage. When all transistors are operating in saturation, it is given by:

$$A_{VL} = A_{V13} \cdot A_{V42} \tag{9}$$

where

$$A_{V13} = \frac{g_{m1}}{g_{m3}} = \sqrt{\frac{W_1 L_3}{W_3 L_1}\cdot\frac{\mu_n}{\mu_p}} \tag{10}$$

$$A_{V42} = \frac{g_{m4}}{g_{m2}} = \sqrt{\frac{W_4 L_2}{W_2 L_4}\cdot\frac{\mu_p}{\mu_n}} \tag{11}$$

The operating point of the two inverter loop is at the intersection of the transfer characteristics of the two inverters and the unity slope line defined by $V_O=V_{IN}$. If more than one intersection occurs, a start-up circuit is needed to select a single stable equilibrium point. To maintain a low sensitivity to the supply voltage in this circuit, it is necessary that all transistors are operating in the saturation region. The transfer characteristics of the inverter pair will now be considered under two scenarios; when the n-channel transistors are the same and when they are different.

B. *Single Threshold Voltage*

In the first scenario, assume that the threshold voltage of the n-channel input transistor of the first inverter, V_{Tn1} to be equal to the n-channel load transistor of the second inverter, V_{Tn2}. The threshold voltages for both p-channel transistors are also assumed to be equal to each other. Fig. 3(a) shows the resulting transfer characteristics under different sizing conditions. For a saturation region loop gain of less than 1, the transfer curve only intersects with the unity loop gain locus at V_{IN} equals to V_{Tn}, which is not a viable operating point because the transistors are operating in the weak-inversion or cutoff region. For loop gain of more than 1, the transfer curve intersects at 2 points; one when the transistors

are cutoff and the other when one of the transistors is in the triode region. The latter intersection is not a viable operating point because one of the transistors is operating in the triode region which will not provide the required low sensitivity to V_{DD}.

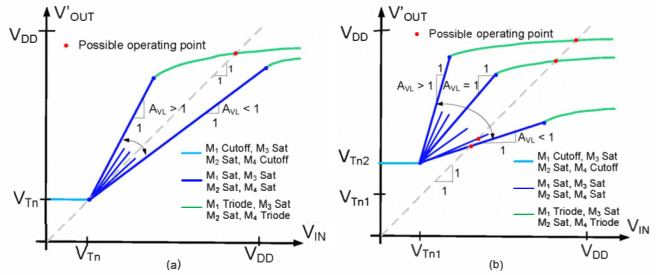


Figure 3. Transfer characteristics of inverter pair with (a) single n-channel threshold voltage, (b) dual n-channel threshold voltage ($V_{Tn1}<V_{Tn2}$)

C. *Dual Threshold Voltage*

In the second scenario, the threshold voltage of the n-channel input transistor of the first inverter, V_{Tn1}, is selected to be less than that of transistor M_2. The threshold voltages for the p-channel transistors are again assumed to be equal to each other. Fig. 3(b) shows the resulting transfer characteristics of the inverting pair with two different n-channel threshold voltages. For a saturation region loop gain that is larger than 1, the transfer curve has a unique intersection point on the unity loop gain curve but at this intersection one or more transistors are operating in triode region. As in the previous scenario, this is not a practical design because the sensitivity to V_{DD} will be large. For a saturation region loop gain that is less than 1, there exists a unique intersection point between with the unity loop gain locus where all transistors are operating in the saturation region. This provides a useful operating point in which the output node voltage is insensitive to V_{DD}. In addition, since there is only one stable equilibrium point in this case, there is no need for a startup circuit to establish the desired operating point.

The threshold voltage difference will be dictated dominantly by what devices are available in a process though bulk bias may also be used advantageously to help manage the threshold differences. In general, small threshold differences will require saturation region gains close to unity resulting in high sensitivities to model and design parameters whereas design constraints will be relaxed if the threshold differences.

D. *Threshold Voltage Referenced Output*

The output voltage for the 4-transistor temperature sensor of Fig. 1 will now be derived. Assuming a square-law model and ignoring output conductance effects, the left and right branches have drain currents given by the expressions :

$$I_{D1} = \frac{\mu_n C_{ox}}{2}\frac{W_1}{L_1}(V_O - V_{Tn1})^2 \quad (12)$$

$$I_{D2} = \frac{\mu_n C_{ox}}{2}\frac{W_2}{L_2}(V_O - V_{Tn2})^2 \quad (13)$$

$$I_{D1} = MI_{D2} \quad (14)$$

where M is the current-mirror gain of the p-channel transistors pair.

Equations (12)–(14) comprise a set of three simultaneous equations with the unknown variables $\{I_{D1}, I_{D2}, \text{and } V_O\}$. V_O can then be solved from these three equations to obtain:

$$V_O = \frac{\sqrt{W_1/L_1}}{\left(\sqrt{W_1/L_1}-\sqrt{MW_2/L_2}\right)}V_{Tn1} - \frac{\sqrt{MW_2/L_2}}{\left(\sqrt{W_1/L_1}-\sqrt{MW_2/L_2}\right)}V_{Tn2} \quad (15)$$

From (15), it can be observed that the output voltage is a weighted linear difference between the threshold voltages V_{Tn1} and V_{Tn2} and is independent of V_{DD}.

The temperature dependent threshold voltage model that is widely used in circuit simulators [7] is given in (16)

$$V_{TH}(T) = V_{TH}(TNOM) + \left(KT1 + \frac{KT1L}{L_{eff}} + KT2\cdot V_{bseff}\right)\cdot\left(\frac{T}{TNOM} - 1\right) \quad (16)$$

where TNOM is the nominal temperature usually set at 300K; KT1, KT1L, and KT2 are process dependent constants; L_{eff} is the effective length, and V_{bseff} is the effective bulk to source voltage. Circuit implementations may result in a weak temperature dependence of V_{bseff} but in the temperature sensor of Fig. 1, all bulks are source connected. Thus, in this circuit, if follows from (15) and (16) that with the simplified square law model, the output voltage is linearly dependent on temperature and thus this circuit serves as a linear temperature sensor. The finite output impedance of the device degrades linearity and introduces a modest V_{DD} sensitivity. Analytical expressions for the effects of output impedance on linearity are unwieldy.

III. Design for High Temperature Sensing Applications

Two temperature sensor circuits (regular and cascode) based upon the 4-transistor cell of Fig. 1 were designed in a 65nm multiple-V_T digital process. The nominal supply voltage in the process is 1.2V. The sensor was designed to operate in the high temperature range between 100°C and 150°C. The nominal temperature was defined to be 125°C. The nonlinear error of the sensor, expressed in °C, is the difference in the measured temperature and the end-point fit line temperature. The temperature integral nonlinearity error (TINL) in °C at the output node of the sensor is defined as

$$TINL = \left[\max_{100°C<T<150°C}\left|V_o(T) - V_{OFIT}(T)\right|\right]\left(\frac{50°C}{V_O(150°C) - V_O(100°C)}\right) \quad (17)$$

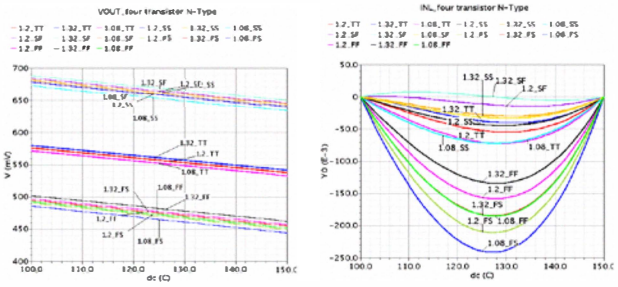
where $V_{OFIT}(T)$ is the output end-point fit line to the two points $V_O(100^\circ C)$ and $V_O(150^\circ C)$.

A. *4-transistors N-Type Temperature Sensor*

Device sizes for the 4-transistor temperature sensor are given in Table 1. Process corner simulations and supply variations were run to predict linearity robustness over process and supply variations compared to typical (TT) operation. Results appear in Fig. 4. Corners are designated as (FF: Fast NMOS Fast PMOS, SS: Slow NMOS Slow PMOS, FS: Fast NMOS Slow PMOS, SF: Slow NMOS Fast PMOS) and ±10% supply variations around nominal V_{DD} of 1.2V as (L=Low, N=Nominal, H=High).

The maximum temperature nonlinearity error at typical conditions is 0.0546°C across the temperature range between 100°C and 150°C and the worst-case maximum temperature

error of 0.241°C occurs at the FS corner with a low supply voltage. The nominal temperature coefficient is -0.771mV/°C.



(a) (b)

Figure 4. Simulated 4T (a) output voltage and (b) temperature error at different process corners and ±10% variation over nominal VDD of 1.2V

At TT, the maximum output variation with ±10% supply voltage variation is 9.182mV. This level of supply variation would cause an additional and much larger temperature error of 11.9°C if VDD varies with time, i.e. noisy supply due to digital switching, temperature dependent supply etc. This is due primarily to the limited output impedance of the sensor.

B. Cascode N-Type Temperature Sensor

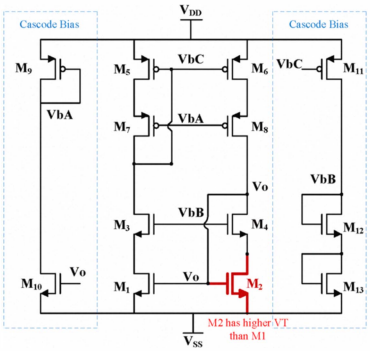
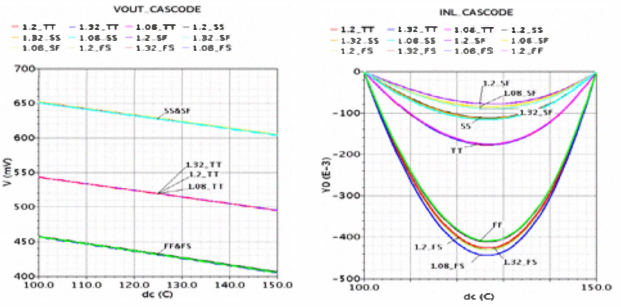


Figure 5. Schematic of cascode temperature sensor with biasing transistors

The circuit of Fig. 1 has enough headroom to allow for complete cascoding. This will significantly reduce the supply voltage sensitivity. A complete schematic of the cascoded n-type temperature sensor including bias generators is shown in Fig. 5.



(a) (b)

Simulated cascode (a) output voltage and (b) temperature error at different process corners and ±10% variation over nominal VDD of 1.2VDevice sizes for an implementation of the cascode temperature sensor are given in Table 1. The cascode circuit was simulated under the same conditions as the 4-transistors circuit and the results are shown in Fig. 6. The maximum temperature error TT is 0.177°C over the temperature range between 100°C and 150°C. The worst-case maximum temperature error of 0.444°C over process and supply variations occurs at the FS corner with a low supply voltage. At TT, the maximum output voltage variation is 313.8µV and this would introduce an additional temperature error of 0.33° C if V_{DD} varies ±10% from its nominal value.

Overall performance of the two temperature sensors is shown in Table 1. It can be seen that the active area is very small and the total power dissipation is very low. These simulation results are based upon the linear temperature dependent model of the threshold voltage that is widely used in many simulators. Some higher-order nonlinearities in the temperature dependence of the threshold voltage do exist and will cause additional degradation in linearity.

IV. CONCLUSIONS

A low-voltage supply-insensitive 4-transistor CMOS threshold-based temperature sensor that relies on the temperature dependence of two NMOS (or PMOS) transistors with different threshold voltages was introduced. A fully cascoded extension of this circuit was presented that has even lower power supply sensitivity. Neither structure requires a start-up circuit. The active area of both structures is small and the power dissipation is also very low. Simulation results suggest that these structures can be used as temperature sensors for power/thermal management.

TABLE I. SUMMARY OF PERFORMANCE

Specification	Performance	
Process	65nm	
Voltage Supply	1.2V	
Temperature Range	100~150°C	
Parameter	**4T**	**Cascode**
Active Area (µm^2)	54	96
Nominal power consumption (µW)	11.02	5.124
Temperature Coefficient (mV/ °C)	-0.771	-0.96
Max. Temp. INL (°C) at Typical	0.0546	0.177
Max. Temp. INL (°C) at Worst Case	0.241	0.444
Supply Sensitivity at Typical (°C)	11.9	0.33
4T sizing (µm): W_1(0.3), W_2(4.8), $W_{3,4}$(1.5), All L(1)		
Cascode sizing (µm): W/L_1(0.15/2.5), W/L_2(3.2/4), W/$L_{3,4}$(0.15/0.3), W/$L_{5,6}$(0.15/0.25), W/$L_{7,8}$(0.75/0.25)		

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