Multi-site On-chip Current Sensor for Electromigration Monitoring

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***Abstract*—An on-chip current measurement method that is suitable for electromigration management is introduced. Rather than inserting a shunt in the current flow path for creating a voltage drop, the voltage drop across existing interconnects is used to determine the current flow. Current is measured with a MOSFET-only sensing circuit that provides 9 bits of resolution with midrange current levels at the threshold where electromigration concerns become relevant. This current sensor can be used for sensing currents in either VDD or VSS busses and is targeted for use in the power power/thermal management units in integrated circuits. Simulation results show the DNL/INL of this sensor is within +0.15/-0.3 LSB. The current sensor is robust to local mismatch. The small area and low power dissipation makes the structure suitable for multiple-site on-chip current measurements.**

I. Introduction

Power consumption and die heating are of major concern in high-density high-speed integrated circuits. The performance of modern IC designs is limited by power consumption and thermal issues. Performance improvements in emerging processes are coming at the architectural level by using multi-core structures along with power management techniques that include combinations of measurement-driven dynamic supply voltage scaling, dynamic clock frequency scaling, and pre-calculated or dynamic task assignments. Direct and continuous measurement of on-chip currents in interconnects at multiple locations on a die for supporting power management and system performance optimization is becoming increasingly common. Traditional off-chip current measurement methods are not practical for continuous-time monitoring of current in critical interconnects that are distributed throughout a chip. The demand for good on-chip current sensors needed to support these applications is growing. Requirements for these on-chip current sensors are not only good accuracy, but also compact area and low power consumption.

Quiescent current test techniques (I_{DDQ}) have proven effective for testing/identifying potential defects in integrated circuits such as shorts or opens between signal and power supply lines [1]. However, the effectiveness of quiescent current testing techniques is being challenged by the growing complexity of circuit designs and by the increasing variability and increasing leakage currents in emerging CMOS processes. Most built-in current sensors (BICS) incorporate a current shunt into the current path to create a voltage that is large enough to practically measure. With this approach, the measured current is the ratio of the shunt voltage to the shunt impedance. Unfortunately, the current shunt permanently degrades the performance of the circuit under test (CUT) by introducing a voltage drop and by dissipating power. The BICS in [2] are claimed to incur no performance degradation since they do not require a current shunt but rather measure the very small voltage drop along a segment of the power supply line of the CUT.

Reliability of semiconductor chips is of growing concern with electromigration failure being one of the most persistent and important contributors to reliability degradation. This effect is particularly important in applications where tradeoffs must be made between interconnect area and interconnect current density. However, electrically-induced stress, such as that due to current densities in interconnects that approach the electromigration critical level, I_{CRIT}, is usually not measured because of perceived challenges in building good on-chip current sensors that do not cause excessive voltage drops, require excessive area, or consume excessive power. It is easy to show that the voltage drop across an interconnect of length L and current density I_{CRIT} is given by $V_{CRIT}=I_{CRIT}L\rho$ where ρ is the resistivity of the interconnect material. This voltage is independent of the thickness or cross-sectional area of the interconnect. In an existing aluminum interconnect of length 100μm, V_{CRIT} is around 10mV and this voltage is large enough to practically measure without adding a current shunt.

A new on-chip current sensing technique which requires no current shunt but rather measures the voltage drop across an existing interconnect is introduced in this paper. The proposed technique is a MOSFET only non-intrusive method that supports power/thermal management circuits and can provide real-time current levels useful for electromigration management. This low power current sensor has good accuracy, small area, and is suitable for multi-site current monitoring in multi-core systems.

A transistor level implementation of the current sensor is presented in Section II. The dynamic comparator and noise

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performance is discussed in Section III. The use of the current sensor for electromigration management is described in Section IV. Section V is comprised of simulation results for a circuit designed in a TSMC 0.18µm CMOS process. The paper is concluded with a summary in Section VI.

II. CIRCUIT ARCHITECTURE

The transistor level implementation for the proposed current measurement strategy is illustrated in Figure.1. For electromigration-safe operation of aluminum at 125℃, the average DC voltage drop must be less than approximately 0.1mV/µm. This is independent of the thickness of the interconnect or the width of the interconnect. Sensing IR in an interconnect of length of 100µm requires no "shunt" for measuring current with a voltage drop of 10mV occurring near the electromigration threshold. In order to make on-chip real-time current measurement at a modest accuracy level, this current sensor is designed with 9 bit resolution over a range from 25% to 200% of the electromigration threshold, which could provide sufficient information to support the power/thermal management system. The distributed I· R voltage drop due to current flowing through parasitic metal resistance will be detected, amplified, and converted to digital codes. It has the advantage of converting that current into voltage in a linear way that inherently follows Ohm's law.

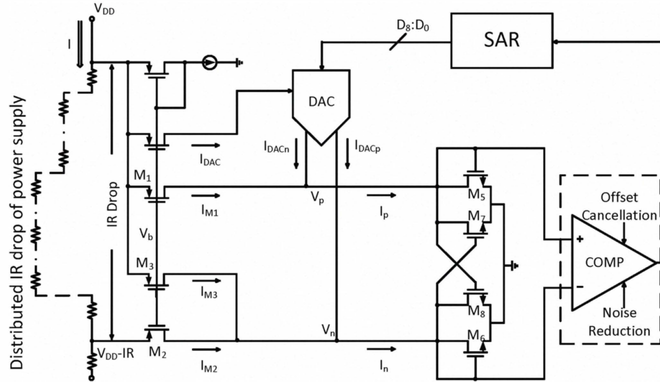

Figure 1. Schematic of proposed current measurement circuitry

The resistors in the figure represent the metal interconnect resistance carrying a critical current to be measured. As the current flows through this metal wire, an IR drop will be created between two locations that are separated by a known distance. To amplify this small signal to a manageable level, an open-loop common gate PMOS amplifier comprised of M_1-M_2 is used. The gate voltage of the amplifier will be biased at a constant voltage V_b. Hence, the voltage drop across the metal wire will serve as a small signal input to the gain stage. The amplifier has diode-connected NMOS devices M_5-M_6 with positive feedback pair M_7-M_8 as the load to enhance the small signal voltage gain. The V_p and V_n nodes in the schematic are self-biased through the diode connected devices. The small signal gain can be expressed as $g_{m1}/(g_{m5} - g_{m7})$. Under normal operation, the currents flowing through the two sides are less than 100µA which is relatively small compared with typical power supply currents that are typically several amps. With the gain stage, the full-scale output signal going into the comparator will be in the hundreds millivolt range near the electromigration limit which greatly relaxes the resolution requirement for the comparator.

For the purpose of reducing circuit complexity and silicon area, the successive approximation register (SAR) based method is used in our structure. To further reduce area, the main DAC in the design is a MOSFET-only R-2R ladder [3]. Sizing of the DAC is based on matching requirements. The output currents of the DAC will balance the current difference between the two drain currents in the common gate input pair. Offset cancellation and noise reduction techniques is applied on comparator and SAR logic is driven by the averaged output of comparator. A binary search is used to equate V_p and V_n or equivalently to equate I_p and I_n. When this happens, we obtain the relationship

$$I_{DAC_p} + I_{M_2} + I_{M_3} = I_{M_1} + I_{DAC_n} \tag{1}$$

I_{DACp} and I_{DACn} can be expressed as

$$I_{DAC_p} = \frac{D}{2^n} I_{DAC} \qquad I_{DAC_n} = I_{DAC} - \frac{D}{2^n} I_{DAC}. \tag{2}$$

where I_{DAC} is the DAC reference current and where D is the decimal equivalent of the 9-bit binary word D8:D0. Assuming that all PMOS transistors have the same threshold voltage and neglecting channel length modulation,

$$I_1 = \frac{\mu_p C_{OX}}{2} \frac{W_1}{L_1} (V_{DD} - V_b - V_{TH})^2 \tag{3}$$

and $$I_2 = \frac{\mu_p C_{OX}}{2} \frac{W_2}{L_2} (V_{DD} - I \cdot R - V_b - V_{TH})^2, \tag{4}$$

where V_b is a fixed dc bias voltage, R is the metal resistance and I is the current that is to be measured.

Assuming that $(W/L)_1 = (W/L)_2$ and substituting (2)-(4) into (1) we obtain,

$$\left(\frac{2D}{2^n} - 1\right) I_{DAC} + I_{M_3} = \frac{\mu_p C_{OX}}{2} \left(\frac{W}{L}\right)_{1,2} IR(2V_{DD} - 2V_b - 2V_{TH} - IR). \tag{5}$$

For a nominal IR drop of 10mV at the electromigration limit, $V_{DD} - V_b - V_{TH} >> IR/2$. (6)

It can be observed from the circuit in Fig. 1 that

$$I_{M_3} = I_{DAC} \approx \frac{\mu_p C_{OX}}{2} \frac{W_3}{L_3} (V_{DD} - V_b - V_{TH})^2 \tag{7}$$

Substituting (5)-(7), Then the IR drop can be expressed as

$$IR = \frac{D}{2^n} \frac{(W/L)_3}{(W/L)_{1,2}} (V_{DD} - V_b - V_{TH}) = \frac{D}{2^n} V_{ref}, \tag{8}$$

where $$V_{ref} = \frac{(W/L)_3}{(W/L)_{1,2}} (V_{DD} - V_b - V_{TH}). \tag{9}$$

As (8) demonstrates, the IR drop is proportional to the digital word. The full scale reference voltage, V_{ref}, can be set by adjusting the size ratio of M_3 and $M_{1,2}$. For current measurement, certain bandgap current sources will be first applied to the power supply line for resistance calibration.

After calibration, the relationship between *IR* voltage drop and actual power supply current will be known. Then real-time current measurement data can be obtained and used to improve the effectiveness of overall power and thermal management algorithms.

III. COMPARATOR OFFSET CANCELLATION AND NOISE REDUCTION TECHNIQUES

The dynamic comparator is a critical component in this system. To reduce the offset voltage and settling time of the compartor, a preamp is used at the input of the comparator. This preamp stage has good common mode rejection. The complete circuit schematic of the comparator is shown in Figure.2. The input differential pair M_1- M_2 pair and the latch pair M_{11}- M_{12} are both sharing the cross-coupled load M_5- M_6. In the reset mode, Clk is high, the input pair is enabled, and M_7- M_8 are off, preventing M_{11}- M_{12} from latch-up. At the same time, the reset of the latch is completed through two NMOS devices M_{13}- M_{14} connecting the output to ground. In latch mode, Clk goes low, disabling the input pair, turning off M_{13}- M_{14}. The positive feedback regenerates the analog signal into a full-scale digital signal.

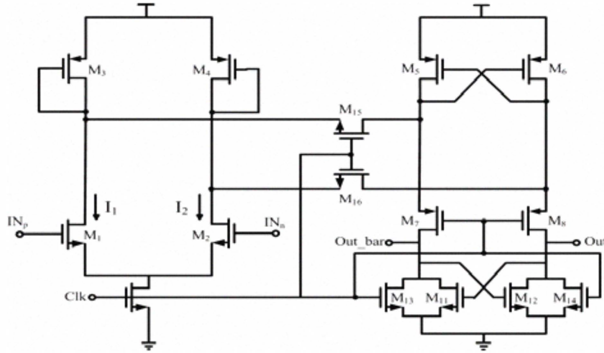

Figure 2. Comparator Circuit Schematic

The accuracy of a current sensor relies heavily on the performance of the comparator because any input signal that is smaller than the input offset will not generate a correct decision to drive the SAR logic. The dynamic comparator is vulnerable to device mismatch. Therefore, the comparator offset needs to be limited to less than 0.5LSB before the SAR conversion begins. The input referred offset of the comparator is dominated by the offset voltage of the preamp.

When some mismatch occurs, there is a difference voltage between the input pair. Then the circuit will lose its balance. In order to correct this mismatch, a successive approximation based offset cancellation method was implemented to control the input differential pair's current as shown in Figure. 3. Driven by SAR logic, the offset DAC successively generates compensation current. In the offset cancelling phase, two inputs are connected together. Without offset, there is randomly 'high' or 'low' at the out node if two inputs are equal. On the contrary, the output won't change until the input difference reaches the offset voltage. Therefore, the count and binary search process injects appropriate compensation current into the differential pair to get approximately 50% 'high' and 50% 'low' at the output while taking a certain amount of time for the comparison. With this approach, the offset will be cancelled out if the output of the comparator provides a random decision. This offset cancellation technique is only enabled when the preamp is on. It does not insert any compensation current into the latch stage so does not affect the latch operation in the latch mode. If multiple current sensors are implemented, the SAR logic used for offset cancellation can be shared between the sensors.

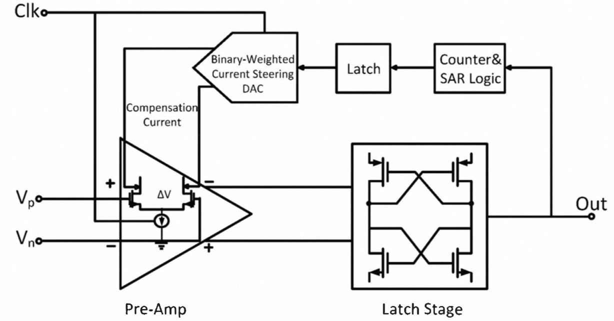

Figure 3. Offset cancellation technique

The comparator also incorporates the chopping technique for noise reduction. Since the current sensor will be operating relatively slowly, the 1/f noise is expected to dominate the noise performance. The differential input pair should have relative large size to minimize 1/f noise effects.

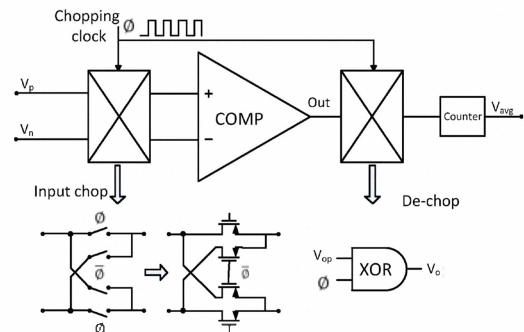

Figure 4. Chopping technique to reduce 1/f noise

As shown in Figure. 4, two inputs of the comparator swap four times during each comparison cycle. The swapping causes the comparator to ideally make complementary decisions. In the time domain, the difference between two nodes should lead to opposite results after comparison. However, the noise should have approximately the same contribution during each cycle. If the accumulated output is averaged, the noise contribution should be reduced.

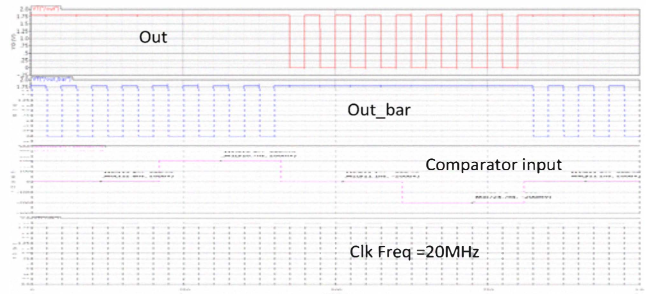

Figure 5. Comparator Transient simulation waveform

Figure. 5 shows the transient simulation waveform of the comparator. At a reset frequency of 20MHz, the comparator is able to resolve a minimum input voltage of ~200µV after offset cancellation.

IV. ELECTROMIGRATION MONITERING

In multi-core circuit systems, computation tasks/loads are typically distributed by a controller. During regular operation, some cores are operating at maximum capacity while others are either handling moderate loads or idling. High-load cores are typically pushed to the limit where the core temperature and current density can be high and stress the die. Hence, it is important to sense the health of the cores and balance the load via an effective power management system. This current sensor has been designed to measure currents that are in the vicinity of the electromigration threshold.

During normal operation, some "wear" will occur whenever the current approaches or exceeds the electromigration threshold. The accumulative "wear" can be assessed by creating a time-history of the current. Electromigration monitoring for the purpose of assessing and managing "wear" will require many current measurements over long times that may be measured in months or even years.

V. SIMULATION RESULTS

This current sensor was designed in a 0.18µm CMOS process with a 1.8V power supply voltage. An IR drop ramp from 0 to 20mV was applied to simulate the static linearity. The simulation was performed with a system clock rate of 8MHz, which are equivalent to a sampling rate of 100KS/s. At this sampling rate, 6000 samples were collected.

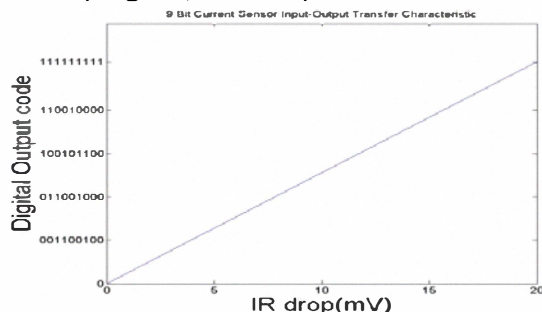

Figure 6. Input-output transfer characteristic of current sensor

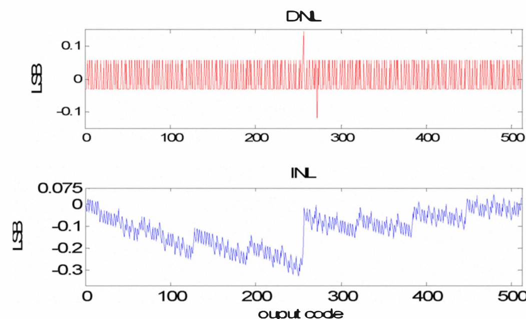

Figure 7. DNL&INL

Simulation results are shown in Figure 6. The response is monotonic. The simulated DNL and INL performance are shown in Figure7. The DNL magnitude is bounded by 0.15LSB and the INL magnitude is bounded by by 0.3LSB. The maximum DNL/INL is shown in Table I.

TABLE I. SUMMARY OF PERFORMANCE

Parameters	Values
Process	1P6M 0.18 µm
Power Supply	1.8V
Power Disspiation	131.4µW
Sampling Frequency	100KHz
INL	+0.05/-0.3 LSB
DNL	+0.15/-0.12 LSB

VI. CONCLUSIONS

In this paper, a new on-chip current sensing technique which provides current measurements near the electromigration threshold has been presented. The proposed technique is a MOSFET only non-intrusive measurement approach which requires a small silicon area and low power. Simulation results show this circuit has good linearity with DNL/INL within +0.15/-0.3 LSB. This structure is suitable for multi- site on-chip current measurement needed to support the power/thermal management of large integrated circuits.

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