ADC Integral Non-Linearity Testing with Low Linearity Monotonic Signals

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***Abstract* — Methods to test the Integral Non-Linearity (INL) of Analog-to-Digital Converters (ADCs) using any monotonic signal with low linearity are proposed. Two methods that estimate the INL of the ADC by removing the error due to non-linearity in the stimulus are described. Signals with linearity dramatically lesser than the ADC under test, can be used to accurately estimate the INL of the ADC. Simulation results show that the maximum INL estimation error for testing 14-bit ADCs using 36 dB pure sinusoids and 7-bit linear exponential signals is under 0.6 LSB.**

***Keywords* — Integral non-linearity (INL), differential non-linearity (DNL), stimulus error identification and removal (SEIR), stimulus error removal (SER)**

I. INTRODUCTION

Quasi-static testing of Analog to Digital Converters (ADCs) is done using the "histogram method" [1]. This method requires the stimulus signal to be 3 or 4 bits more linear, or spectrally more pure than the ADC under test. For high resolution ADCs, generating such accurate signals is very challenging. The procedure is carried out on expensive equipment called Automated Test Equipment (ATE) which houses high resolution signal generators. The expensive ATEs are one of the chief contributors to the test cost. A test procedure that can employ low cost test equipment can provide significant savings on the test cost.

Built in self-test (BIST) solutions to quasi-static testing is another application where low cost testing resources are desired. Stringent requirements are imposed on signal generators. The signal generators are required to be on-chip with small area and power overhead.

Recent works have proposed alternate approaches to carrying out ADC's INL testing. The authors in [6] propose using low linearity ramps to estimate the INL of high resolution ADCs. In [7]-[8] using low spectral purity sinusoids have been proposed. In [9] low precision Dynamical Element Matching Digital-to-Analog Converters are used to test the INL of high resolution ADCs. In [10] low spectral purity sinusoids are used to carry out spectral testing of high resolution ADCs. In [11] authors propose using simple circuitry to generate exponential signals to test the INL and DNL of high resolution ADCs. The inexpensive signal generators make the above approaches well suited not only for on-chip implementations but also in production testing to be used instead of expensive signal generators.

In this work we propose algorithms that can use any monotonic signal with linearity much lesser than the ADC under test to estimate the INL. The paper is organized as follows. In section II, INL testing with monotonic signals with a known Probability Density Function (PDF) is discussed. In section III testing with monotonic signals with low linearity is discussed. Two methods to identify and remove the input non-linearity are described. In section IV we demonstrate the working of the proposed methods for low linearity exponential signals and low spectral purity sinusoids using MATLAB simulations. We conclude the paper in section V.

II. INL TESTING WITH LINEAR SIGNALS

A. Probability Density Function of Commonly Used Signals

Histogram based test algorithms conventionally use a highly linear ramp or a spectrally pure sine wave. The PDF of the input signal is assumed to be known. In the test procedure a large number of samples of the input signal are collected using the ADC under test. A pure sine wave can be represented as:

$$y = A.\sin(\omega t) + B \tag{1}$$

Either random sampling or non-coherent sampling can be used to collect the samples. Assuming a very high resolution ideal ADC, the resulting voltage distribution can be described by:

$$y = A.\sin(x) + B \tag{2}$$

The random variable, 'x', can be treated as though it is uniformly distributed in the interval $[-\pi/2, \pi/2]$:

$$x \sim Uniform[\frac{-\pi}{2}, \frac{\pi}{2}] \tag{3}$$

From (2) and (3), the well-known PDF of the variable of interest, 'y', can be derived using 2.18 in [2] as:

$$f_Y(y) = \begin{cases} \frac{1}{\pi}.\frac{1}{\sqrt{A^2-(y-B)^2}} & \text{-A+B} \le y \le A+B \\ 0 & \text{otherwise} \end{cases} \tag{4}$$

Using the same analogy as in (2) and (3) an ideal ramp can represented as:

$$y = x: \quad x \sim Uniform[x_1, x_2] \tag{5}$$

The PDF of the linear ramp signal can be derived as:

$$f_Y(y) = \begin{cases} \dfrac{1}{x_2 - x_1} & x_1 \le y \le x_2 \\ 0 & otherwise \end{cases} \tag{6}$$

Using the analogy as in as in (2) and (3) an exponential signal can be represented as:

$$y = D - C.\exp(-\frac{x}{\tau}): \ x \sim Uniform[x_1, x_2] \tag{7}$$

The PDF of the exponential signal can be derived as:

$$f_Y(y) = \begin{cases} \dfrac{\tau}{x_2 - x_1}.\dfrac{1}{(D-y)} & y_1 \le y \le y_2 \\ 0 & \text{otherwise} \end{cases} \tag{8}$$

where,

$$y_1 = D - C.\exp(-\frac{x_1}{\tau}), y_2 = D - C.\exp(-\frac{x_2}{\tau}) \tag{9}$$

In general, for any signal g(x) that is a monotone, the variable 'x' can be expressed as a uniform variable over a range $[x_1, x_2]$.The PDF of the signal y=g(x) can then be obtained using Theorem 2.18 in [2].For the ADC INL test procedure, the interval $[x_1, x_2]$ is chosen such that all the codes of the ADC are hit.

B. Estimating the INL of the ADC

With the PDF of the stimulus well defined the ADC's INL can be tested as described in [1] and [2] - [4] .The following notations will be used in the paper.

ADC Input range normalized: (0, 1)
n: Resolution of the ADC under test
N: 2^n , number of distinct output codes
T_k: k^{th} transition level between code *k-1* and *k* of the ADC
Ns: Total number of samples collected
V_k : Cumulative histogram count associated with T_k where

$$V_k = \frac{\sum_{i=0}^{k-1} H_i}{Ns}, k = 1,2,3...N-1 \tag{10}$$

H_i: Total number of samples received in code *i*, *i=0, 1, 2…N-1*
$\hat{INL}_k$: Integral non-linearity of transition level T_k

Consider a signal y with PDF $f_Y(y)$.The probability, Q_K, of a measurement $y<T_K$ is:

$$Q_K = P(y < T_K) = \int_{-\infty}^{T_K} f_Y(y).dy \tag{11}$$

Q_K can be estimated using the cumulative histogram count;

$$V_k \approx \int_{-\infty}^{T_K} f_Y(y).dy \tag{12}$$

From the above expression an estimate of the transition level, T_K can be obtained. For the pure sine wave described in (2)-(4) we have the well-known expression:

$$\hat{T}_K = -A\cos(\pi.V_k) + C \tag{13}$$

For the linear ramp described in (5) and (6) we have:

$$\hat{T}_K = V_K \tag{14}$$

For the exponential signal described in (7) - (9) we have:

$$\hat{T}_K = D + (y_1 - D).\exp[-(x_2 - x_1).V_k / \tau] \tag{15}$$

The INL based on end point fit line is estimated using the formula:

$$\hat{INL}_k = \frac{\hat{T}_k - \hat{T}_1}{\hat{T}_{N-1} - \hat{T}_1}.(N-2) - k, \text{k=2,3,...,N-2} \tag{16}$$

The overall INL is given by:

$$\hat{INL} = \max(\left|\hat{INL}_k\right|) \tag{17}$$

III. TESTING WITH NON-LINEAR SIGNALS

Real world signals have some amount of non-linearity in them which alters the distribution of the input signal. This results in errors in the transition level estimates expression described in (13)-(15). This error can be identified by using functionally related excitations (FRE) - based ADC INL testing algorithms [6]-[9]. In this work we use two non-linear signals, one being the voltage shifted version of the other to excite an ADC. The functional relationship here is a simple voltage shift. The algorithms that are developed are based on the FRE approaches described in [6] - [7].

A. Stimulus Error Identification and Removal (SEIR) algorithm:

The error in transition level estimate due to the non-linearity in the input signal can be approximated using orthogonal basis functions. The transition level estimates can

be estimated by removing the non-linearity error.

$$T_k = \hat{T}_k + \sum_{j=1}^{M} a_j F_j\left(\hat{T}_k\right) + \varepsilon \tag{18}$$

where,

$\hat{T}_k$: Transition level estimates with stimulus error

a_j: Co-efficient of the j^{th} basis function $F_j(t)$

ε: Error due to finite number of samples collected and finite accuracy basis expansion

Since the ADC range is normalized the transition levels are in the range (0, 1).Over this interval sinusoidal basis functions or shifted Legendre's polynomial basis functions can approximate the errors due to non-linearity. Two estimates of the transition levels are obtained for the two non-linear signals.

$$T_k^{(1)} = \hat{T}_k^{(1)} + \sum_{j=1}^{M} a_j F_j\left(\hat{T}_k^{(1)}\right) + \varepsilon \tag{19}$$

$$T_k^{(2)} = \hat{T}_k^{(2)} + \sum_{j=1}^{M} a_j F_j\left(\hat{T}_k^{(2)}\right) - \alpha + \varepsilon \tag{20}$$

α is the constant voltage shift between the excitations. A Least Squares method can then be used to estimate all the basis function coefficients and the voltage shift, α.

$$\{\hat{a}_j, \hat{\alpha}\} = \arg\min\{\sum_{k=1}^{N-1}[\hat{T}_k^{(2)} - \hat{T}_k^{(1)} + \sum_{j=1}^{M} a_j[F_j(\hat{T}_k^{(1)}) - F_j(\hat{T}_k^{(2)})] + \alpha]^2\} \tag{21}$$

With the basis functions' coefficients and voltage shift estimated, (19) or (20) can be used to identify the transition levels from which the INL can be estimated using (16)-(17).

B. Stimulus Error Removal (SER) algorithm:

This algorithm uses two estimates of transition levels obtained using (12) for the two non-linear signals to extract equivalent histogram vectors, $\hat{H}_j$ s. These vectors are used in algorithm described in [7] to obtain estimates of ADC's INL and DNL. The algorithm is described below:

Cumulative histogram vectors, $C_k^{(1)}$ and $C_k^{(2)}$, are calculated using the following expression:

$$\begin{aligned} C_{k-1}^{(1)} &= Ns.\hat{T}_k^{(1)} \\ C_{k-1}^{(2)} &= Ns.\hat{T}_k^{(2)}, k = 1,2,3...N-1 \end{aligned} \tag{22}$$

Equivalent histogram vectors, $\hat{H}_j^{(1)}$ and $\hat{H}_j^{(2)}$, are calculated from the cumulative histogram vectors using the recursive relation:

$$\begin{aligned} \hat{H}_j^{(1)} &= C_j^{(1)} - C_{j-1}^{(1)} \\ \hat{H}_j^{(2)} &= C_j^{(2)} - C_{j-1}^{(2)}, j = 1,2,3...N-2 \end{aligned} \tag{23}$$

The first elements are initialized as:

$$\hat{H}_0^{(1)} = C_0^{(1)}, \hat{H}_0^{(2)} = C_0^{(2)}$$

With the above information, the algorithm for low-linearity ramp signals, [7], can be directly used to accurately estimate the INL of the ADC under test. The code-width of the ADC is defined as:

$$cw_i = \frac{H_i^S}{H_i^{IDEAL}}, i = 1,2,3..N-2 \tag{24}$$

where,

$$H_i^S = \frac{\hat{H}_i^{(1)} + \hat{H}_i^{(2)}}{2} \tag{25}$$

$$H_i^{IDEAL} = \sum_{j=0}^{i-1} \frac{\hat{H}_j^{(2)} - \hat{H}_j^{(1)}}{\hat{\alpha}} + \frac{\hat{H}_i^{(2)} - \hat{H}_i^{(1)}}{2} \tag{26}$$

where, $\hat{\alpha}$ is the estimated voltage shift given by:

$$\hat{\alpha} = \frac{N-2}{\sum_{i=1}^{N-2} \frac{H_i^S}{\sum_{j=0}^{i-1} \hat{H}_j^{(2)} - \hat{H}_j^{(1)} + \frac{\hat{H}_i^{(2)} - \hat{H}_i^{(1)}}{2}}} \tag{27}$$

From the code widths cw_i , the INL of the ADC can be calculated using the expressions:

$$\begin{aligned} DNL_i &= cw_i - 1, i = 1,2,3...N-1 \\ INL_i &= \sum_{j=1}^{i} DNL_j \end{aligned} \tag{28}$$

The methods described in Section *III.A* and *III.B* can be extended to any monotonic signal with low linearity. The functional form of the low linearity signal is known beforehand but the non-linearity present in it is not known. Assuming the non-linearity in the signal is zero the approach proposed in Section II can be used to obtain an estimate of the transition level T_K. The errors due to the nonlinear component can then be modeled as in (18) and the SEIR algorithm can used to estimate the INL. Alternatively, the approach proposed in SER algorithm can be used to estimate the INL.

IV. Simulation Results

Simulations in MATLAB have been carried out to verify the working of the two proposed algorithms. Transition levels of a 14-bit ADC are characterized using a resistor string representation. The transition level errors of the ADCs are generated randomly (Gaussian distribution). The INL of the ADCs is calculated to be around 4 LSBs as shown in Fig 3 and Fig.4. Gaussian distributed input additive noise with a standard deviation of 0.5 LSBs is included to simulate ADC's device noise. The proposed algorithms are then used to estimate the INL of the ADC using low linearity exponential

stimuli and imprecise sinusoids. The reader is directed to [6] and [7] for results on ramp signals.

A. Low Linearity Exponential Signals

The input signal is modeled as shown in (7).A non-linearity as shown in Fig.1 is added to the input. The signal is now 7-bit linear. A voltage shift of 200 LSBs is used to create two versions of the signal. The two signals are sampled in time to collect a total of 262144 samples per signal.36 Sinusoidal basis functions are used to characterize the non-linearity in the input by the SEIR algorithm. The true INL and the estimation error using SEIR and SER algorithm are as shown in Figure 2.

B. Imprecise Sinusoids

Sinusoids with randomly generated harmonic distortion components are used as a stimulus. The FFT spectrum of the stimulus used is shown in Fig.3.The Total Harmonic Distortion of the signal is around 36 dB. A voltage offset of 200 LSBs is used to obtain two versions of the imprecise sinusoid. 36 sinusoidal basis functions are used in the SEIR algorithm to characterize the nonlinearities. A total of 262144 samples of the input are collected over the entire ADC range for each of the sinusoids. The true INL and the estimation error using SEIR and SER algorithm are as shown in Fig. 4.

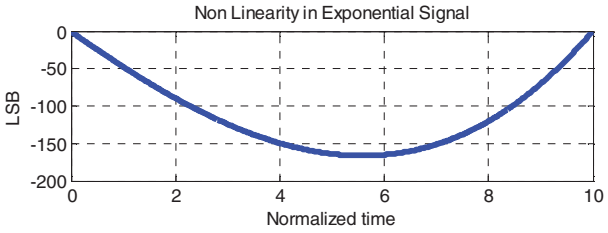

Figure 1.Non Linearity in Exponential Signal

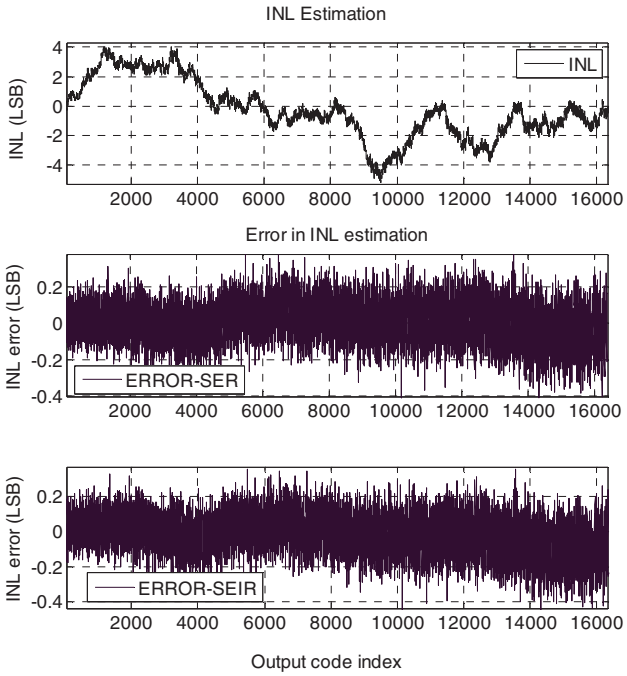

Figure 2.INL Estimation with low linearity exponential signals

C. Results Discussion

From Fig.2 we see that the FRE-based methods accurately estimate the INL of the 14-bit ADC with a maximum INL estimation error of around 0.4 LSB for both the SEIR method and the SER method. In Fig.4 we observe that sinusoid that is only 36 dB pure can be used to estimate the INL of the 14-bit ADC. The maximum INL estimation error for this case is only about 0.6 LSB for the SEIR and SER methods.

The proposed methods are robust to estimation errors in offset voltage and amplitude of the stimulus. In the simulation results for the imprecise sinusoids a coherent data set is used. The algorithm can be modified to handle non-coherent data sets. The most significant aspect of the proposed method is that it is robust to non-linearity errors in the stimulus. The only requirement on the stimulus is that it must contain nonlinearities with low spatial frequency content. The proposed algorithms drastically reduce the requirement on the linearity of the signal. The requirement is replaced with a new

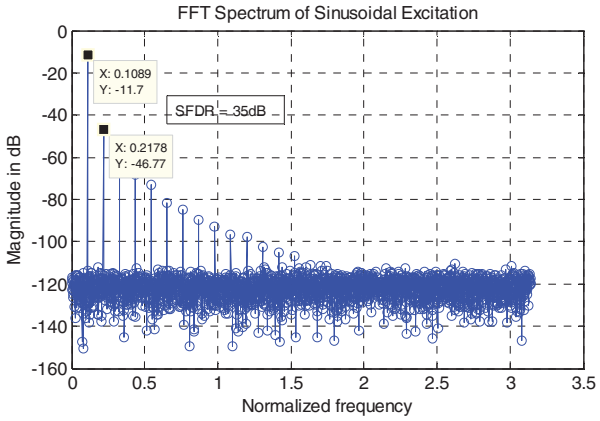

Figure 3.Spectrum of the Imprecise Sinusoidal Excitation

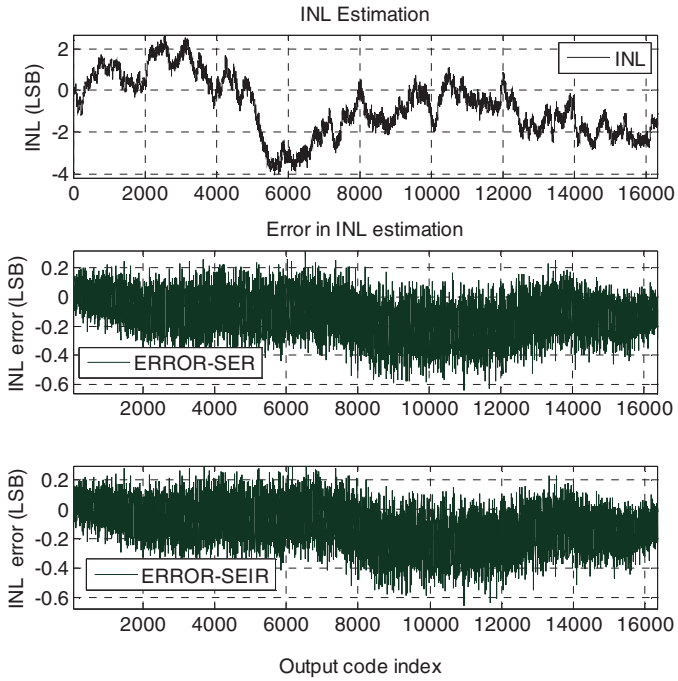

Figure 4.INL Estimation with Imprecise Sinusoids

requirement on the constancy of the offset voltage added to the second signal. This requirement is easy to meet using simple signal generators [14].The effects of environmental non-stationarity can be mitigated using center symmetric interleaving pattern of the signals [15].The results suggest that the any low linearity monotonic signal with linearity around 7-bits can be used to test the INL of 14-bit ADCS with an accuracy of more than 14-bits.This would allow simple signal generators suggested in [12] and [13] to accurately test the INL of 14-bit ADCs.

V. CONCLUSION

In this work we have proposed algorithms that can use any low linearity monotonic signal to test the INL of high resolution ADCs. Unlike the conventional method the methods require very simple signal generators thus offering a cost saving in the hardware resources required for production testing. The methods also lend themselves well to BIST solutions as these simple signal generators can be implemented on–chip with low overhead.

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