A Low Cost Method for Testing Offset and Gain Error for ADC BIST

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Abstract — **As the Systems-on-Chips (SoCs) complexity increases, test cost contributes more in the total cost. Especially, test of deeply embedded analog and mixed signal blocks are the most costly test. Built-In Self-Test (BIST) is considered as a low cost substitution of traditional production test. This paper presents a low cost method for testing ADC's offset and gain error. This is a complement of previous published linearity and spectral performance test methods. The simulation results show the method has good accuracy.**

I. INTRODUCTION

ADCs are indispensable and very important mixed signal blocks in SoCs. Testing of these deeply embedded blocks in SoCs is becoming challenging and expensive. Lack of access to internal analog nodes, difficulty in maintaining signal integrity driving accurate signals on and off chip, and long external testing time are among the reasons. As a result, practical low-cost ADC BIST is regarded as the ultimate alternative to traditional production test.

Significant research results of ADC BIST have been published in literature over the last two decades. BIST schemes of SNR and other frequency specifications testing were presented in [1]-[2]. Precise analog signal is generated on chip and output is analyzed with on chip digital circuitry. A BIST method based on polynomial fitting is presented in [3] for testing static performances such as offset, gain error, and linearity. On chip DAC is required for generating linear ramp stimulus. Another BIST method of testing static performance from exponential input signal is presented in [4]. In [5], static performances are tested by histogram method with sinusoidal stimulus. A sigma-delta modulator is built to generate the sinusoidal stimulus with enough linearity. Most published approaches focus on replicating a production test scheme on chip, which could be very costly and design challenging.

Recently a Stimulus Error Identification and Removal technique is published to test INL with nonlinear ramp signal [6]. This work is presented and validated in standalone production test. However, it makes on chip ADC BIST practical by using ramp signal with low linearity in INL test. Based on this technique, the authors have developed several methods [7-9] to test INL, THD, SFDR, and SNR. All these methods can be implemented on chip with low cost. As the complement, this paper investigates a low cost solution to test offset and gain error based on tested INL values. Additional hardware is only required to generate 3 DC voltages. The measurement accuracy of the method is high enough so that INL measurement accuracy is the limitation.

The rest of the paper is organized as follow. In Section II, the stimulus error identification and removal (SEIR) method is briefly reviewed first. Section III describes the method and analyzes its accuracy from statistically. Section IV provides the simulation validation and Section V concludes the paper.

II. STIMULUS ERROR IDENTIFICATION AND REMOVAL

In pseudo-static linearity test procedure with ideal input ramp signal, each transition level of ADC can be expressed as following.

$$T_i = T_0 + (T_{N-2} - T_0)\cdot t_i \qquad i = 0,1...N-2 \tag{1}$$

In which, T_0 and T_{N-2} are the first and last transition levels of ADC respectively, t_i is the normalized transition time that can be acquired from histogram data [6]. Differences between these tested transition levels and end points fit line transition levels give INLs.

In real test environment, input ramp signal is nonlinear and can be expressed as the sum of an ideal ramp and the nonlinear part.

$$V(t) = T_0 + (T_{N-2} - T_0)\cdot t + \sum_{j=1}^{M} a_j F_j(t) + \varepsilon \tag{2}$$

The nonlinear part is modeled by a set of basis functions $F_j(t)$ and ε is the residual error. If coefficients of all basis functions are known, nonlinearity of input ramp is known.

In SEIR method, two ramp signals with the same nonlinearity are used to test the ADC. The only difference between these two signals is a constant voltage level shift so that $V_2(t)$ equals to $V_1(t)$ - α.

Similar to equation (1), we can get following equations

$$T_i = T_0 + (T_{N-2} - T_0)\cdot t_i^{(1)} + \sum_{j=1}^{M} a_j F_j\left(t_i^{(1)}\right) + \varepsilon \tag{3}$$

$$T_i = T_0 + (T_{N-2} - T_0)\cdot t_i^{(2)} - \alpha + \sum_{j=1}^{M} a_j F_j\left(t_i^{(2)}\right) + \varepsilon \tag{4}$$

These two equations contain non-linearity information of both ADC and input ramp. Remove T_i from (3) and (4), we can solve coefficients of all basis functions by using least square method.

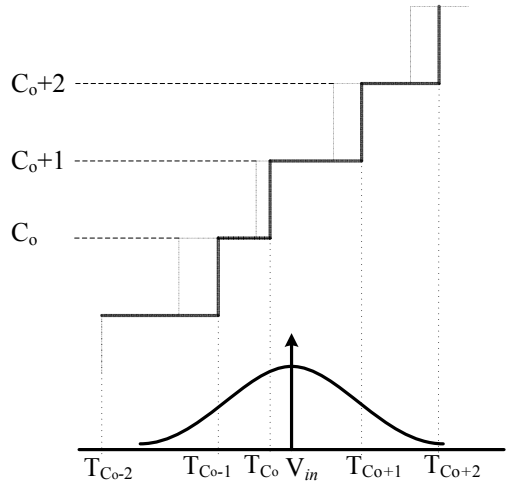

Fig.1. ADC transfer curve and input

$$\{\hat{a}_j s, \hat{\alpha}\} = \arg\min\left\{\sum_{k=0}^{N-2}\left[\hat{t}_{k,1} - \hat{t}_{k,2} + \sum_{j=1}^{M} a_j\left[F_j(\hat{t}_{k,1}) - F_j(\hat{t}_{k,1})\right] + \alpha\right]^2\right\} \quad (5)$$

The set of basis functions represents the nonlinear part of input ramp. The real transition level T_i and INL of ADC can be calculated from (3) or (4).

III. Offset and Gain Error Testing

A. Test method

Histogram based INL testing cannot test code width at two ends or voltage value of each code edge. Binary search or servo method is needed to test offset and gain error in production testing [10]. But neither of these two methods is cost effective and practical for ADC BIST. From cost point of view, estimating offset and gain error from existing resources is attractive. As described in section II, INL of each transition level has been measured. Nonlinearity of the input ramp and voltage level shift α between two ramps has also been identified. In this section, a method of testing offset and gain error based on INL is presented. Offset and gain error is obtained by testing four different unknown input voltages a number of times respectively.

Fig.1 shows a part of ADC transfer curve, gray line is the ideal transfer curve and black line is the real transfer curve. The input voltage V_{in} plus additive noise V_n is plotted below the transfer curve. The additive noise makes the actual input of ADC a normal distributed random variable as shown in the figure. Due to additive noise, the ADC may output different codes around C_o. The probability of output code larger than C_o is

$$P = \frac{1}{2} - \frac{1}{2} erf\left(\frac{T_{Co} - V_{in}}{\sigma\sqrt{2}}\right) \quad (6)$$

in which, T_{Co} is the transition voltage and σ is the standard deviation of noise. Thus the transition voltage can be expressed as

$$T_{Co} = V_{in} + \sqrt{2}\sigma \cdot erf^{-1}(1-2P) \quad (7)$$

On the other hand, transition voltage T_{Co} can also be expressed in terms of INL as following

$$T_{Co} = -V_{ref} + 1\cdot LSB + C_o \cdot LSB + INL_{Co} \cdot LSB + E_{os} \cdot LSB + E_{gCo} \cdot LSB \quad (8)$$

where E_{os} is the offset error, E_{gCo} is the gain error at this transition point, and INL_{Co} is the INL of T_{Co}. From (7) and (8), we have

$$V_{in} + \sqrt{2}\sigma \cdot erf^{-1}(1-2P) = -V_{ref} + 1\cdot LSB + C_o \cdot LSB + INL_{Co} \cdot LSB + E_{os} \cdot LSB + E_{gCo} \cdot LSB \quad (9)$$

In this equation, INL_{Co} is the true INL value of T_{Co}, but we only have the tested value $\hat{INL}_{Co}$, so $\hat{INL}_{Co}$ will be actually used in calculation. In order to obtain the value of P, test the same voltage H_{tot} times. H_c is the number of test that output code is larger than C_o. The probability of output code larger than C_o can be approximately calculated by (10).

$$\hat{P} = \frac{H_c}{H_{tot}} \quad (10)$$

Equation (9) gives the value of offset and gain error in terms of V_{in}, σ. With enough number of equations like (9), we can calculate the values of offset and gain error. By testing four different voltage H_{tot} times respectively, we obtain four equations in (11) at the bottom.

The first equation is obtained from the test that only the voltage offset α is used as the input of ADC and the input voltage is $V_a = -V_{ref} + \alpha \cdot LSB$. There are only two unknowns in this equation. Another equation is introduced by testing an arbitrary input voltage around middle input range V_i. Now we have two equations but three unknowns. Since α is known, if we test input voltage of $V_k = V_i + \alpha \cdot LSB$, another equation will be obtained

$$\hat{T}_{Cj} = V_i + \alpha\cdot LSB + \sqrt{2}\sigma \cdot erf^{-1}(1-2\hat{P}_j) = -V_{ref} + 1\cdot LSB + C_j \cdot LSB + \hat{INL}_{Cj} \cdot LSB + \hat{E}_{os} + \hat{E}_{gCj} \quad (12)$$

From the first two equations of (11) and (12), we can solve offset and gain error, and the gain error is

$$\hat{E}_g \cdot LSB = \frac{2^n - 2}{C_j - C_i} \cdot \left\{\sqrt{2}\sigma \cdot \left[erf^{-1}(1-2\hat{P}_j) - erf^{-1}(1-2\hat{P}_i)\right] + \left(\alpha + C_i - C_j + INL_{Ci} - INL_{Cj}\right)\cdot LSB\right\} \quad (13)$$

Though the gain error has been solved, equation (13) has a problem which is the scale factor after the equator. This factor has large value which will amplify value in the brace including estimation error. To test gain error more accurately, testing a voltage close to V_{ref} is more helpful. Thus the forth equation in (11) is obtained by testing input voltage close to full scale voltage which is $V_b = V_{ref} - \alpha' \cdot LSB$.

$$\begin{cases} \hat{T}_{Ca} = -V_{ref} + \alpha \cdot LSB + \sqrt{2}\sigma \cdot erf^{-1}\left(1-2\hat{P}_a\right) = -V_{ref} + 1 \cdot LSB + \hat{E}_{os} \cdot LSB + C_a \cdot LSB + I\hat{N}L_{Ca} \cdot LSB + \hat{E}_{gCa} \cdot LSB \\ \hat{T}_{Ci} = V_i + \sqrt{2}\sigma \cdot erf^{-1}\left(1-2\hat{P}_i\right) = -V_{ref} + 1 \cdot LSB + C_i \cdot LSB + I\hat{N}L_{Ci} \cdot LSB + \hat{E}_{os} \cdot LSB + \hat{E}_{gCi} \cdot LSB \\ \hat{T}_{Ck} = V_i - \alpha' \cdot LSB + \sqrt{2}\sigma \cdot erf^{-1}\left(1-2\hat{P}_k\right) = -V_{ref} + 1 \cdot LSB + C_k \cdot LSB + I\hat{N}L_{Ck} \cdot LSB + \hat{E}_{os} \cdot LSB + \hat{E}_{gCk} \cdot LSB \\ \hat{T}_{Cb} = V_{ref} - \alpha' \cdot LSB + \sqrt{2}\sigma \cdot erf^{-1}\left(1-2\hat{P}_b\right) = -V_{ref} + 1 \cdot LSB + C_b \cdot LSB + I\hat{N}L_{Cb} \cdot LSB + \hat{E}_{os} \cdot LSB + \hat{E}_{gCb} \cdot LSB \end{cases} \tag{11}$$

$$\hat{E}_g = \frac{2^n-2}{C_b+C_i-C_k-C_a}\Big\{2V_{ref} - (\alpha-1) - \left(C_b+C_i-C_k-C_a+1\right) - \left(I\hat{N}L_{Cb} + I\hat{N}L_{Ci} - I\hat{N}L_{Ck} - I\hat{N}L_{Ca}\right) + \sqrt{2}\sigma\left[erf^{-1}\left(1-2\hat{P}_b\right) + erf^{-1}\left(1-2\hat{P}_i\right) - erf^{-1}\left(1-2\hat{P}_k\right) - erf^{-1}\left(1-2\hat{P}_a\right)\right]\Big\} \tag{9-14}$$

$$\hat{E}_{os} = (\alpha-1) + \sqrt{2}\sigma \cdot erf^{-1}\left(1-2\hat{P}_a\right) - \left(C_a + I\hat{N}L_{Ca}\right) - \frac{C_a}{2^n-2}\hat{E}_g \tag{15}$$

$$\begin{aligned} \Delta E_g = \hat{E}_g - E_g = \frac{2^n-2}{C_b+C_i-C_k-C_a} \cdot \{ & \\ & \sqrt{2}\sigma\left[erf^{-1}\left(1-2\hat{P}_b\right) + erf^{-1}\left(1-2\hat{P}_i\right) - erf^{-1}\left(1-2\hat{P}_k\right) - erf^{-1}\left(1-2\hat{P}_a\right)\right] - \left(I\hat{N}L_{Cb} + I\hat{N}L_{Ci} - I\hat{N}L_{Ck} - I\hat{N}L_{Ca}\right) - \\ & \sqrt{2}\sigma\left[erf^{-1}\left(1-2P_b\right) + erf^{-1}\left(1-2P_i\right) - erf^{-1}\left(1-2P_k\right) - erf^{-1}\left(1-2P_a\right)\right] + \left(INL_{Cb} + INL_{Ci} - INL_{Ck} - INL_{Ca}\right) \ \} \end{aligned} \tag{16}$$

$$E\left(\Delta E_g\right) = \frac{2^n-2}{C_b+C_i-C_k-C_a}\left[\left(INL_{Cb} + INL_{Ci} - INL_{Ck} - INL_{Ca}\right) - \left(I\hat{N}L_{Cb} + I\hat{N}L_{Ci} - I\hat{N}L_{Ck} - I\hat{N}L_{Ca}\right)\right] \tag{17}$$

$$Var\left(\Delta E_g\right) = \left(\frac{2^n-2}{C_b+C_i-C_k-C_a}\right)^2 \cdot 2\sigma^2 \cdot Var\left[erf^{-1}\left(1-2\hat{P}_b\right) + erf^{-1}\left(1-2\hat{P}_i\right) - erf^{-1}\left(1-2\hat{P}_k\right) - erf^{-1}\left(1-2\hat{P}_a\right)\right] \tag{18}$$

The difference between -α' and α is that -α' is down shift while α is up shift. The reason is we only have -V_{ref} + α·LSB at bottom and V_{ref} - α'·LSB at top. But the value of α'·LSB is unknown so we have three equations and four unknowns. The third equation is obtained by testing the voltage V_{in}=V_i - α'·LSB without introducing new unknown. From these four equations, we can solve the gain error and offset as shown in (14) and (15) the unit of which is LSB.

B. Accuracy analysis

Tested value of INL and probability P are different from their real value, which causes estimation error in $\hat{E}_g$ and $\hat{E}_{os}$. The error of estimated gain error is expressed by (16). The expectation value of ΔE_g is expressed by (17). For a certain ADC and tested INL data, the value of E(ΔE_g) is fixed and determined by the accuracy of INL testing. The variance of ΔE_g is expressed by (18). Based on the second order Taylor expansion of error function, we have (19).

$$Var\left[erf^{-1}\left(1-2\hat{P}_i\right)\right] = \pi \cdot \exp\left(\frac{(T_{Ci}-V_i)^2}{\sigma^2}\right) \cdot Var\left(\hat{P}_i\right) \tag{19}$$

Since T_{Ci}-V_i is always in the range of [-0.5LSB, 0.5LSB), we can find the boundary of (19).

$$Var\left[erf^{-1}\left(1-2\hat{P}_i\right)\right] \le \pi \cdot \exp\left(\frac{1}{4\sigma^2}\right) \cdot Var\left(\hat{P}_i\right) \tag{20}$$

Other three terms in the square bracket of (18) have the same form and boundary as (19). The expression of $Var\left(\hat{P}_i\right)$ can be obtained by analyzing a binomial distribution that output code larger or not larger than C_i.

$$Var\left(\hat{P}_i\right) = \frac{1}{4H_{tot}}\left[1 - erf^2\left(\frac{T_{Ci}-V_i}{\sigma\sqrt{2}}\right)\right] \le \frac{1}{4H_{tot}} \tag{21}$$

From (18)-(21), write maximum value of $Var(\Delta E_g)$ as

$$Var\left(\Delta E_g\right) \le \left(\frac{2^n-2}{C_b+C_i-C_k-C_a}\right)^2 \cdot \frac{2\pi\sigma^2}{H_{tot}} \cdot \exp\left(\frac{1}{4\sigma^2}\right) \tag{22}$$

From (22), we can see that the variance value is in the inverse ratio of number of testing H_{tot}. Take the case of input noise standard deviation equal to 1 LSB and 1% voltage level shift as an example, standard deviation of the estimation error will be smaller than 0.14 LSB when H_{tot} equals to 400.

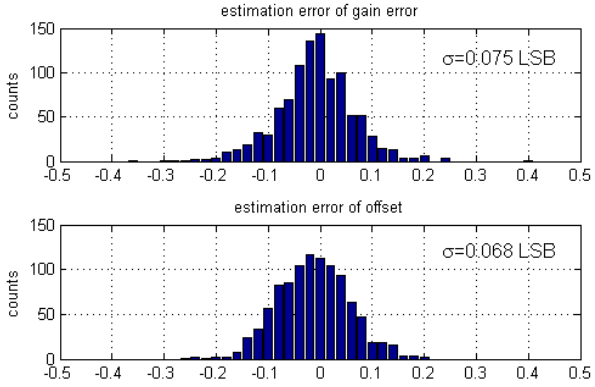

Fig.4. Estimation error of offset and gain error

Analyze the offset in the same way as gain error, the error of estimated offset is

$$\Delta E_{os} = \hat{E}_{os} - E_{os} = \sqrt{2}\sigma erf^{-1}\left(1-2\hat{P}_a\right) - \sqrt{2}\sigma erf^{-1}\left(1-2P_a\right) + INL_{Ca} - \hat{INL}_{Ca} - \frac{Ca}{2^n-2}\Delta E_g \quad (23)$$

The expectation value of ΔE_{os} is

$$E\left(\Delta E_{os}\right) = INL_{Ca} - \hat{INL}_{Ca} - \frac{Ca}{2^n-2}E\left(\Delta E_g\right) \quad (24)$$

Same as estimation error of gain error, offset estimation error is also determined by the accuracy of INL testing. The variance of the estimation error is

$$Var\left(\Delta E_{os}\right) = 2\sigma^2 \cdot Var\left[erf^{-1}\left(1-2\hat{P}_a\right)\right] + \left(\frac{C_a}{2^n-2}\right)^2 \cdot Var\left(\Delta E_g\right) \quad (25)$$

The second term is very small that can be ignored. By the same analysis as above, variance of offset estimation error can be bounded as following.

$$Var\left(\Delta E_{os}\right) \le \pi\sigma^2 \cdot \exp\left(\frac{1}{4\sigma^2}\right) \cdot \frac{1}{2H_{tot}} \quad (26)$$

In the same case as above, the standard deviation is always less than 0.07 LSB when H_{tot} equals to 400. From (22) and (26), estimation can be very accuracy with reasonable H_{tot} value.

IV. Simulation Results

Testing methods discussed above have been validated in MATLAB simulations. Simulation results are presented as following. A 14 bits flash ADC is modeled as a set of transition voltages that have random errors. Offset and gain error of the ADC are 1.6 LSB and -3.1 LSB respectively. INL of the ADC is tested by SEIR mothed with nonlinear ramp and level shift first. Then the offset and gain error is tested as discribed in section III, in which, four different voltages are tested 400 times respectively. As mentioned before, tested offset and gain error are different from their real value due to noise and approximating P by $\hat{P}$. The difference stays within a small range as long as H_{tot} is large enough. Fig.4 shows histograms of estimation error of offset and gain error from testing of 1000 different ADCs. The figure shows that standard deviations of the estimation errors are very small and close the value given by error analysis.

V. Conclusion

A low cost method for measuring ADC's offset and gain error is presented. The measurement is based on tested INL data, thus only 3 DC voltages are needed. The additional hardware requirement is very small. Combine with other published INL and spectral performance test methods, Most ADC parameters commonly tested are now can be tested on chip with low cost.

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