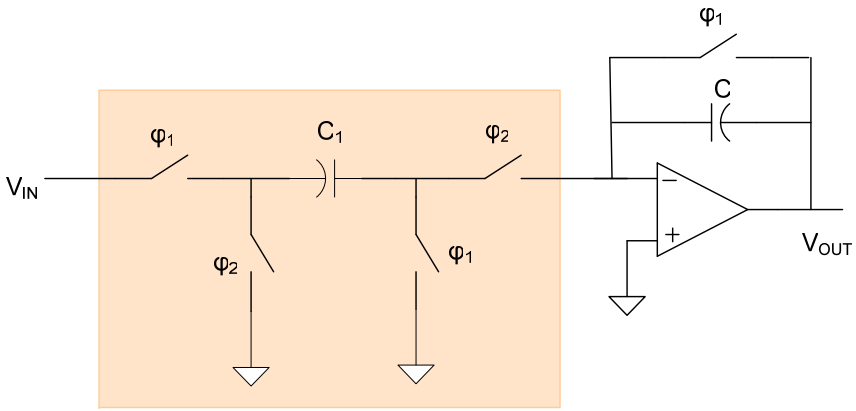
EE 435
Lecture 44

Switched-Capacitor Amplifiers

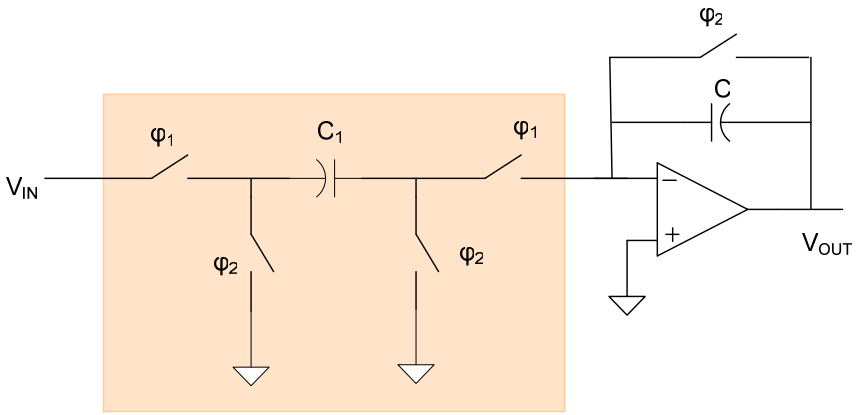
Other Integrated Filters

Switched-Capacitor Amplifiers



Noninverting Amplifier

$$A_V = \frac{C_1}{C}$$

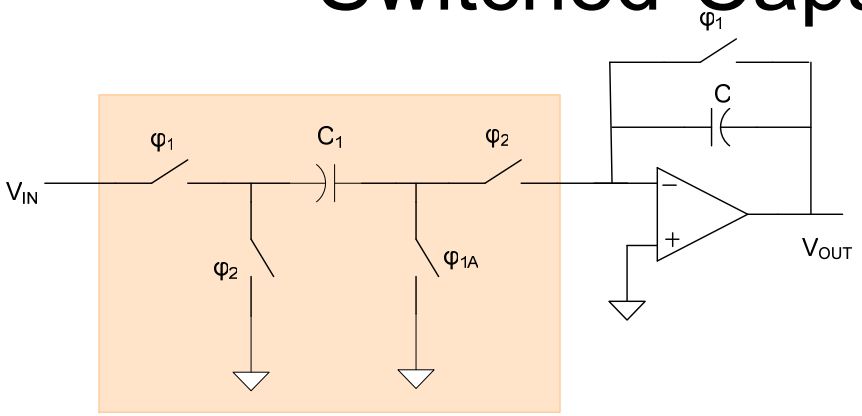


Inverting Amplifier

$$A_V = -\frac{C_1}{C}$$

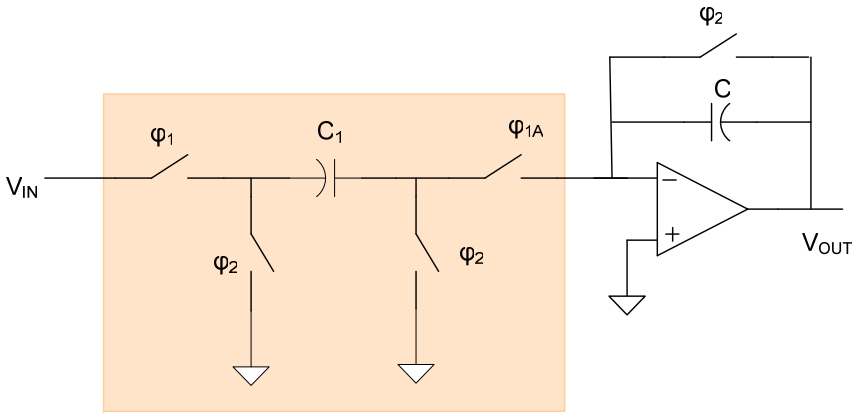
- Accurate control of gain is possible (0.1% or better) but extreme care to detail in layout and statistical analysis for adequate area allocation is necessary
- Stray-insensitive structures

Switched-Capacitor Amplifiers



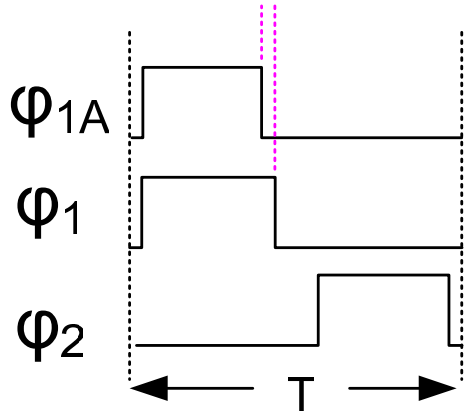
Noninverting Amplifier

$$A_V = \frac{C_1}{C}$$



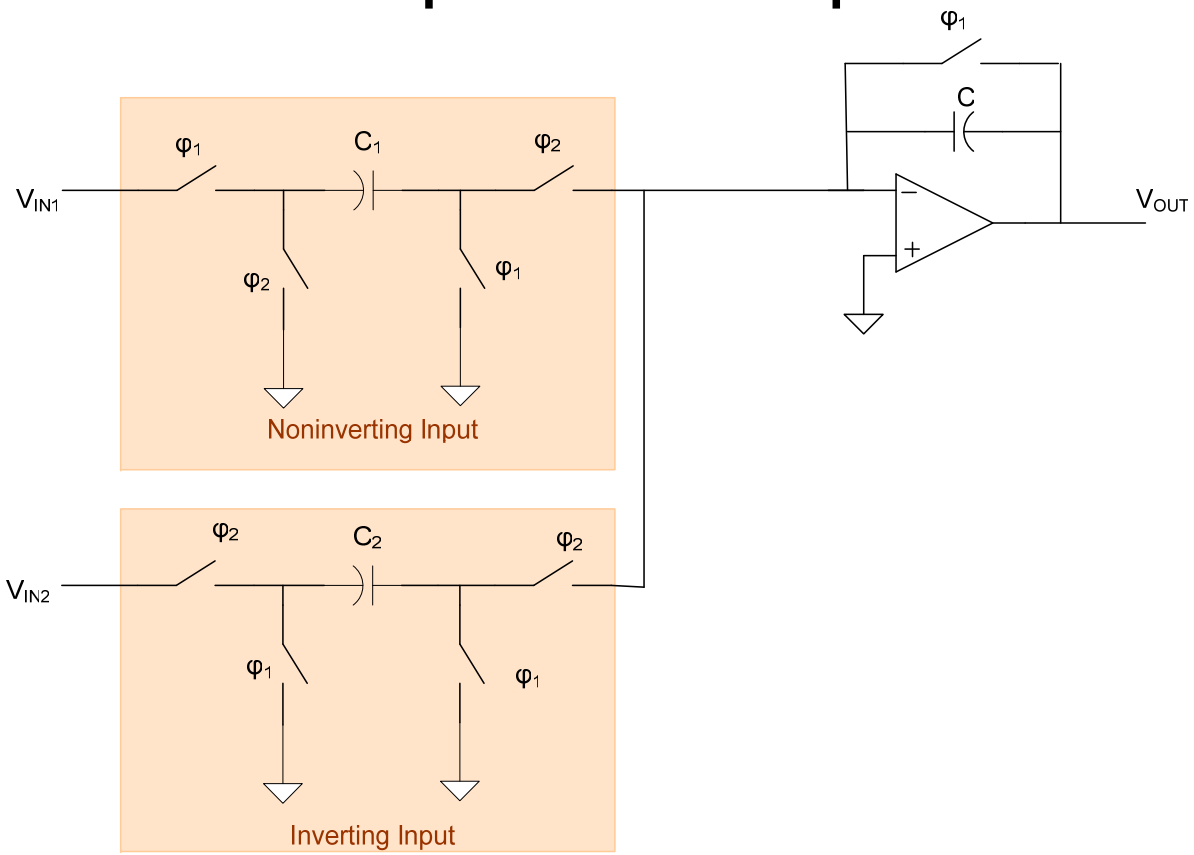
Inverting Amplifier

$$A_V = -\frac{C_1}{C}$$



Bottom-plate sampling with advanced clock reduces signal-dependent gain errors when V_{IN} is time varying: Sample and Hold

Switched-Capacitor Amplifiers

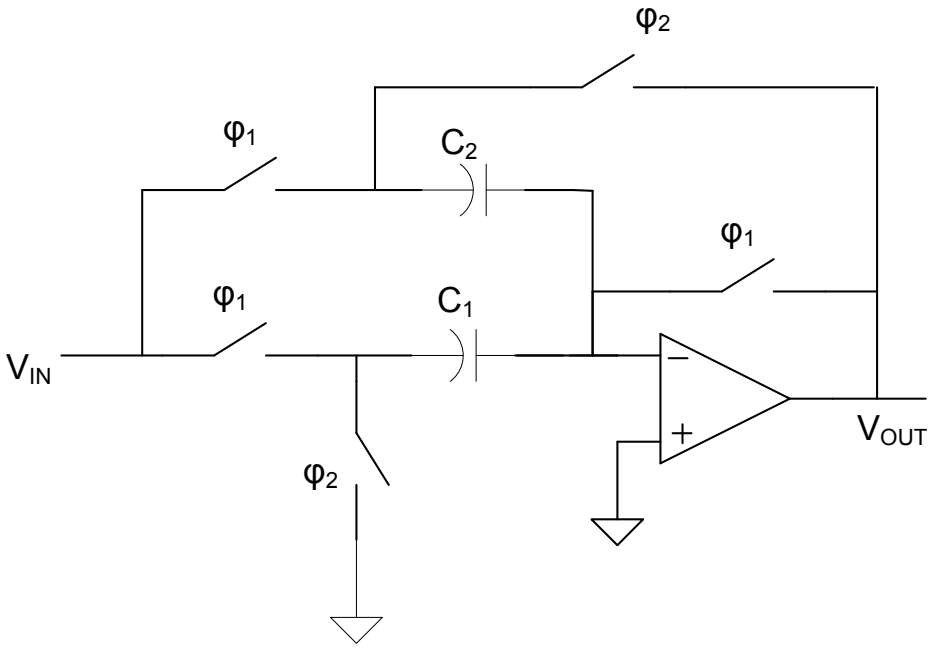


Summing Inverting and Noninverting Amplifier

$$V_{OUT} = \frac{C_1}{C} V_{IN1} - \frac{C_2}{C} V_{IN2}$$

(modification for bottom-plate sampling needed if V_{IN} is time varying: track and hold)

Switched-Capacitor Amplifiers

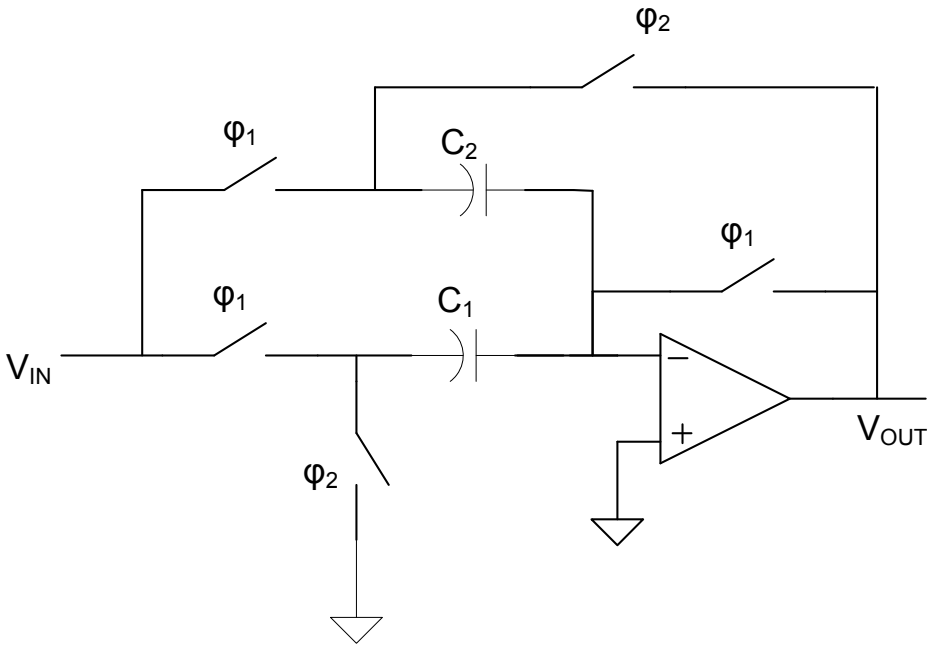


$$A_V = 1 + \frac{C_1}{C_2}$$

Flip-Around Amplifier

(modification for bottom-plate sampling needed if V_{IN} is time varying: track and hold)

Switched-Capacitor Amplifiers



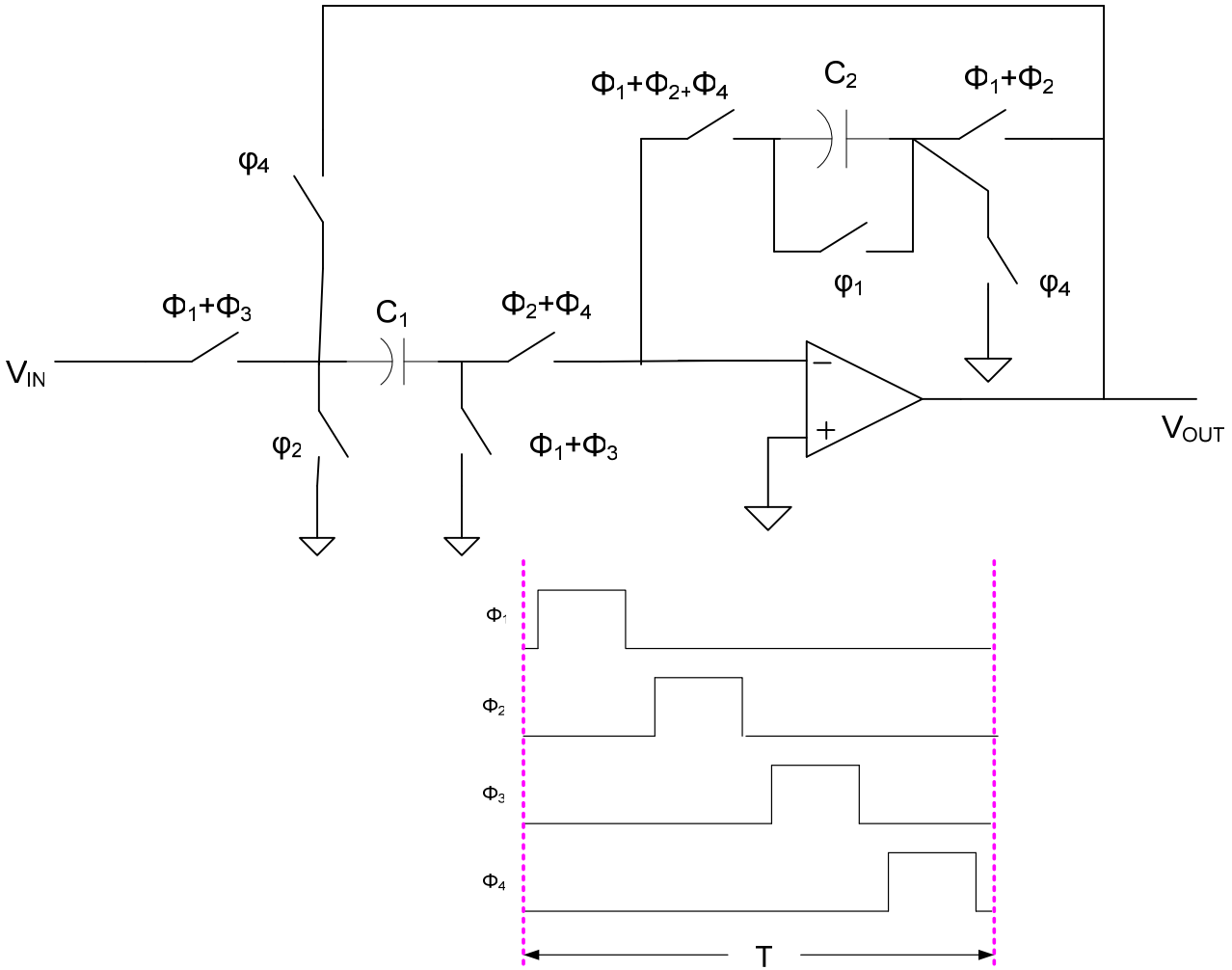
$$V_{OUT} = V_{IN1}\left(1 + \frac{C_1}{C_2}\right) - V_{IN2}\left(\frac{C_1}{C_2}\right)$$

Flip-Around Subtracting Amplifier

(modification for bottom-plate sampling needed if V_{IN} is time varying: track and hold)

Switched-Capacitor Amplifiers

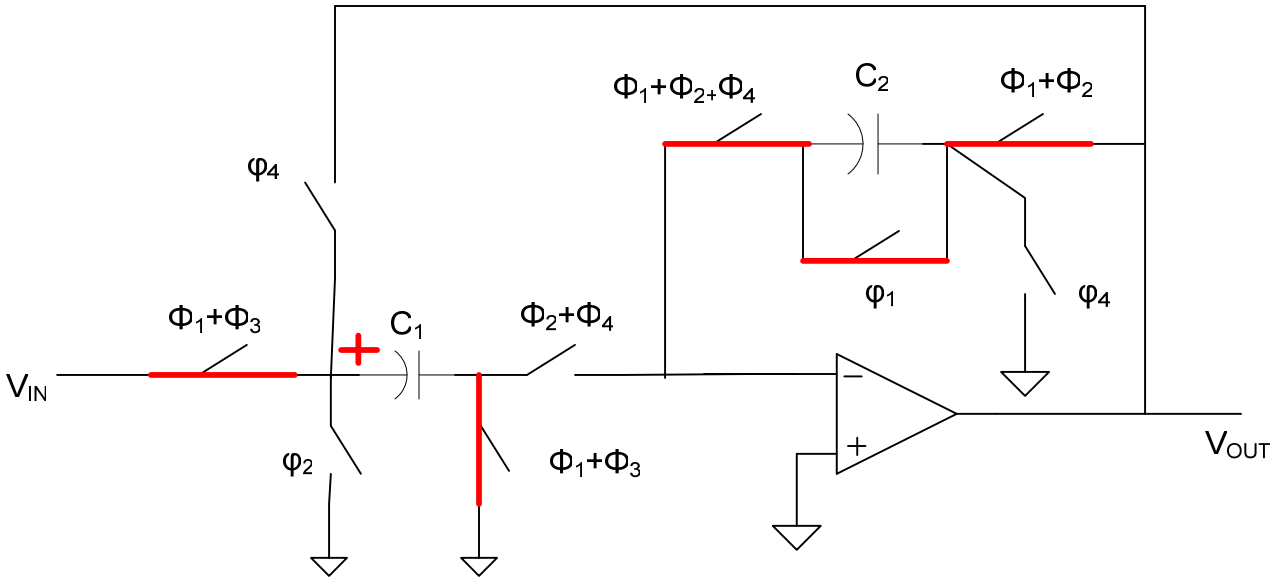
Consider the following circuit



Switched-Capacitor Amplifiers

Consider the following circuit

During phase Φ_1

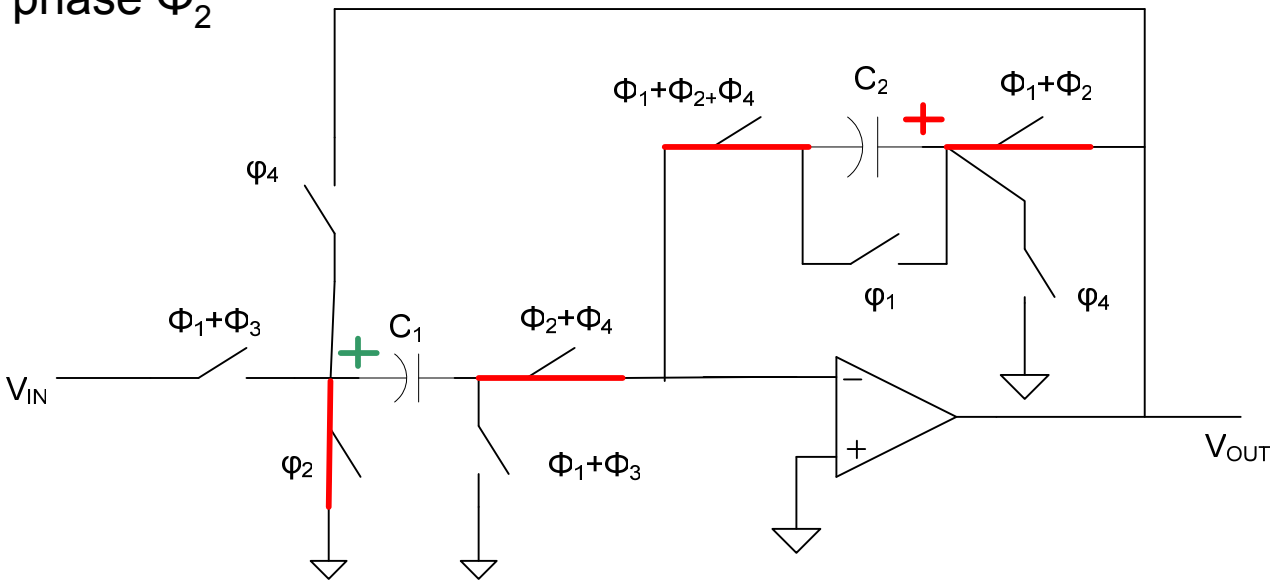


$$Q_{C1}=C_1V_{IN}$$

Switched-Capacitor Amplifiers

Consider the following circuit

During phase Φ_2



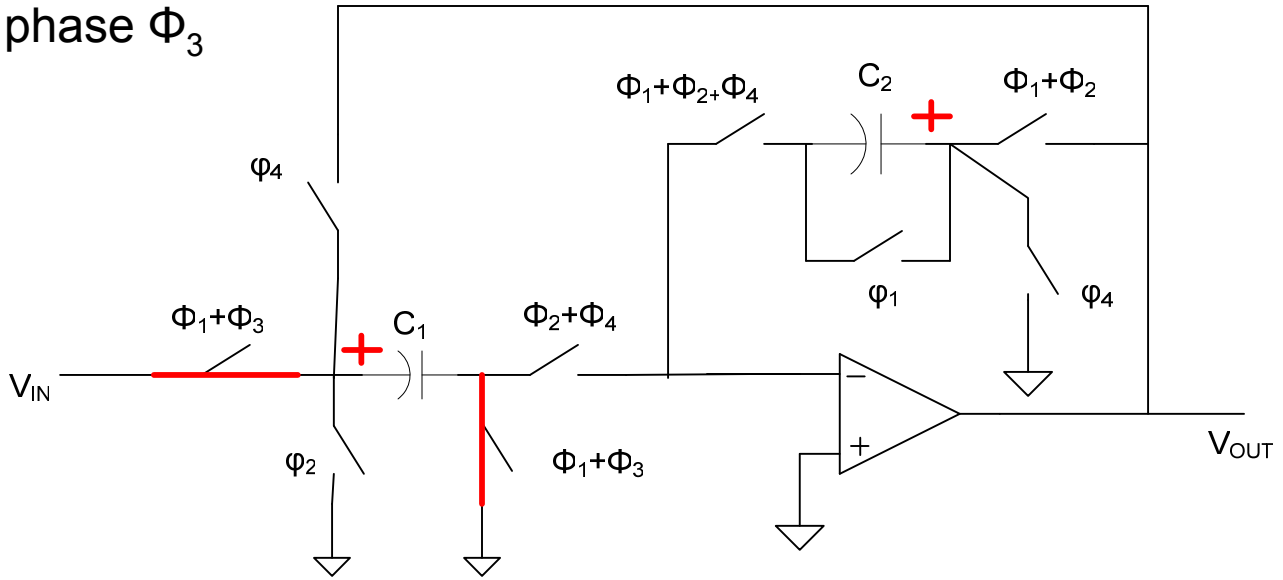
from Φ_1 $Q_{C1}=C_1V_{IN}$

during Φ_2 $Q_{C1}=0$ $Q_{C2}=C_1V_{IN}$

Switched-Capacitor Amplifiers

Consider the following circuit

During phase Φ_3



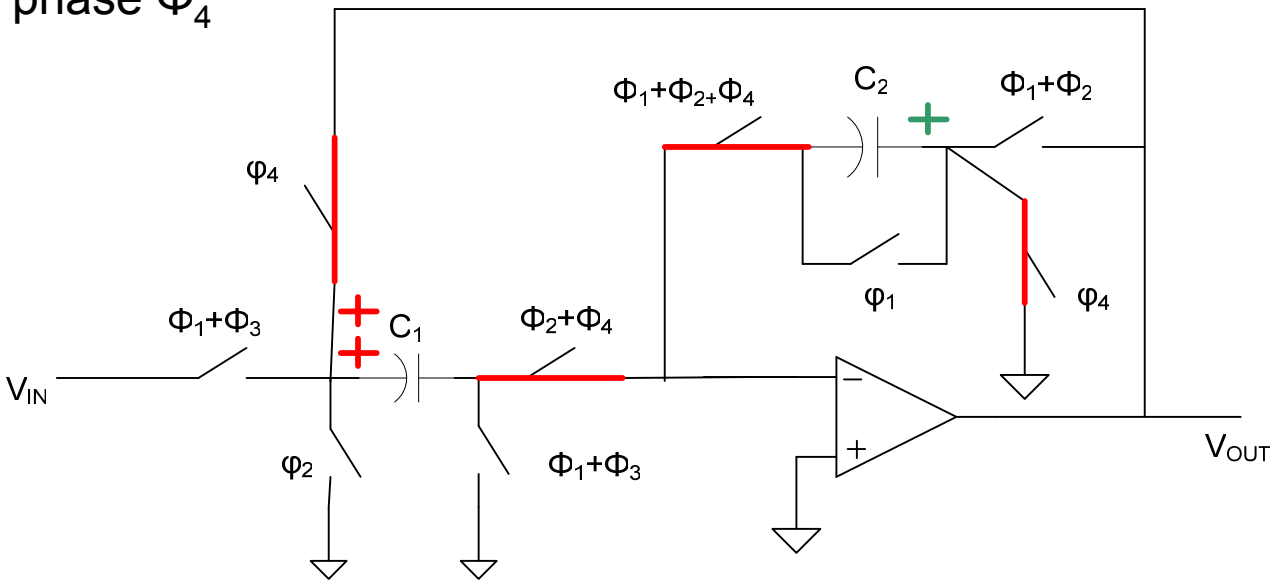
from Φ_2 $Q_{C1}=0$ $Q_{C2}=C_1V_{IN}$

during Φ_2 $Q_{C1}=C_1V_{IN}$ $Q_{C2}=C_1V_{IN}$

Switched-Capacitor Amplifiers

Consider the following circuit

During phase Φ_4



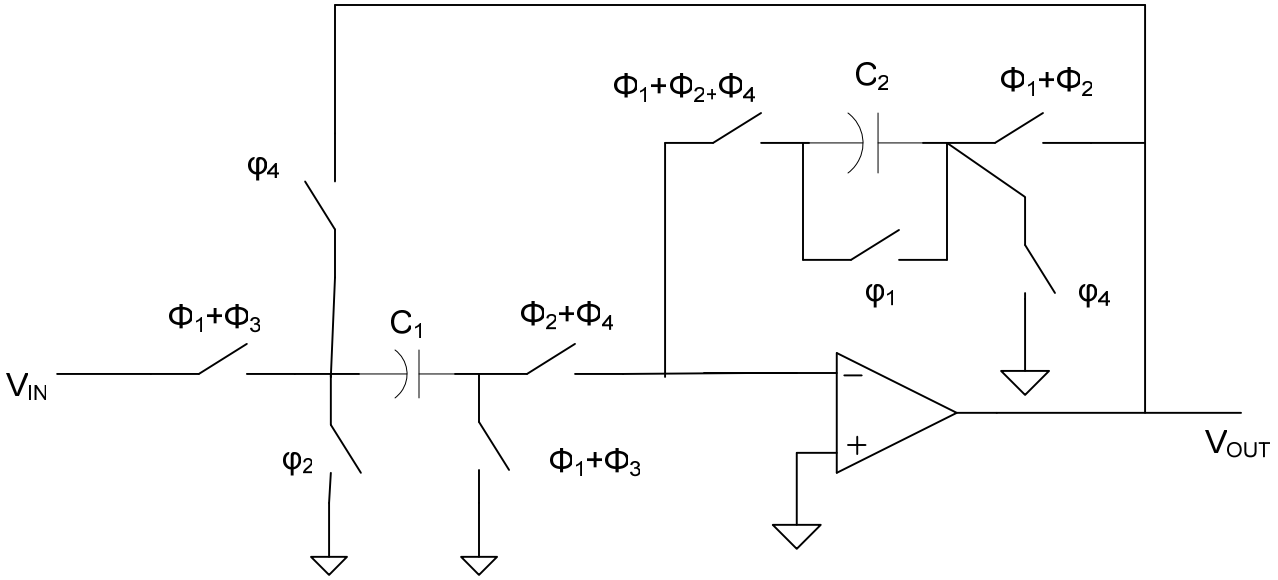
from Φ_3 $Q_{C1}=C_1V_{IN}$ $Q_{C2}=C_1V_{IN}$

during Φ_2 $Q_{C2}=0$ $Q_{C1}=2C_1V_{IN}$

Thus $V_{OUT}=Q_{C1}/C_1=2V_{IN}$

Switched-Capacitor Amplifiers

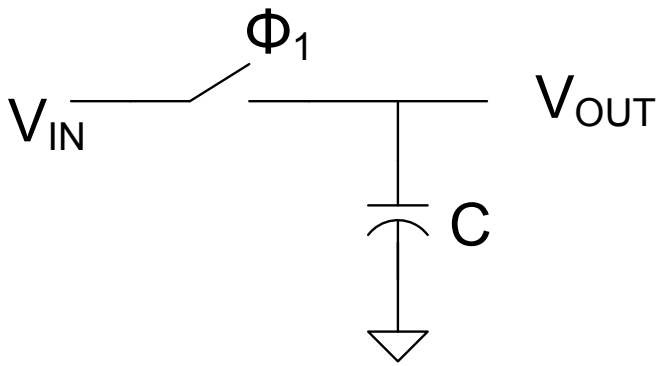
Consider the following circuit



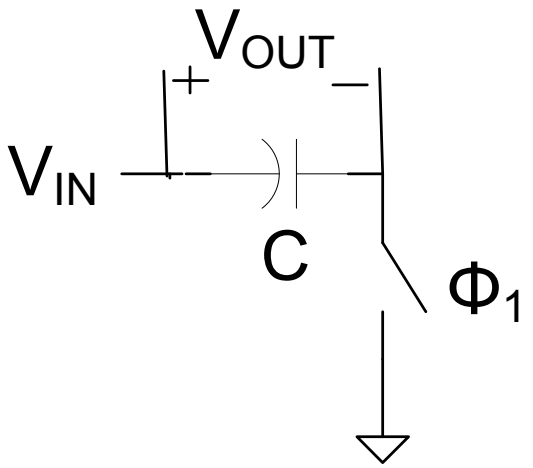
$$A_V = 2$$

Gain of 2 obtained without requiring any matching of components

Top-Plate vs Bottom-Plate Sampling



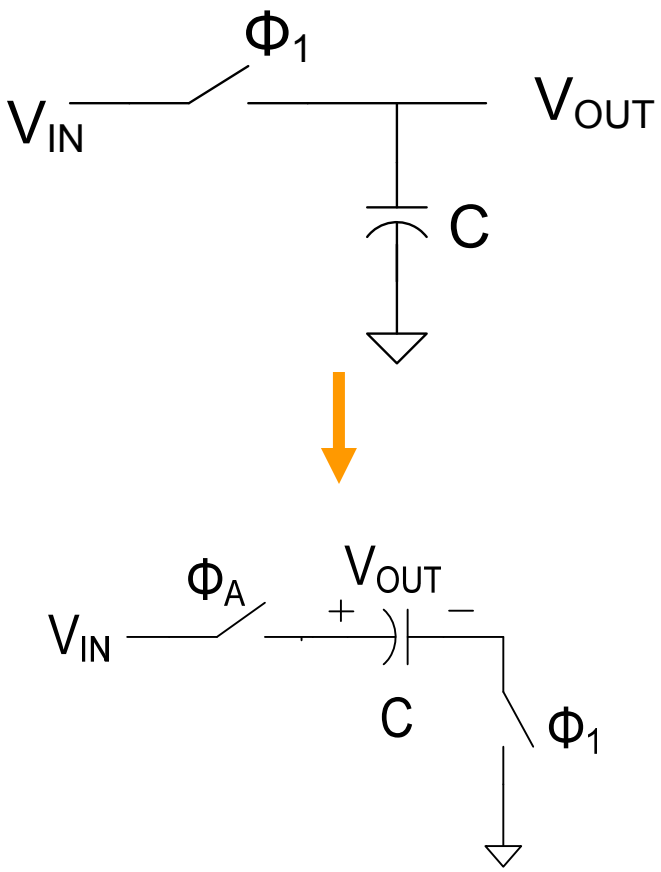
Top-Plate Sampling



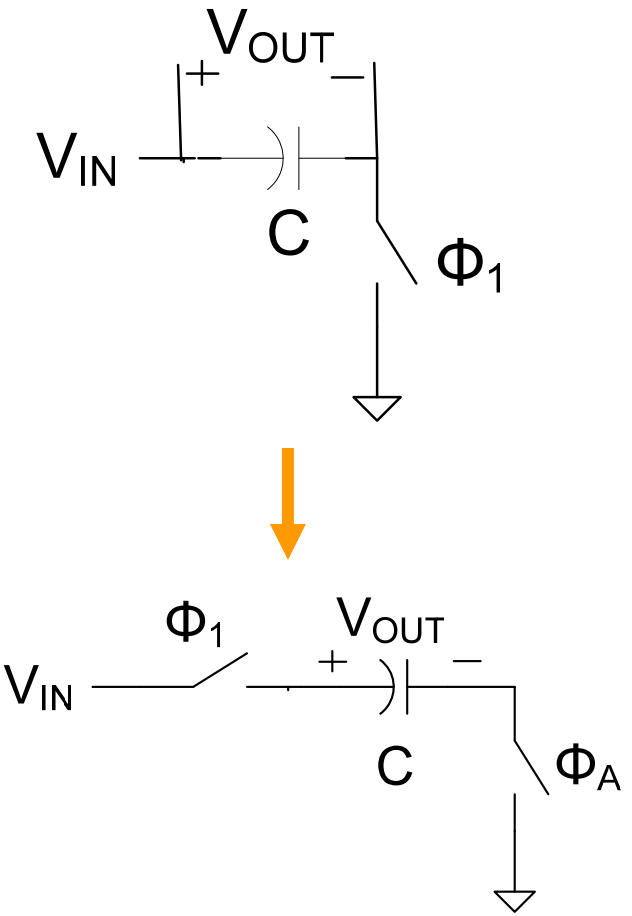
Bottom-Plate Sampling

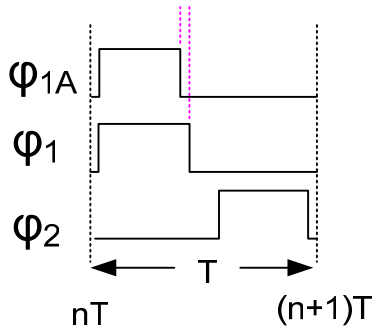
Top-Plate vs Bottom-Plate Sampling

Top-Plate Sampling

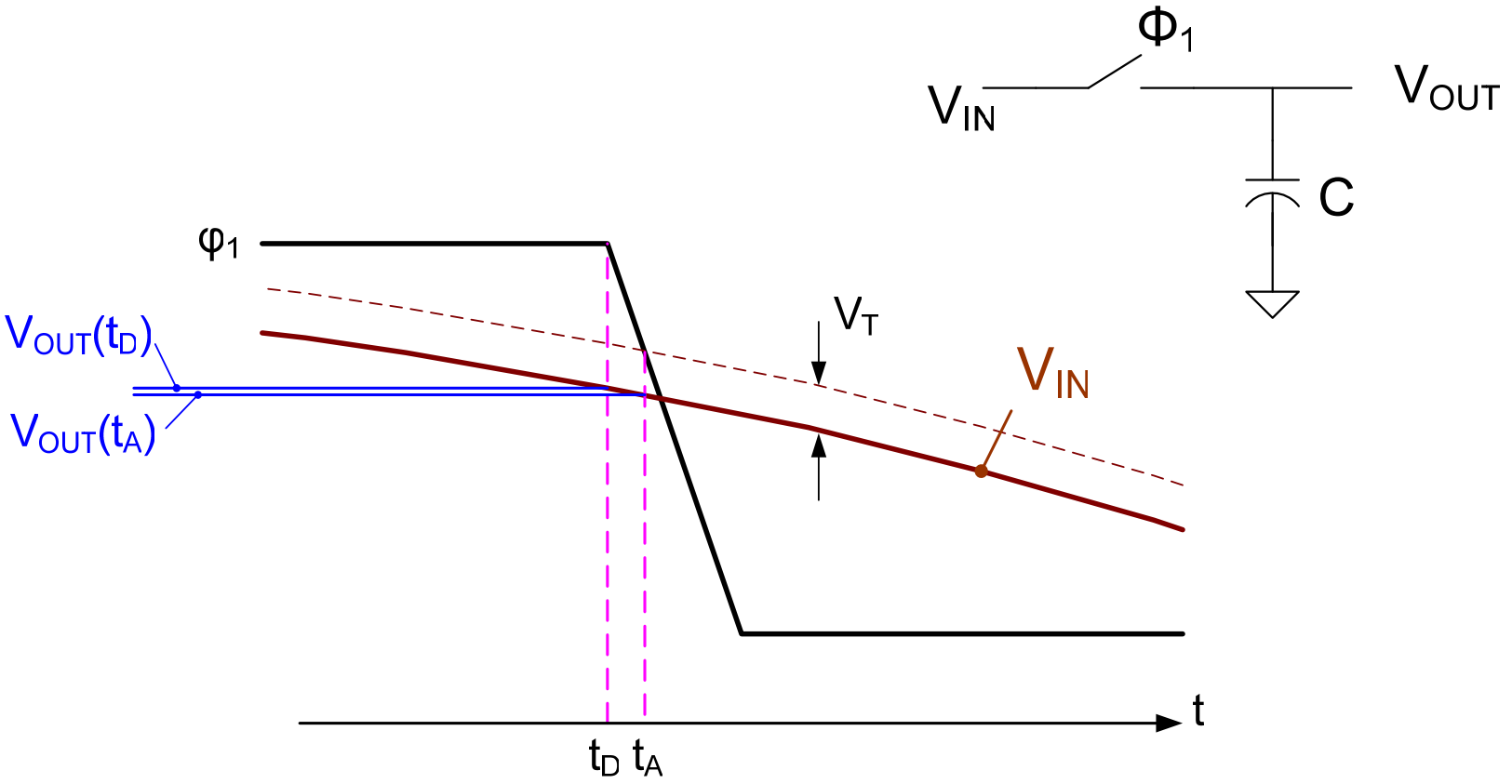


Bottom-Plate Sampling



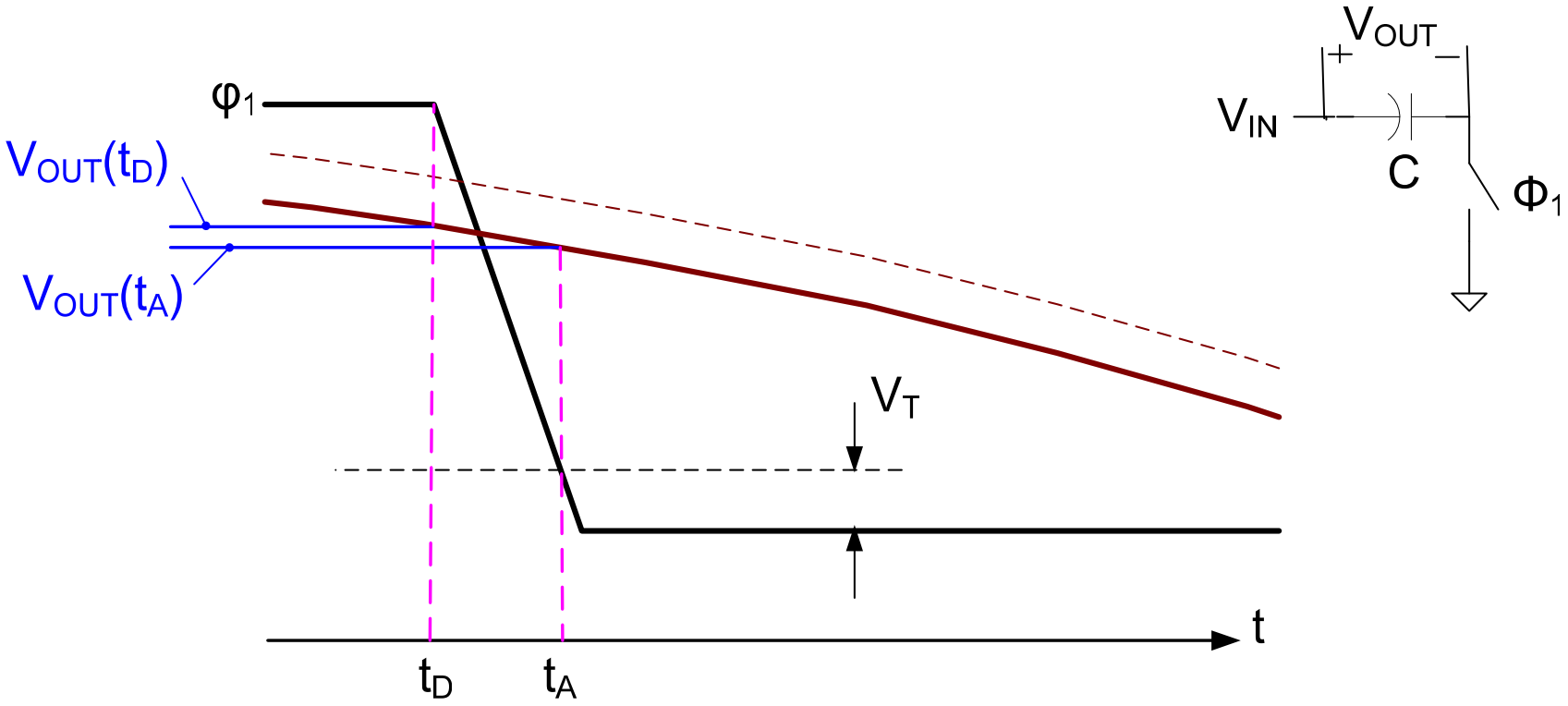


Top-Plate Sampling



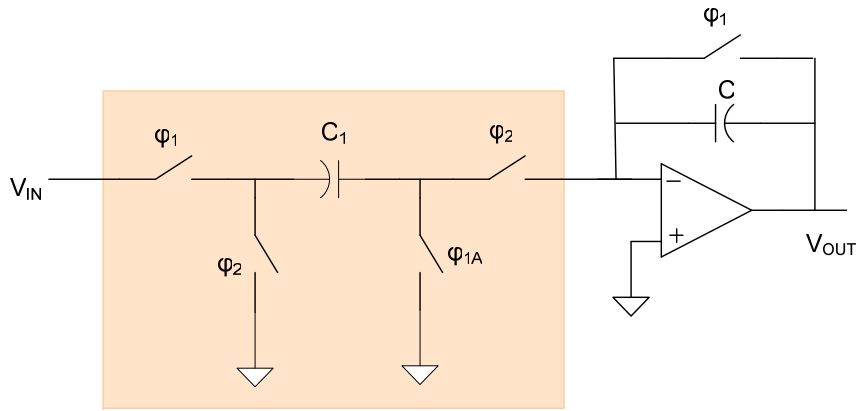
- Actual sample taken at t_A
- Sampled-value is signal-level dependent
- Equivalent to a signal-dependent jitter on sampling clock
- Causes serious nonlinear distortion if signal frequency is high

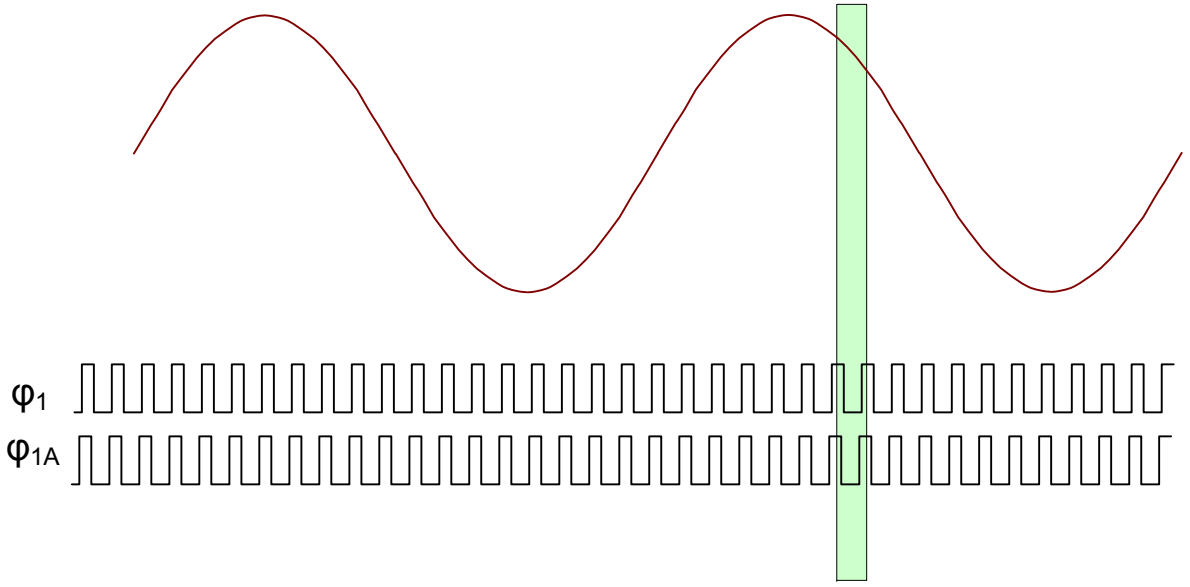
Bottom-Plate Sampling



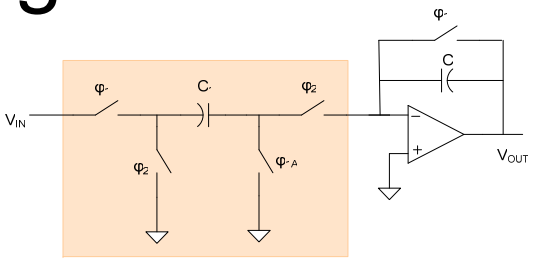
- Actual sample taken at t_A
- t_A-t_D is independent of $V_{IN}(t)$
- Dramatic reduction in nonlinear distortion and signal-dependent sampling error
- Effectively causes a constant phase shift in sampling time

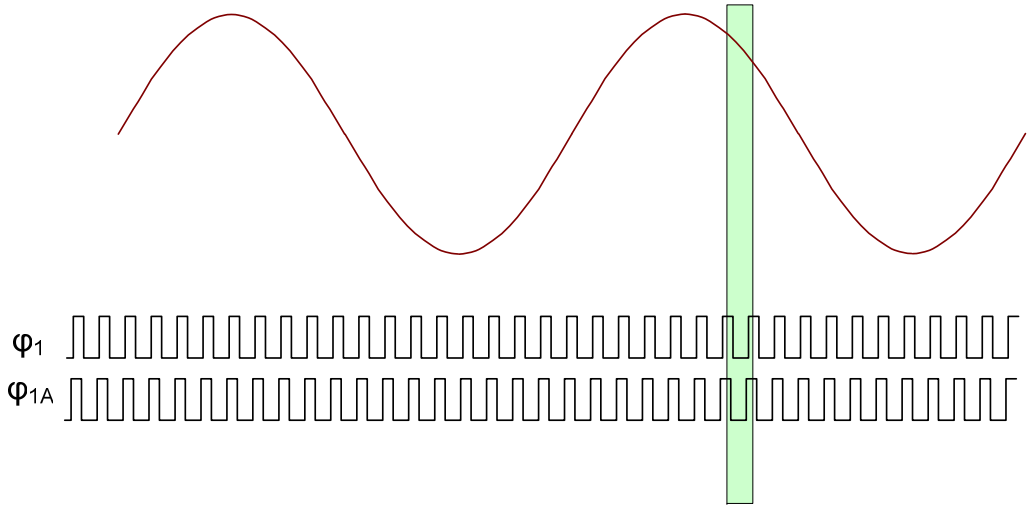
Bottom-Plate Sampling



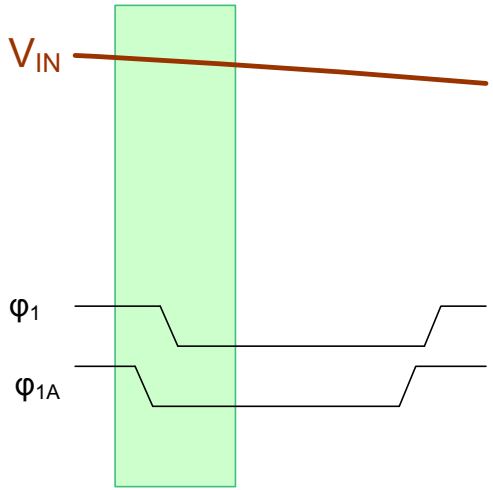


Bottom-Plate Sampling

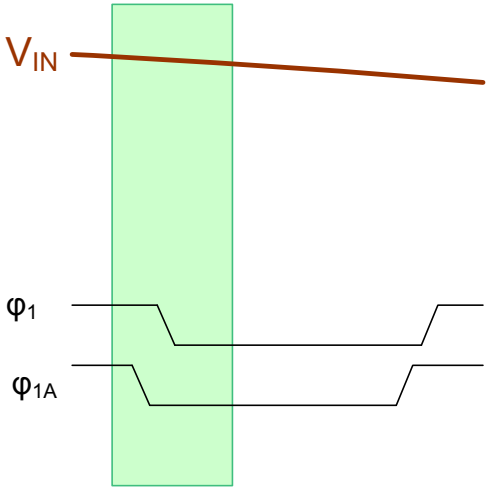


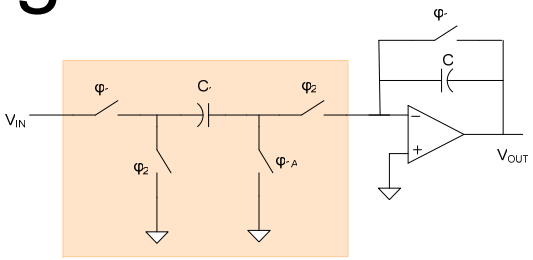


Expanded time axis:

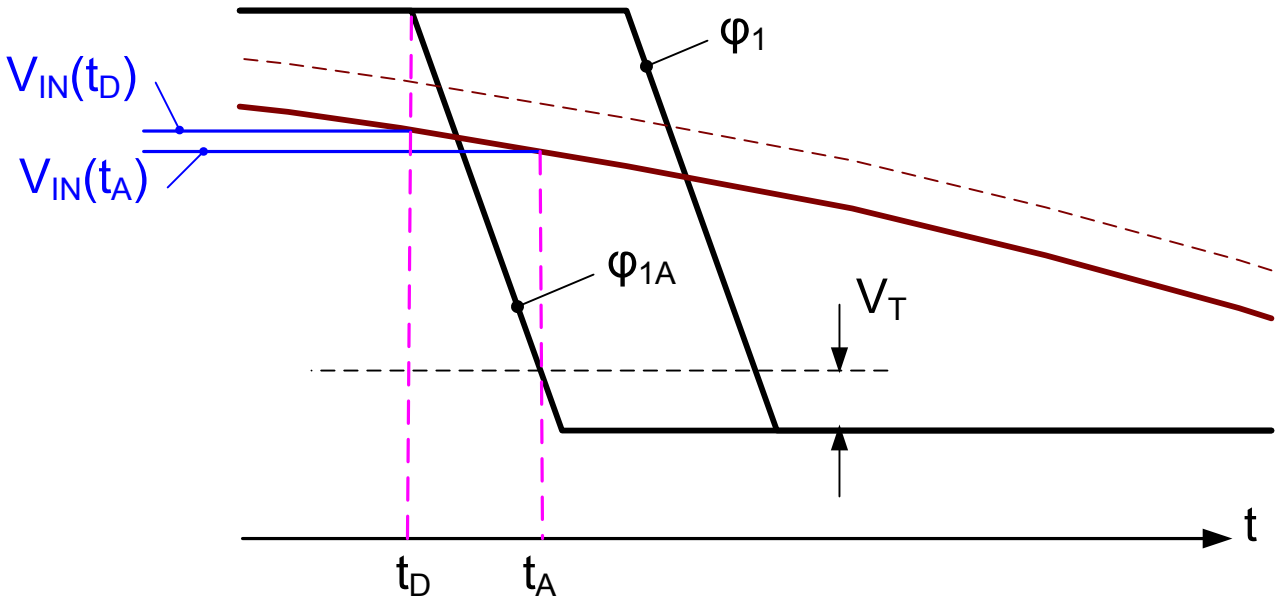


Bottom-Plate Sampling

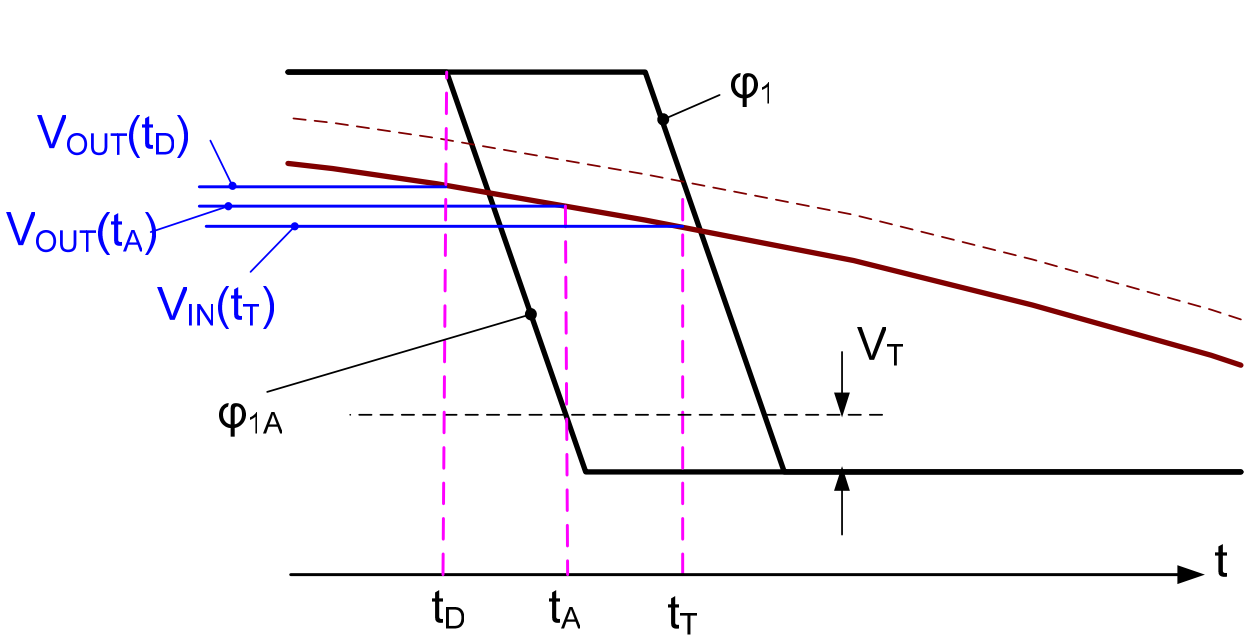


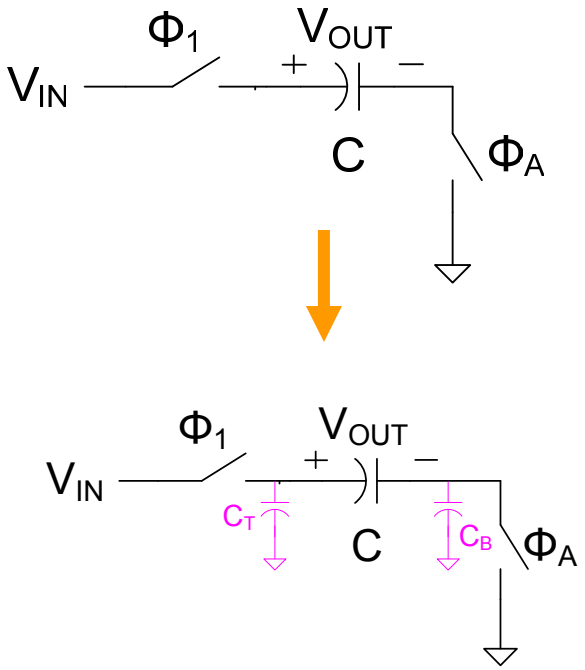


Further expanded time axis (V_{IN} change exaggerated to show effects):



Bottom-Plate Sampling

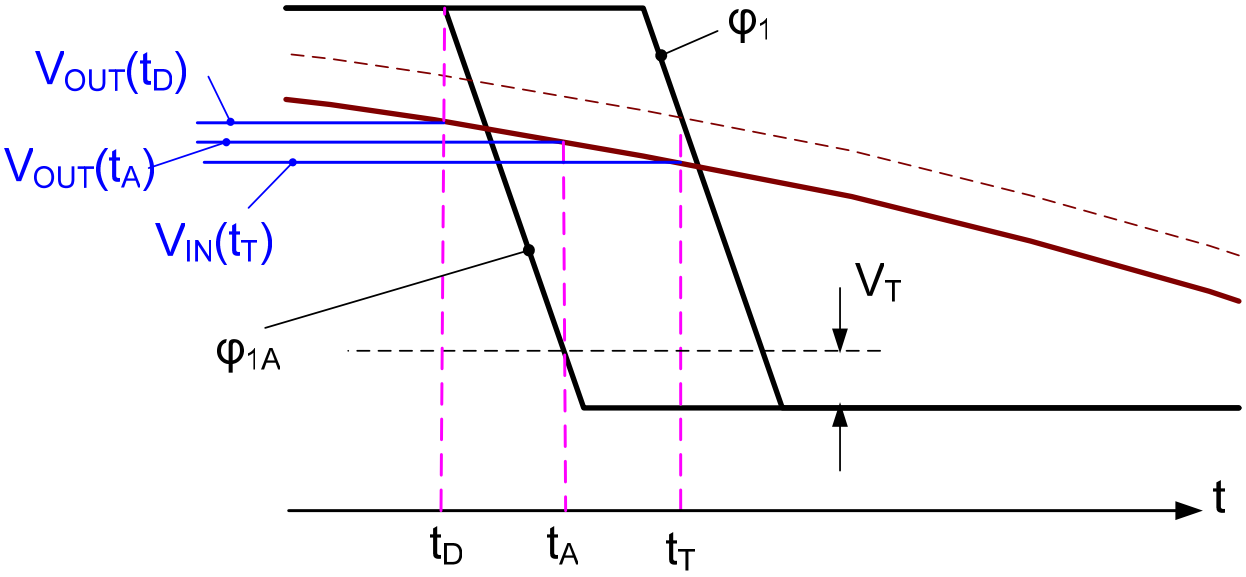


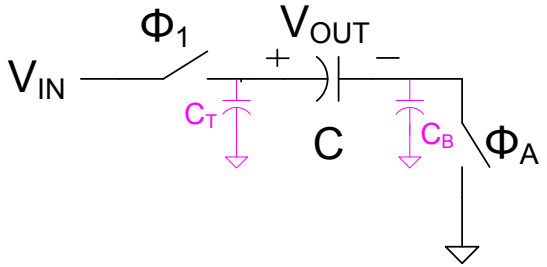


C_T and C_B are parasitic capacitances that appear at nodes connected to top plate and bottom plate of C

- Actual sample taken at t_A
- t_A-t_D is independent of $V_{IN}(t)$
- Some change in V_{OUT} will occur until Φ_1 opens
- Time Φ_1 opens is input signal-level dependent

Bottom-Plate Sampling





$$V_{OUT}(t_A) = V_{IN}(t_A)$$

but:

$$V_{OUT}(t_T) = V_{IN}(t_A) + \left(\frac{C_B}{C+C_B}\right)\left(V_{IN}(t_T) - V_{IN}(t_A)\right)$$

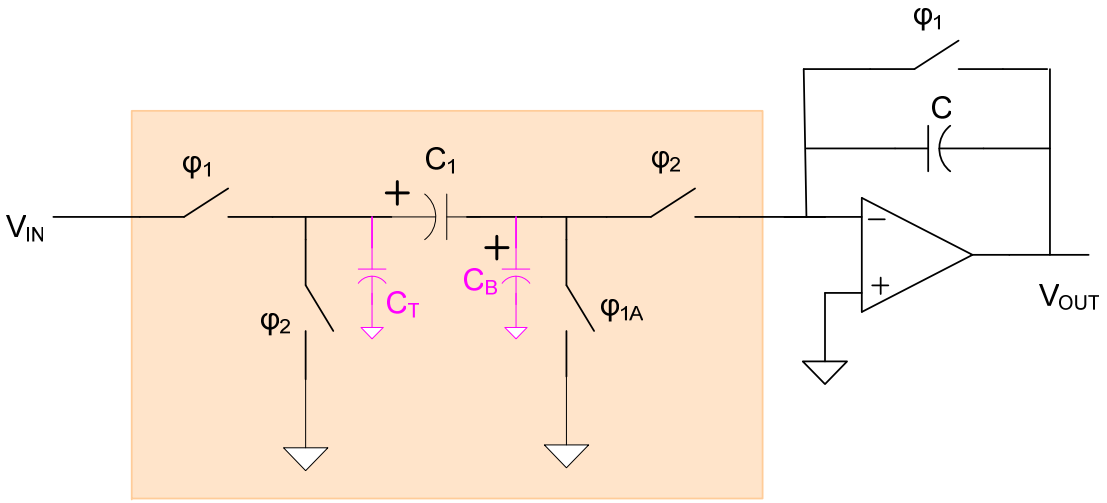
can be rewritten as:

$$V_{OUT}(t_T) = V_{IN}(t_A)\left[\frac{C}{C+C_B}\right] + \left(\frac{C_B}{C+C_B}\right)V_{IN}(t_T)$$

- Gain error on sampling V_{IN} at t_A
- Dependent upon $V_{IN}(t_T)$ which causes distortion in sample
- C_B can be a reasonable percentage of C

Bottom-Plate Sampling

Consider the entire SC amplifier



$$V_{C_1}(t_T) = V_{IN}(t_A)\left[\frac{C_1}{C_1+C_B}\right]+\left(\frac{C_B}{C_1+C_B}\right)V_{IN}(t_T)$$

Likewise:

$$V_{C_B}(t_T) = \left(\frac{C_1}{C_1+C_B}\right)V_{IN}(t_T)-\left(\frac{C_1}{C_1+C_B}\right)V_{IN}(t_A)$$

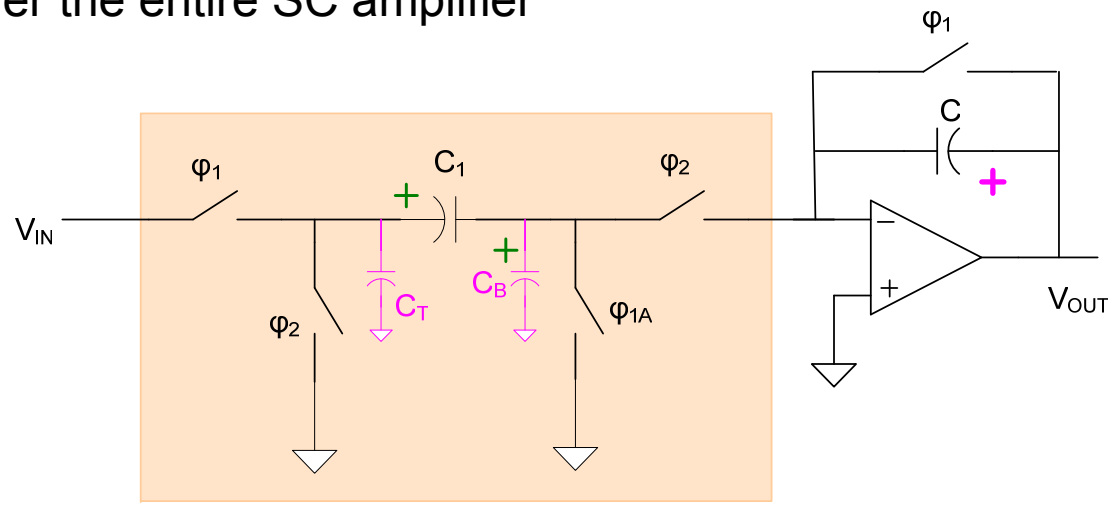
Thus charges stored on C_1 and C_B at t_T are

$$Q_{C_1}(t_T) = C_1V_{IN}(t_A)\left[\frac{C_1}{C_1+C_B}\right]+C_1\left(\frac{C_B}{C_1+C_B}\right)V_{IN}(t_T)$$

$$Q_{C_B}(t_T) = C_B\left(\frac{C_1}{C_1+C_B}\right)V_{IN}(t_T)-C_B\left(\frac{C_1}{C_1+C_B}\right)V_{IN}(t_A)$$

Bottom-Plate Sampling

Consider the entire SC amplifier



$$Q_{C_1}(t_T) = C_1 V_{IN}(t_A)\left[\frac{C_1}{C_1+C_B}\right] + C_1\left(\frac{C_B}{C_1+C_B}\right)V_{IN}(t_T)$$

$$Q_{C_B}(t_T) = C_B\left(\frac{C_1}{C_1+C_B}\right)V_{IN}(t_T) - C_B\left(\frac{C_1}{C_1+C_B}\right)V_{IN}(t_A)$$

During Φ_2, these capacitors are both discharged and the charge on feedback capacitor C becomes

$$Q_C = Q_{C_1} - Q_{C_B}$$

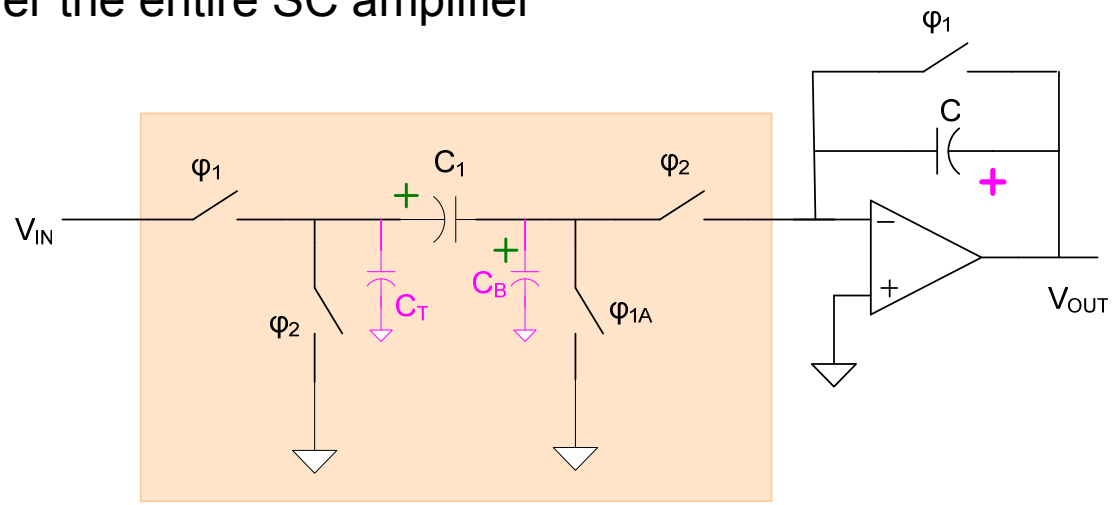
it thus follows that

$$Q_C(t_T) = C_1 V_{IN}(t_A)$$

- Extra charge accumulated on C_1 until the top switch opened equal to charge accumulated on C_B
- For switching scheme used here, effects precisely cancel when charge is transferred to C

Bottom-Plate Sampling

Consider the entire SC amplifier



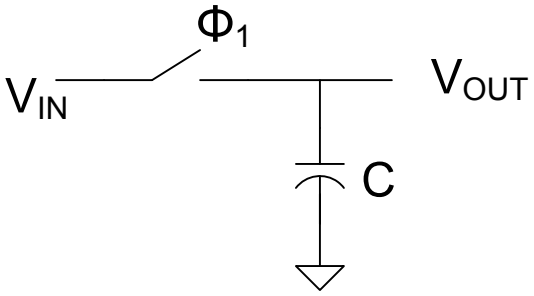
$$Q_C(t_T) = C_1 V_{IN}(t_A)$$

Thus:

$$V_{OUT}(t_T) = \frac{Q_C(t_T)}{C} = \frac{C_1}{C} V_{IN}(t_A)$$

As predicted the output voltage is not a function of t_T and thus the parasitic capacitance on the bottom Plate does not affect performance when bottom plate sampling is used

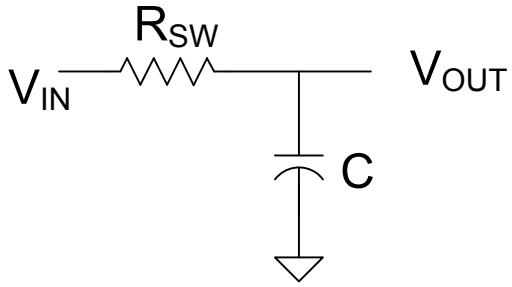
Switch impedance issues

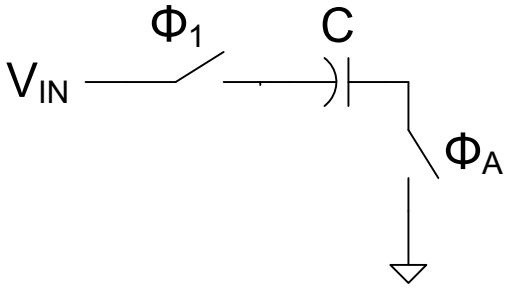


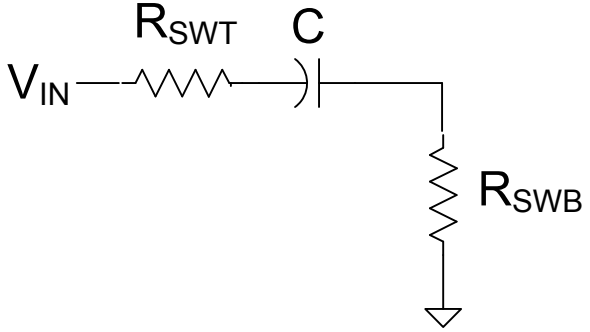
$$T(s)=\frac{V_{OUT}(s)}{V_{IN}(s)}=\frac{1}{1+R_{SW}Cs}$$

$$\left|T(j\omega)\right|=\frac{1}{\sqrt{1+(R_{SW}C\omega)^2}}$$

$$\angle T(j\omega)=-\tan^{-1}\left(\frac{\omega R_{SW}C}{1}\right)$$

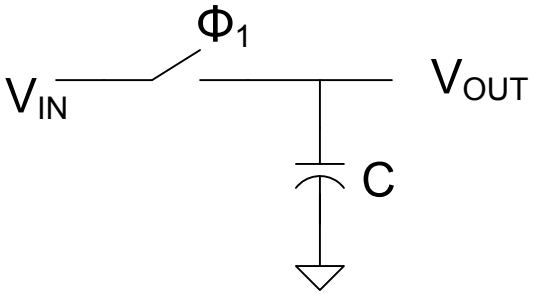


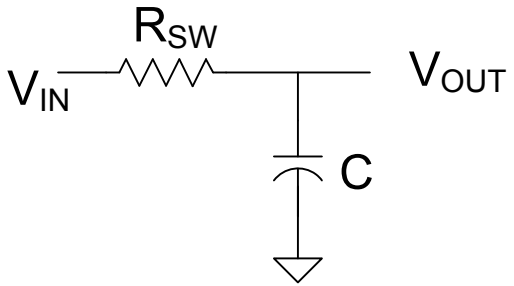


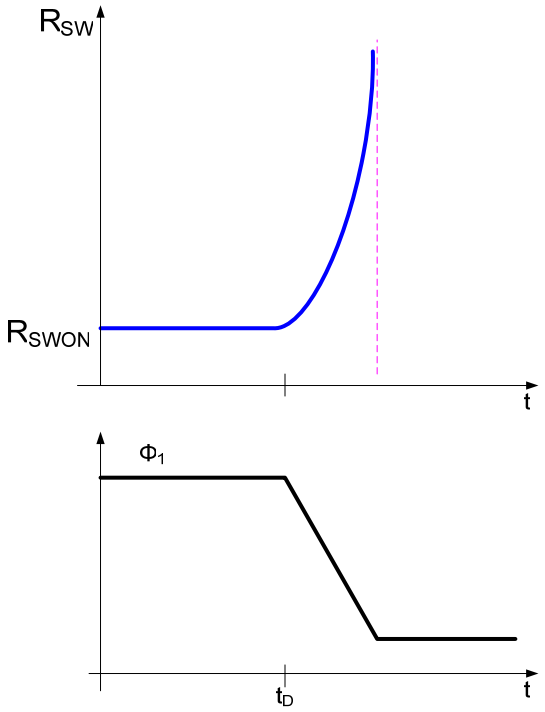


- When in track mode, non-zero R_{SW} causes small amplitude decrease and phase shift but no nonlinear distortion provided R_{SW} is not signal-level dependent
- Top-plate switch (R_{SW} or R_{SWT}) is signal level dependent if implemented with simple transistor
- Bottom-plate switch (R_{SWB}) is not signal-level dependent
- Make R_{SW} and R_{SWT} sufficiently small to avoid distortion

Switch impedance issues

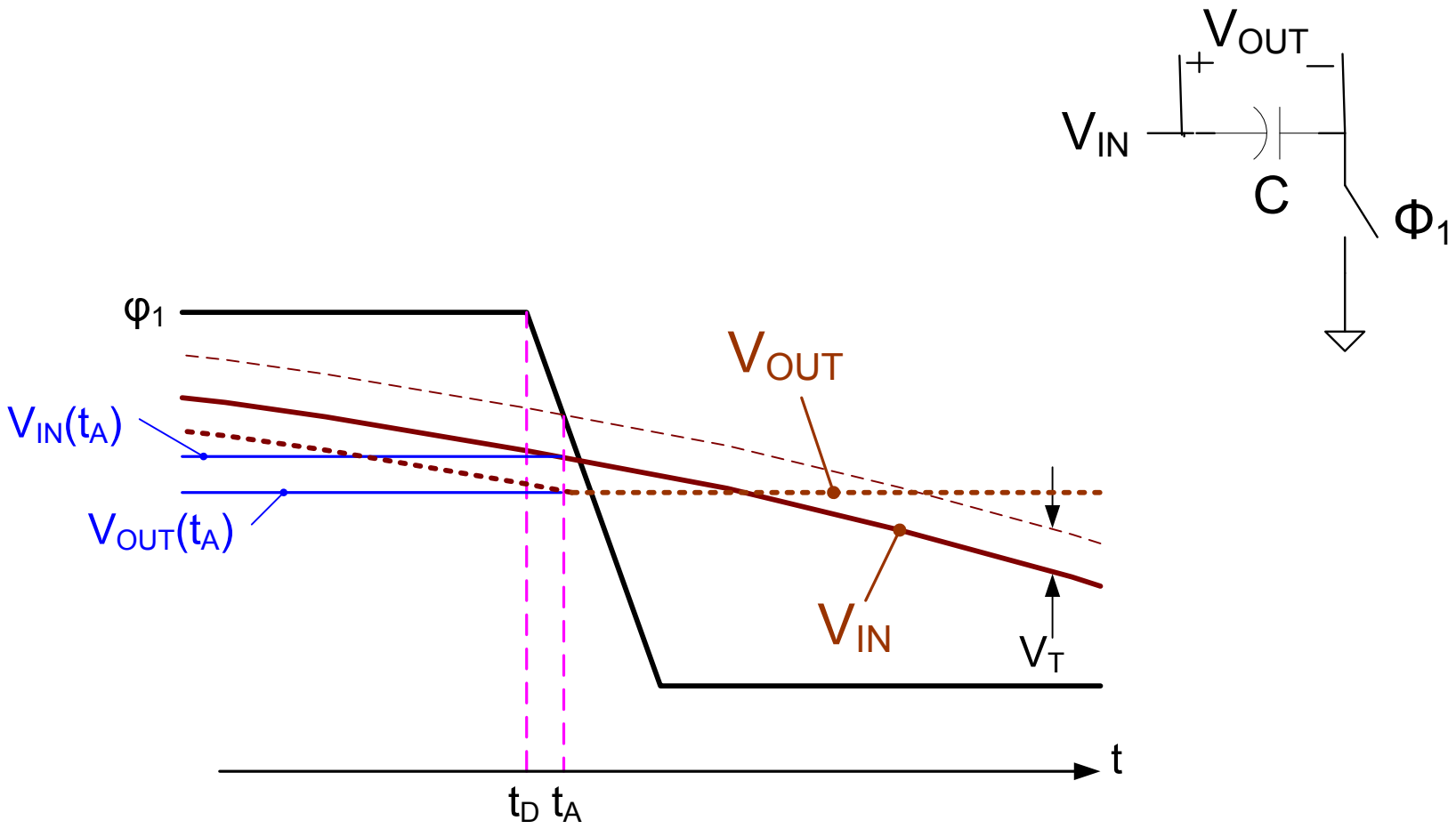






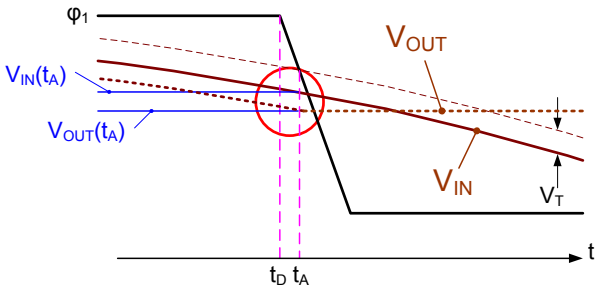
When transitioning from track mode to hold mode, swtich impedance increases rapidly from non-zero R_{SW}

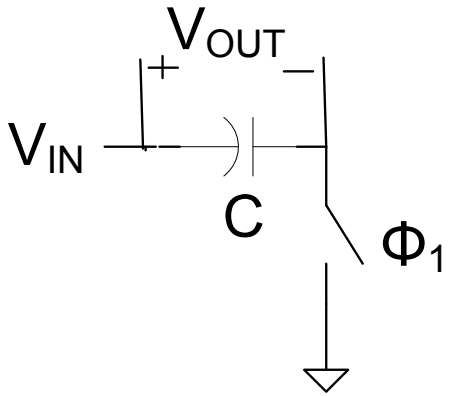
Switch impedance issues

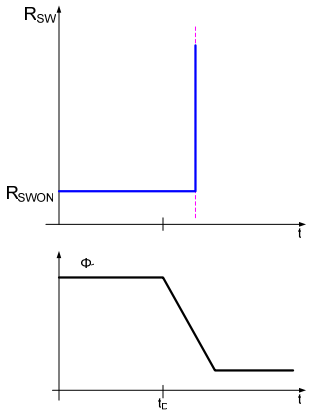


Amplitude and phase shift for bottom-plate sampler (difficult to distinguish between phase and amplitude effects in this zoom)

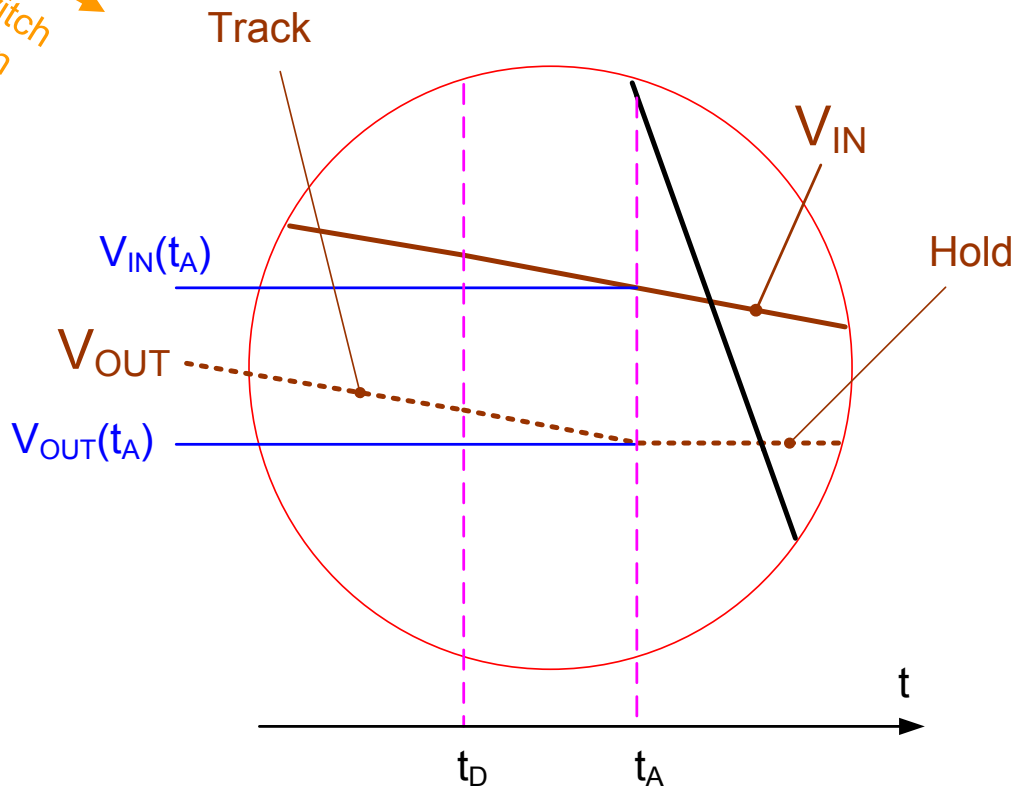
Switch impedance issues



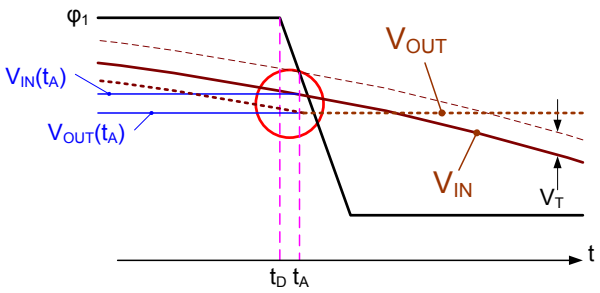


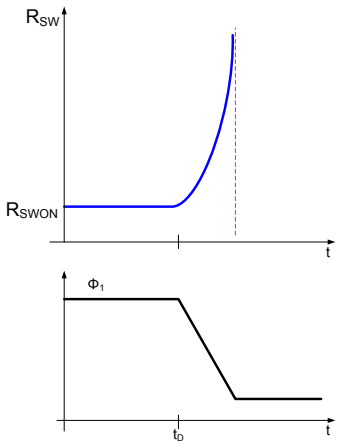


Ideal Switch Transition

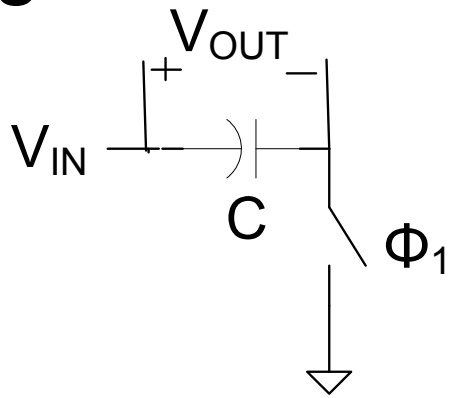


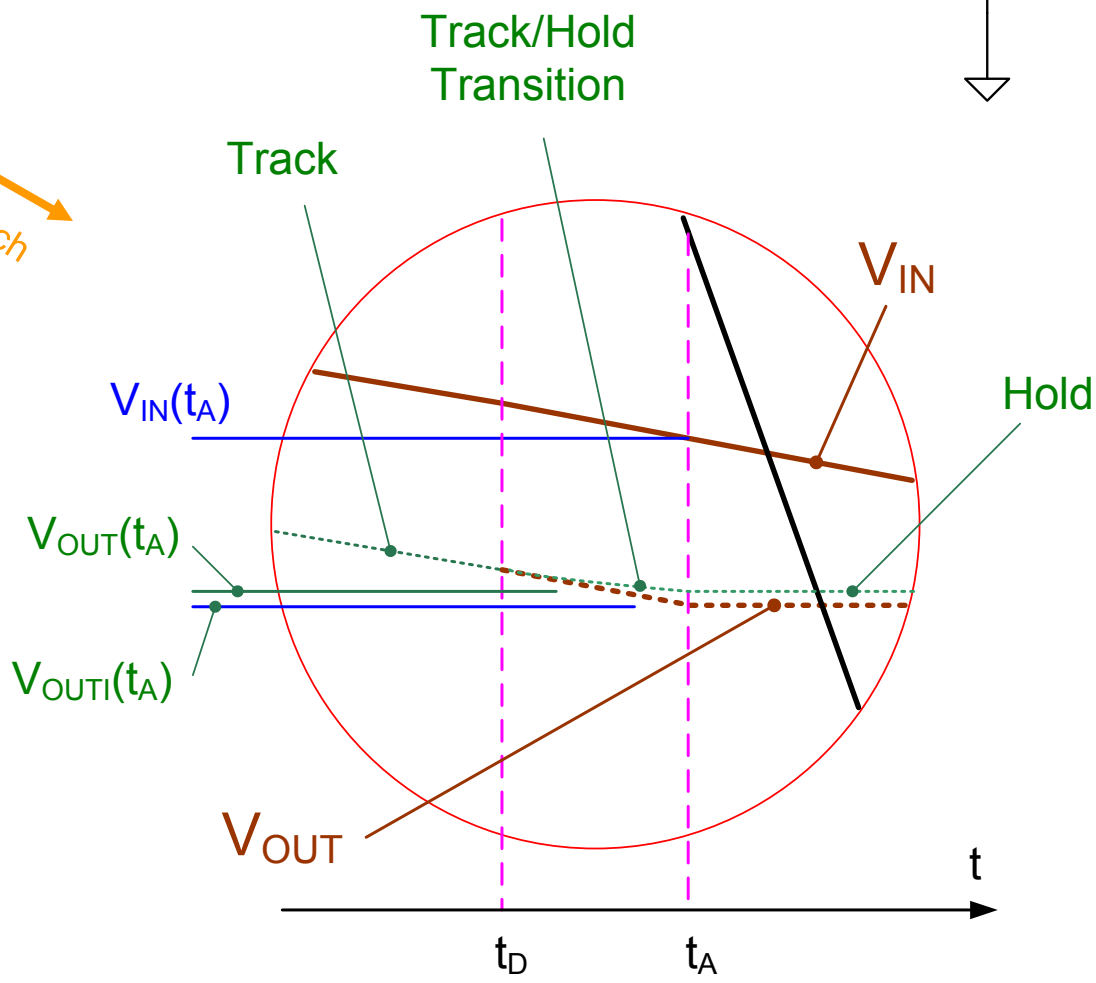
Switch impedance issues



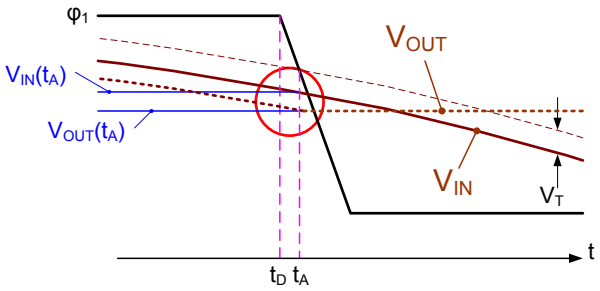


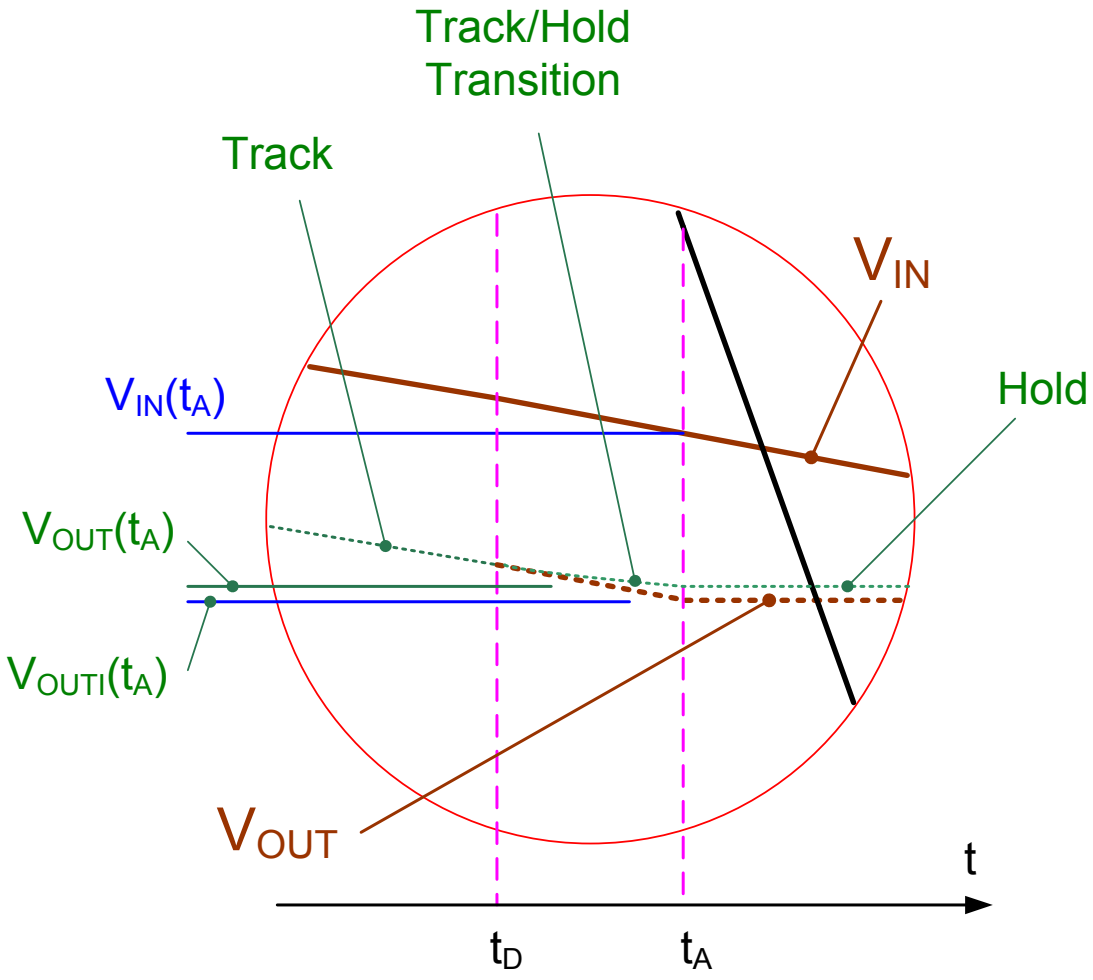
Actual Switch Transition





Switch impedance issues





- Track/Hold Transition usually not of concern if fast fall time on switch
- Switch impedance effects can be managed by making R_{SW} small
- Bottom-plate sampling does not introduce distortion