EE 505

CMOS and BiCMOS Data Conversion Circuits

Course Information:

Lecture Instructor:

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Voice: 294-7745
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WEB: www.randygeiger.org

Laboratory Instructor:

Randy Geiger

Course Information:

CMOS and BiCMOS Data Conversion Circuits

Lecture: MW 2:15-3:35
Online

Labs: W 8:00 – 10:50
Online

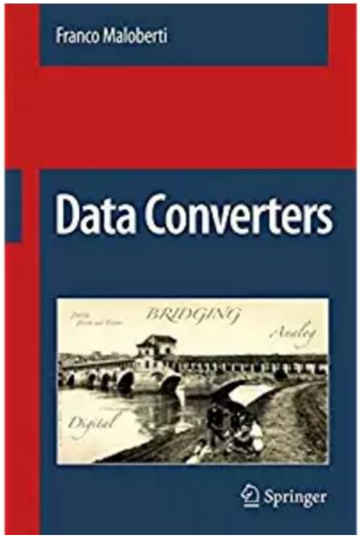
Course WEB Site: http://class.ee.iastate.edu/ee505/

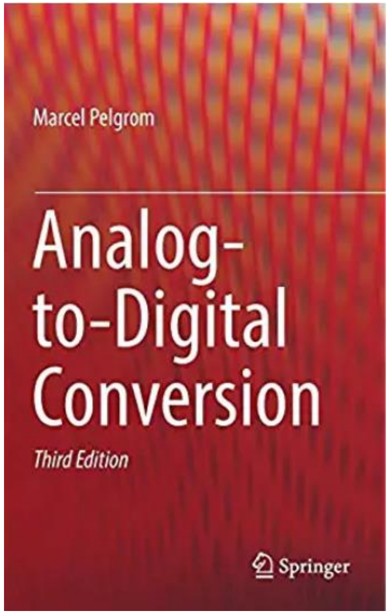
Course Description:

Theory, design and applications of data conversion circuits (A/D and D/A converters) including: architectures, characterization, quantization effects, conversion algorithms, spectral performance, element matching, design for yield, and practical comparators, implementation issues.

Course Information:

Key Reference Texts:



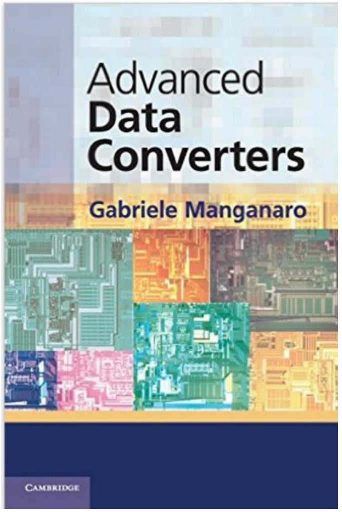


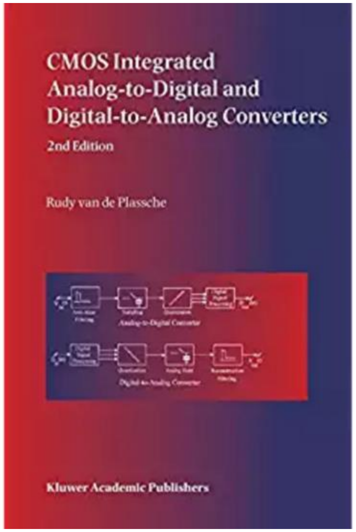
Data Converters, Maloberti, Springer, 2007

Analog-to-Digital Conversion – 3rd Edition by Marcel Pelgrom, Springer, 2016

Course Information:

Other Reference Texts:



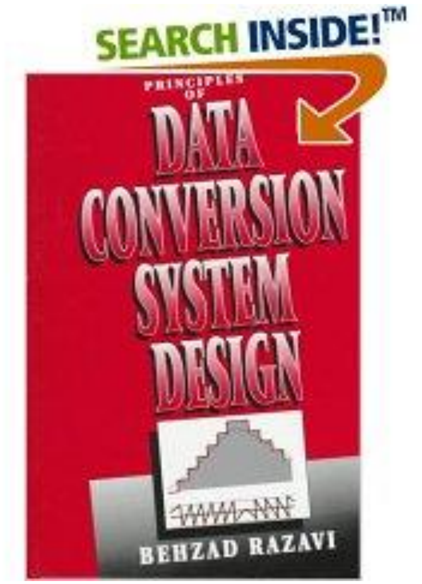


Advanced Data Converters by G. Manganaro, Cambridge, 2012

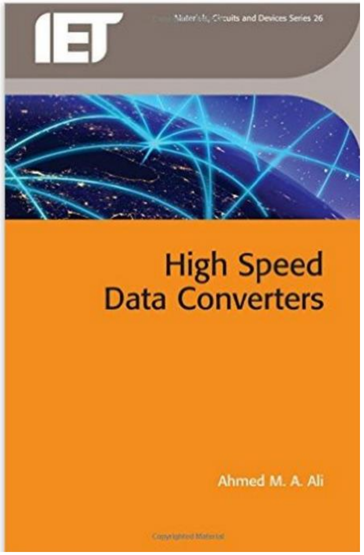
CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters – 2nd Edition by Rudy van de Plassche, Kluwer, 2003

Course Information:

Other Reference Texts:



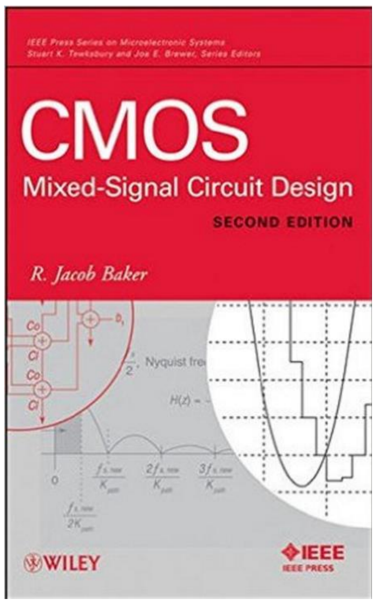
Principles of Data Conversion System Design
by B. Razavi, IEEE Press, 1995



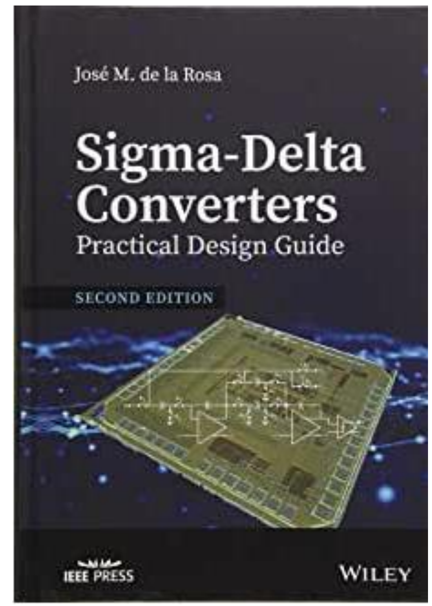
High Speed Data Converters
by A. Ali, IET, 2016

Course Information:

Other Reference Texts:



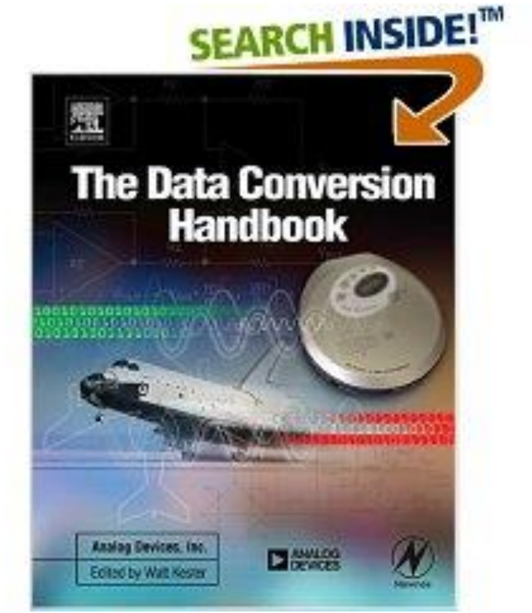
CMOS Mixed-Signal Circuit Design,
2nd Edition, R. Jacob Baker, Wiley, 2008

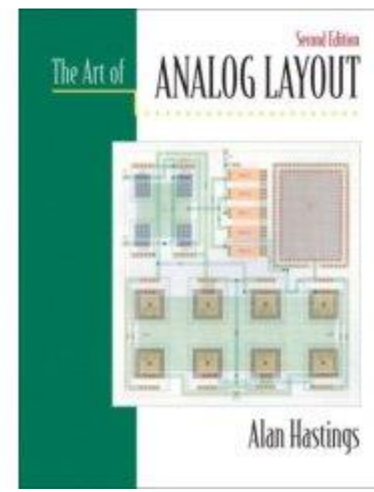


Sigma-Delta Converters – Practical Design Guide,
2nd Edition, J. de la Rosa, Wiley, 2018

Course Information:

Other Reference Texts:



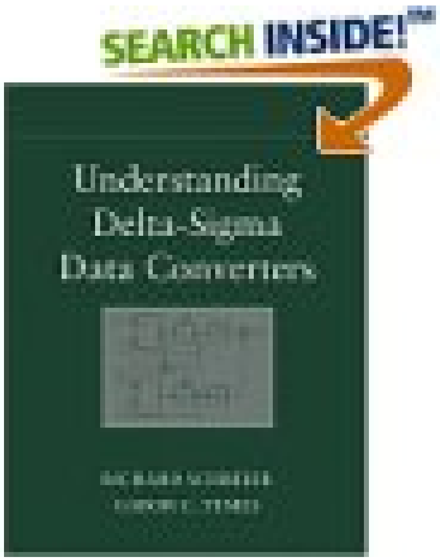


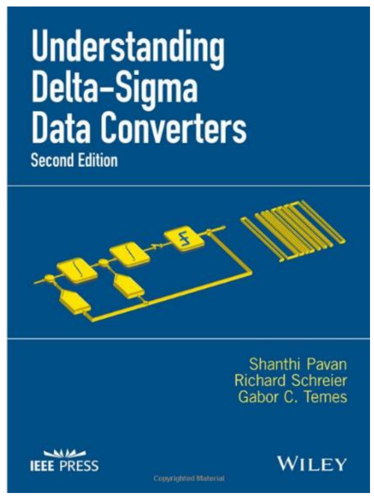
Data Conversion Handbook
by Analog Devices, 2005

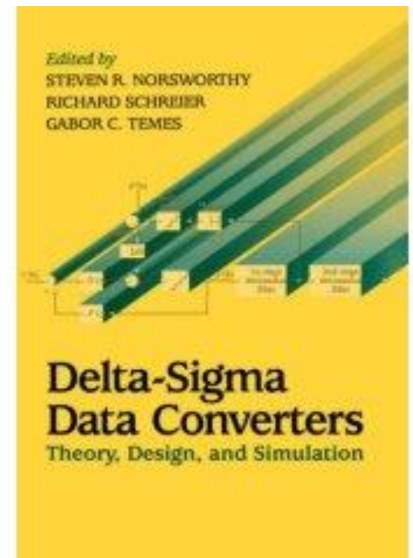
The Art of Analog Layout
by A. Hastings, Prentice Hall, 2001

Course Information:

Other Reference Texts:





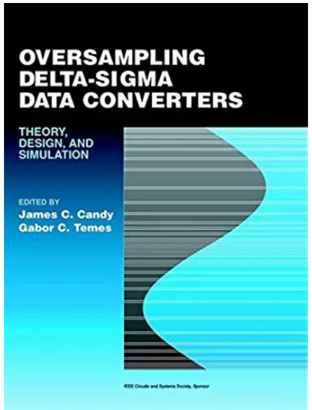


Understanding Delta-Sigma Data Converters
by R. Schreier and G. Temes, Wiley, 2005
by Pavan, Schreier and Temes, Wiley, 2017

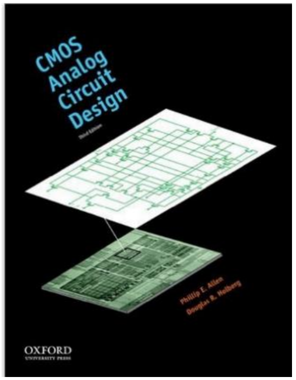
Delta-Sigma Data Converters – Theory, Design, and Simulation
edited by S. Norsworthy, R. Schreier and G. Temes, Wiley, 1997

Course Information:

Reference Texts:



Oversampling Delta-Sigma Data Converters: Theory, Design, and Simulation 1st Edition
By Candy and Temes, 1991.

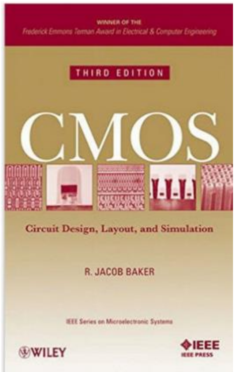


CMOS Analog Circuit Design
by Allen and Holberg, Oxford, 2011.

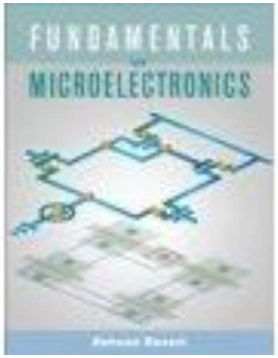
Course Information:

Reference Texts:

CMOS: Circuit Design, Layout, and Simulation – Second Edition by J. Baker, Wiley, 2011.



Fundamentals of Microelectronics
by B. Razavi, McGraw Hill, 2008



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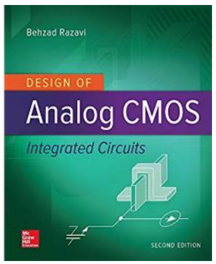
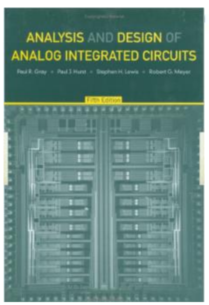
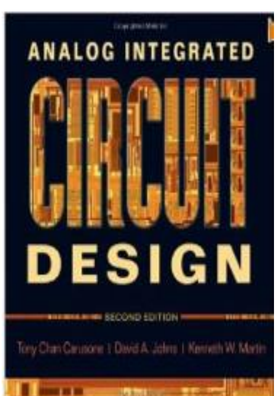


Design of Analog CMOS Integrated Circuits – 2nd edition
by B. Razavi, McGraw Hill, 2016



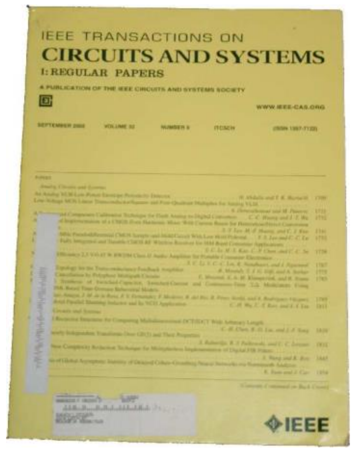
Analysis and Design of Analog Integrated Circuits-Fifth Edition
Gray,Hurst,Lewis and Meyer, Wiley, 2009

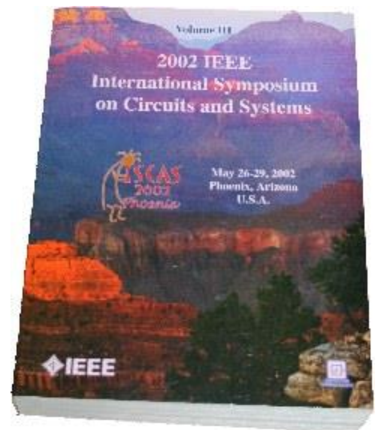


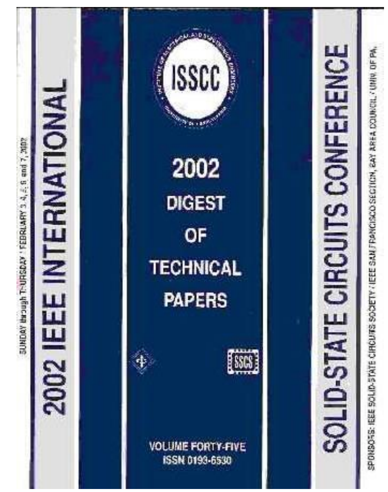
Analog Integrated Circuit Design -2nd Edition
by D. Johns and K. Martin, Wiley, 2011

Course Information:

Reference Materials:







Course Information:

Grading: Points will be allocated for several different parts of the course. A letter grade will be assigned based upon the total points accumulated. The points allocated for different parts of the course are as listed below:

1 Exam	100 pts
1 Final	100 pts.
Homework	100 pts.total
Lab and Lab Reports	100 pts.total
Design Project	100 pts.

Note: In the event that one of the exams is not given, the weight of the remaining exam will be increased to somewhere between 100 pts and 200 pts.

Course Information:

Design Project:

The design project will be assigned by mid-term. Additional details about the design project will be given after relevant material is covered in class. The option will exist to have this project fabricated through the MOSIS program. The design should be ready for fabrication and post-layout simulations are to be included as a part of the project.

Course Information:

E-MAIL:

I encourage you to take advantage of the e-mail system on campus to communicate about any issues that arise in the course. I typically check my e-mail several times a day. Please try to include “EE 505" in the subject field of any e-mail message that you send so that they stand out from what is often large volumes of routine e-mail messages.

Topical Coverage

- Data Converter Operation, Characterization and Specifications
  - Transfer Characteristics
  - Noise
  - Spectral characterization
- Component Matching and Yield
- Nyquist-Rate Data Converter Design
  - DACs
    - Architectures
    - Building Blocks
    - Analysis, Simulation, and Yield
  - ADCs
    - Architectures
    - Building Blocks
    - Analysis, Simulation, and Yield
- Over-Sampled Data Converters
  - Operation
  - Architectures
  - Building Blocks

Signals

Types of signals:

Continuous amplitude vs discrete amplitude

Continuous time vs discrete time

Finite resolution vs infinite resolution

Probability of any continuous-amplitude signal value being exactly equal to a specific value is 0

Probability of any time being exactly equal to a specific time value is 0

If x is a continuous variable (time, voltage, current,….) then in the context of data converters, there is no distinction in the following sets of numbers

$$(x_1,x_2) \quad [x_1,x_2] \quad (x_1,x_2] \quad [x_1,x_2)$$

It may be more convenient to include boundary points when using programs such as Matlab to characterize data converters but results should not depend upon whether end points are included or excluded

Signals

Digital representations (many exist)

unary (thermometer), binary, decimal, gray (RBC),BCD, hexadecimal,……

In the context of data converters, the digital representation is almost always represented by sets whose elements are {0,1}

Binary and occasionally unary are invariable the codes that are used when building ADCs and DACs

Unless specifically stated to the contrary, it will be assumed throughout this course that the input or output codes in a data converter are binary

Data Converters

Types:

A/D (Analog to Digital)

Converts Analog Input to a Digital Output

D/A (Digital to Analog)

Converts a Digital Input to an Analog Output

A/D is the world's most widely used mixed-signal component

D/A is often included in a FB path of an A/D

A/D and D/A fields will remain hot indefinitely

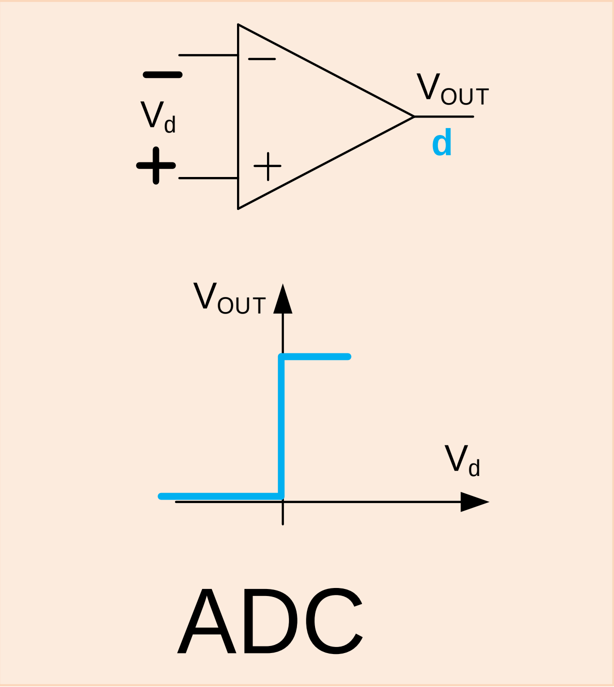
- technology advances make data converter design more challenging
- embedded applications
- designs often very application dependent

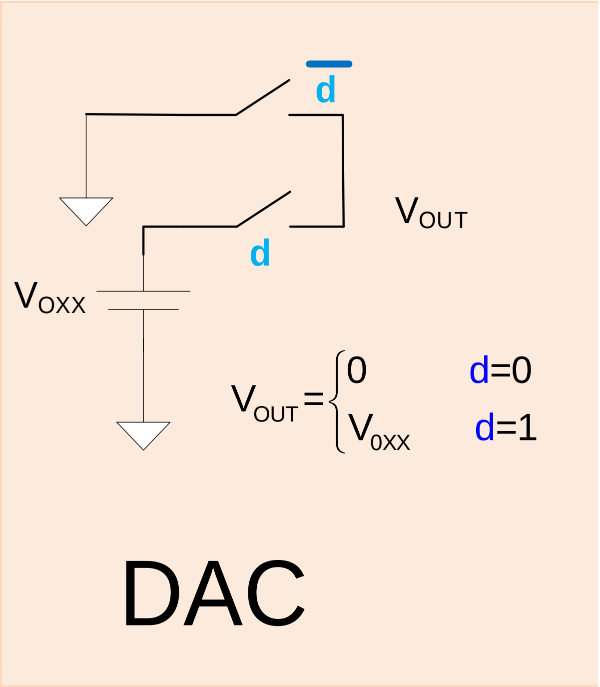
Data Converters

- Data converters are ratio-metric devices and outputs are all relative to a reference (i.e. traceability to a primary or secondary standard is not an issue)
- Can be thought of as an amplifier where the output is a ratio-metric version of the input
- Units of output of ADC are dimensionless and units of input to DAC are dimensionless
- Units of input to ADC can be arbitrary and units of output of DAC can be arbitrary

Data Converters

Electronic Data Conversion Process:

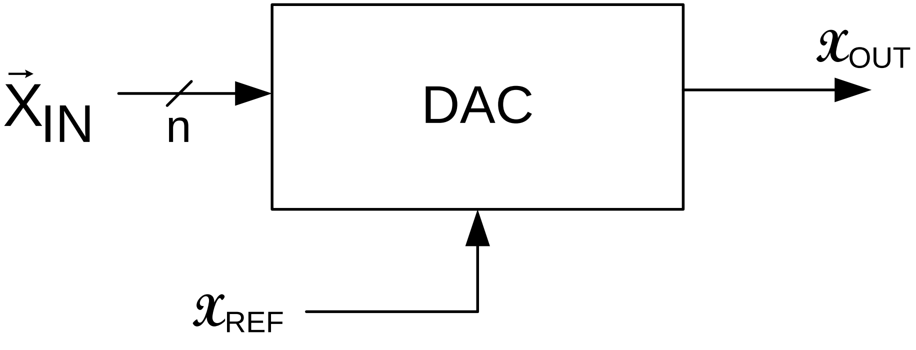




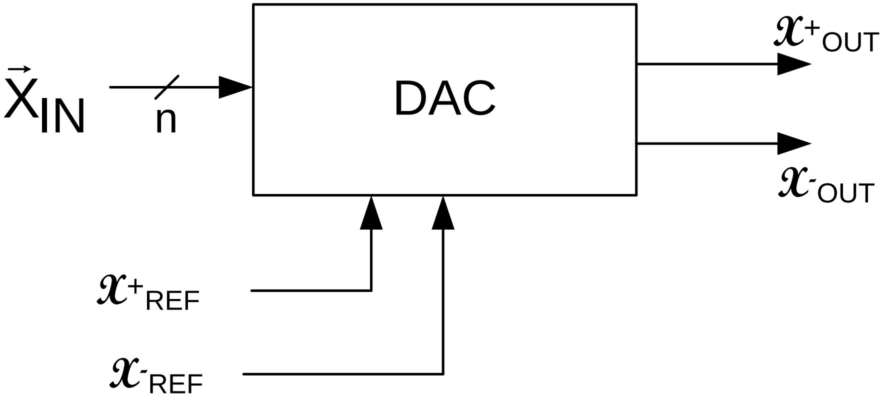
- The comparator is the basic analog to digital conversion element in all ADCs
- The switch is the basic digital to analog conversion element in all DACs
- Data converters incorporate one or more basic ADC or DAC cells
- Design of comparator or switch is often critical in data converters
- Performance of data converters often dependent upon performance of comparator, switch, and matching

D/A Converters

Basic structure:

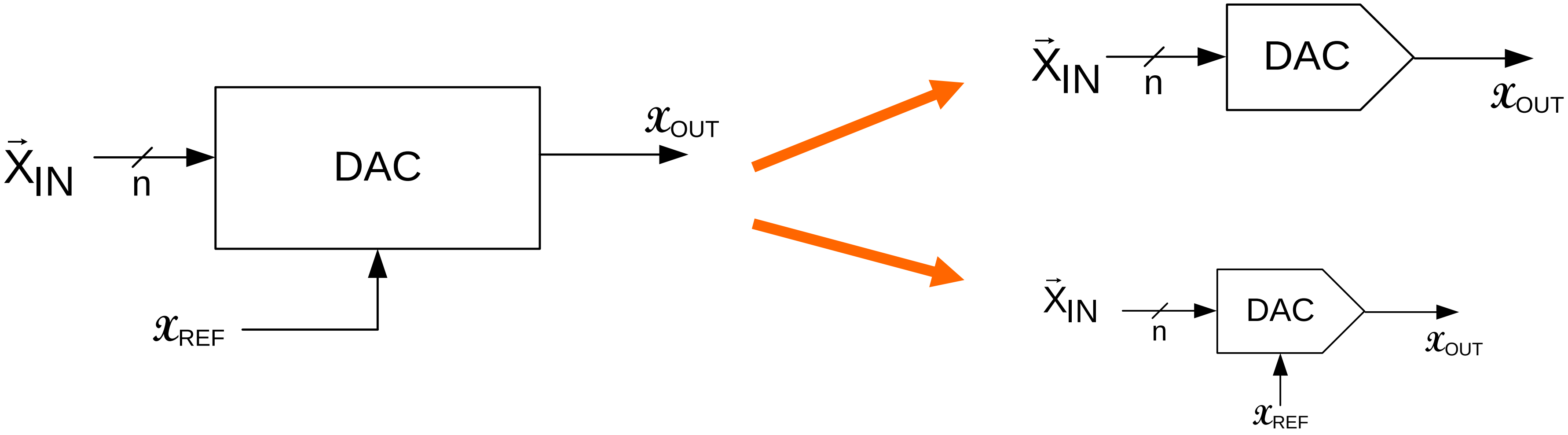


Basic structure with differential outputs::



D/A Converters

Notation:



Reference always exists even in not explicitly shown

D/A Converters

(assuming binary coding)

$$\vec{X}_{IN} = <b_{n-1}, b_{n-1}, \ldots b_1, b_0>$$

b_0 is the Least Significant Bit (LSB)

b_{n-1} is the Most Significant Bit (MSB)

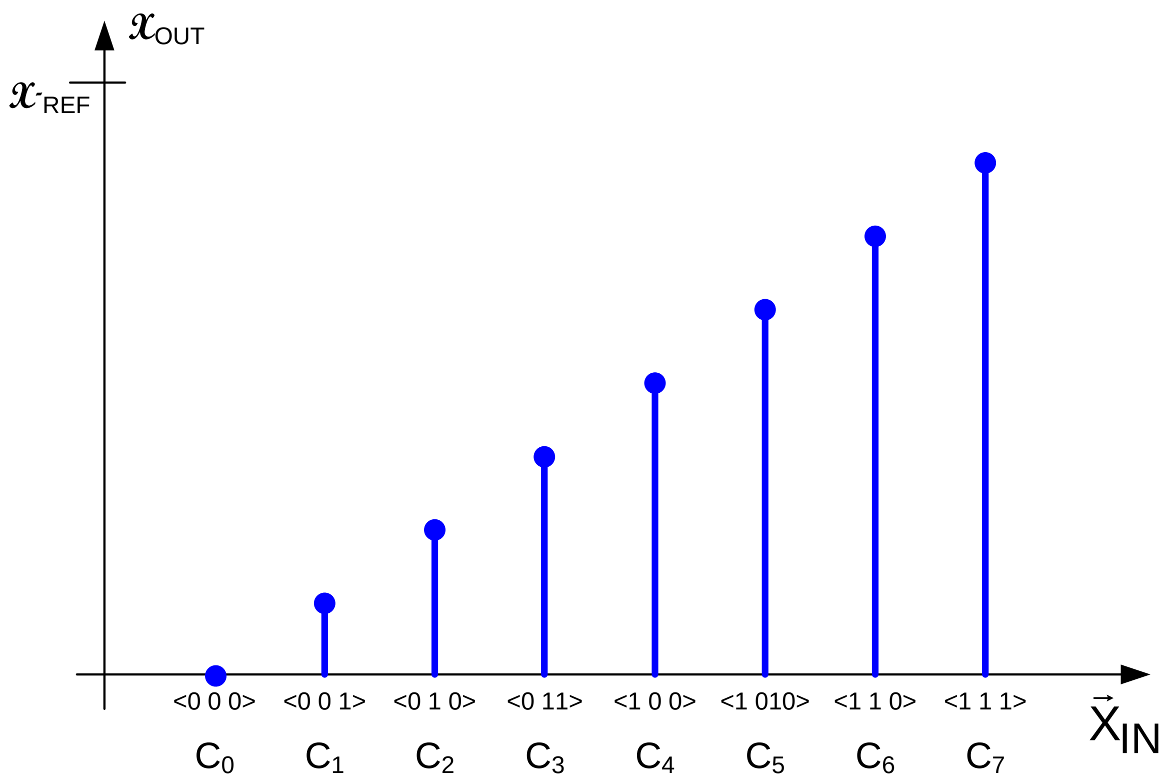
Note: some authors use different index notation

An Ideal DAC is characterized at low frequencies by its static performance

D/A Converters

$$\vec{X}_{IN}=<b_{n-1},b_{n-1},\ldots b_1,b_0>$$

<u>An</u> Ideal DAC transfer characteristic (3-bits) (Nyquist Rate)

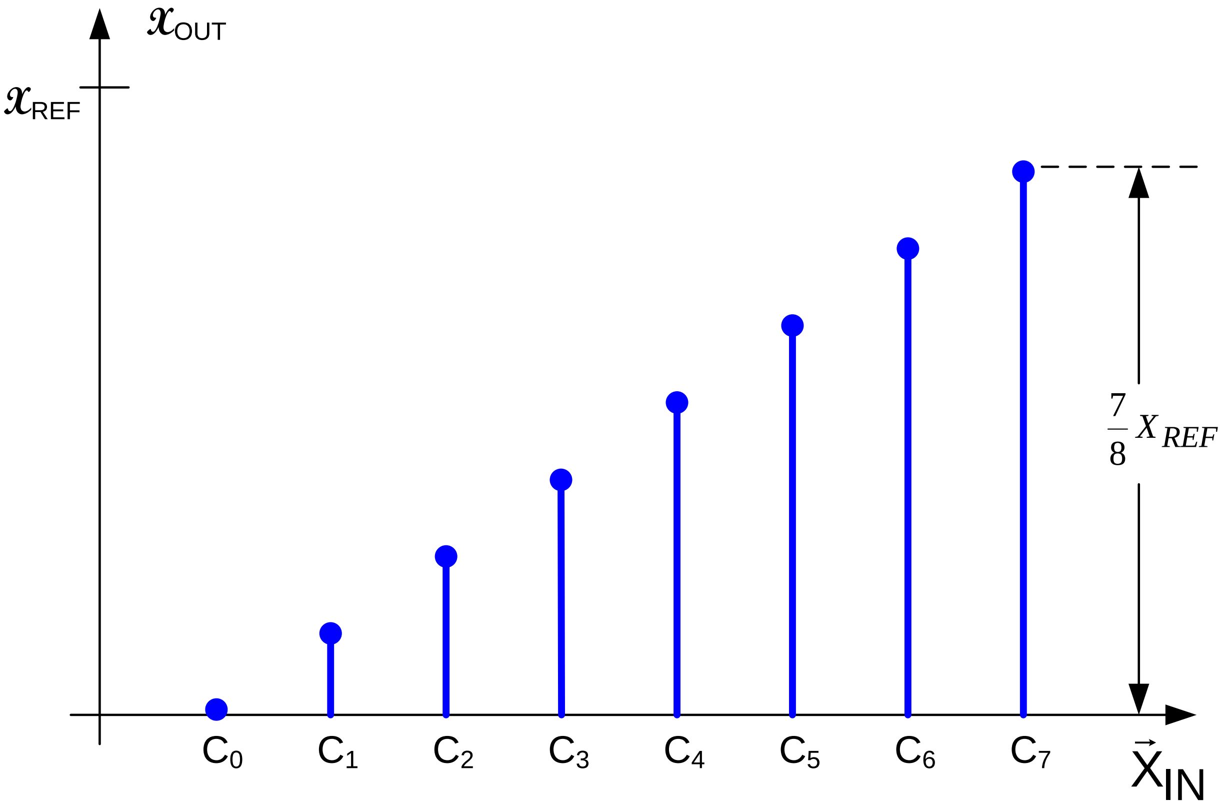


Code C_k is used to represent the decimal equivalent of the binary number $<b_{n-1} .. b_0)>$

D/A Converters

$\vec{X}_{IN}$=<b_{n-1},b_{n-1},…b_1,b_0>

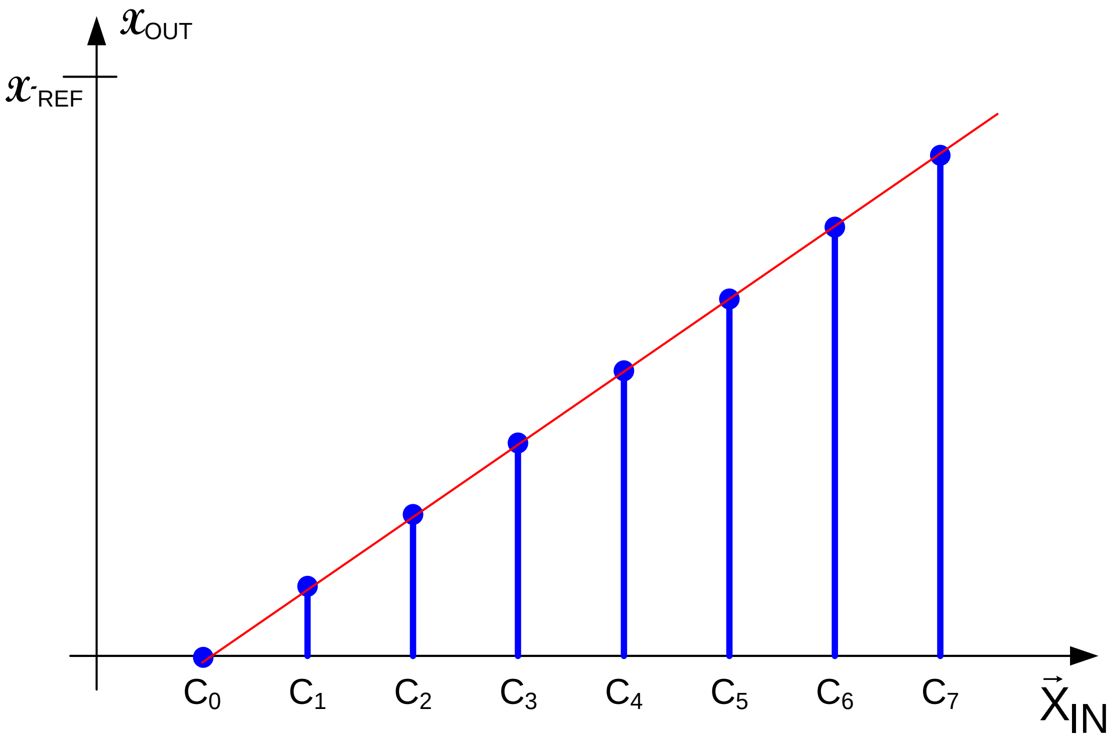
An Ideal DAC transfer characteristic (3-bits)



D/A Converters

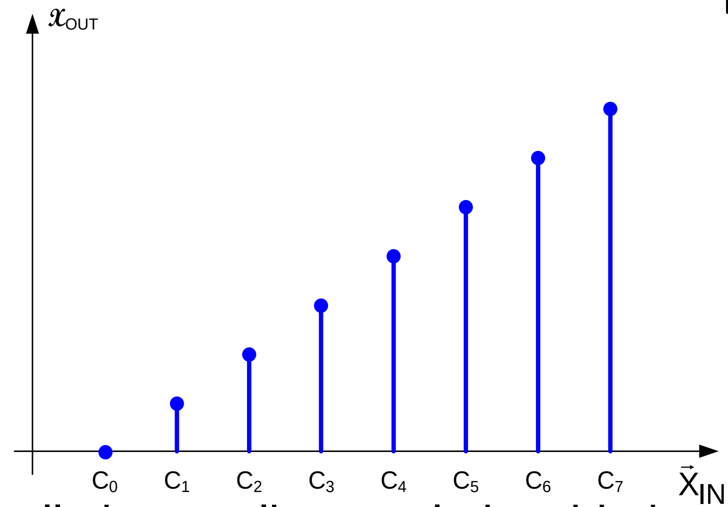
$$\vec{X}_{IN} = \langle b_{n-1}, b_{n-1}, \ldots b_1, b_0 \rangle$$

An Ideal DAC transfer characteristic (3-bits)



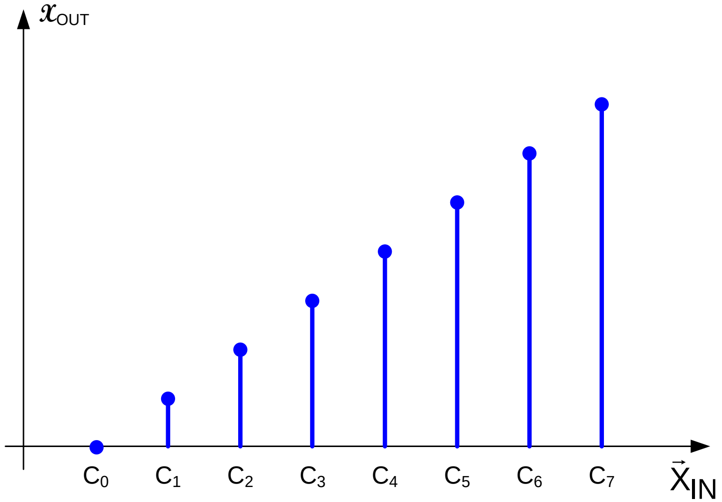
All points of this ideal DAC lie on a straight line

D/A Converters



- Most D/A ideally have a linear relationship between binary input and analog output
- Output represents a discrete set of continuous variables
- Typically this number, N, is an integral power of 2, i.e. $N=2^n$
- $\vec{X}_{IN}$ is always dimensionless
- x_{OUT} could have many different dimensions
- An ideal nonlinear characteristic is also possible (waveform generation and companding)
- Will assume a linear transfer characteristic is desired unless specifically stated to the contrary

D/A Converters



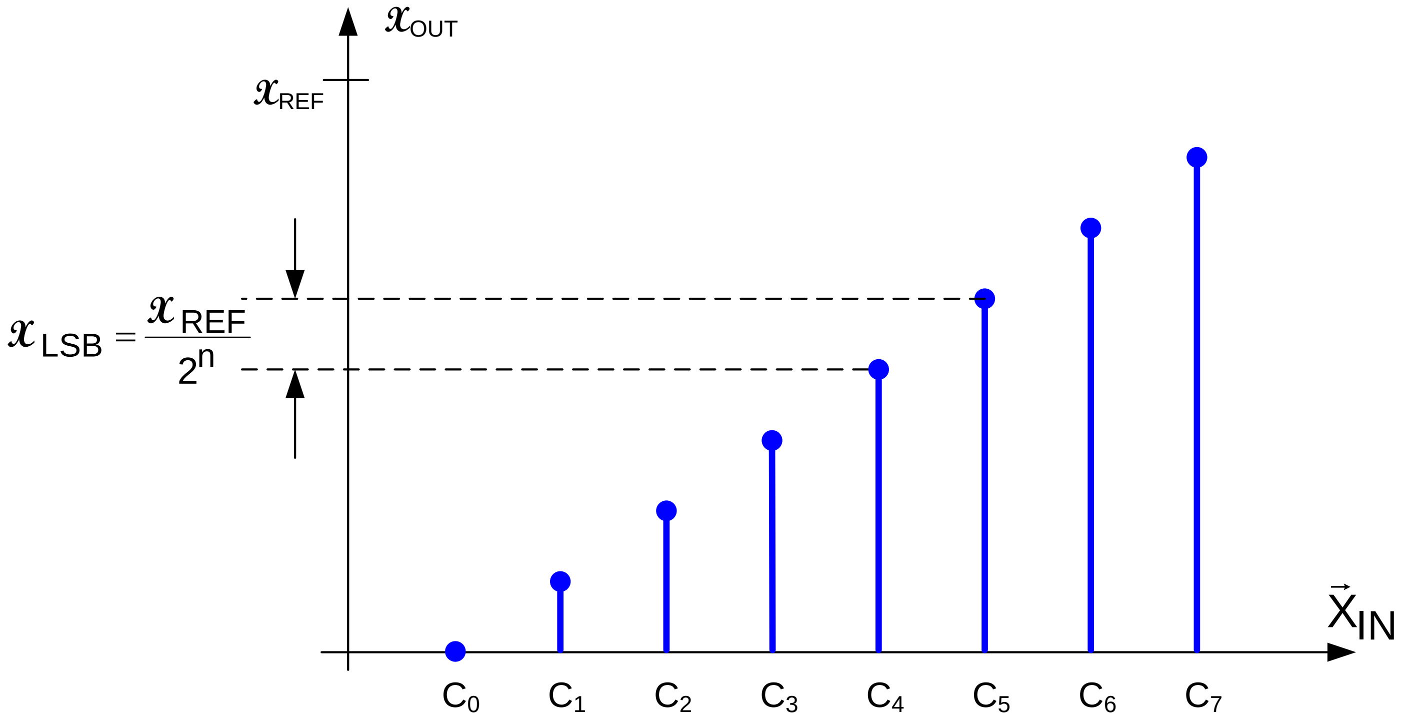
For this ideal DAC

$$X_{OUT} = X_{REF}\left(\frac{b_{n-1}}{2}+\frac{b_{n-2}}{4}+\frac{b_{n-3}}{8}+\ldots+\frac{b_1}{2^{n-1}}+\frac{b_0}{2^n}\right)$$

$$X_{OUT} = X_{REF}\sum_{j=1}^{n}\frac{b_{n-j}}{2^j}$$

- Number of outputs gets very large for n large
- Spacing between outputs is $X_{REF}/2^n$ and gets very small (relative to X_{REF}) for n large

D/A Converters

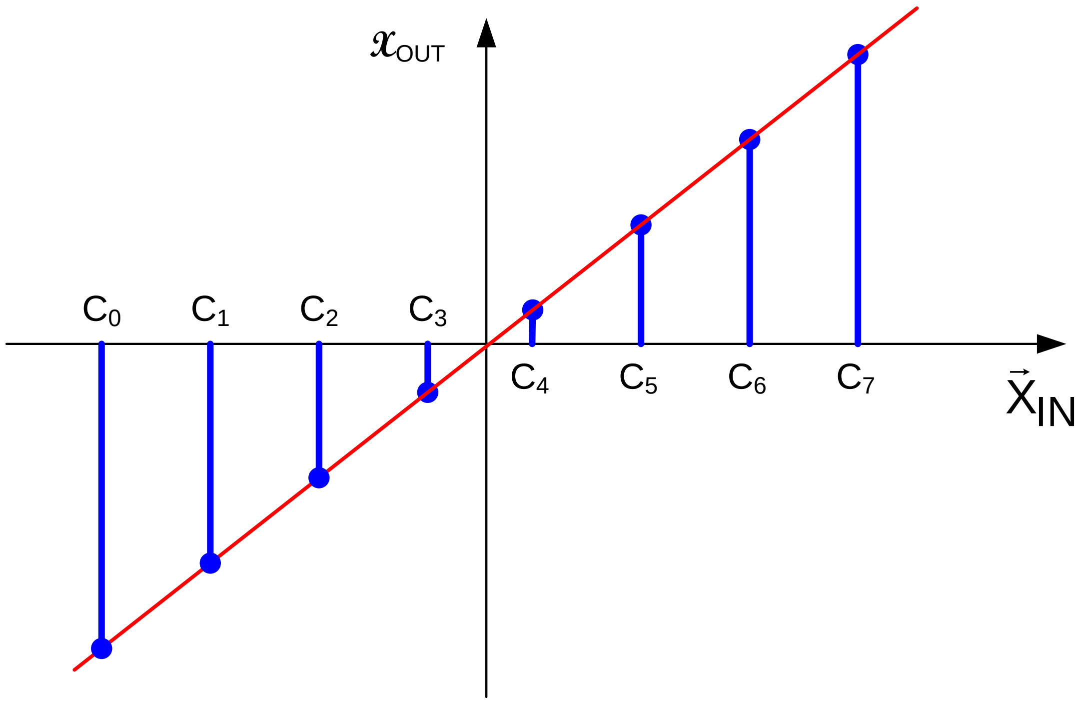


- Ideal steps all equal and termed the LSB
- x_{LSB} gets very small for small x_{REF} and large n

e.g. If x_{REF}=1V and n=16, then N=2^{16} =65,536, x_{LSB}=15.25μV

D/A Converters

An alternate ideal 3-bit DAC



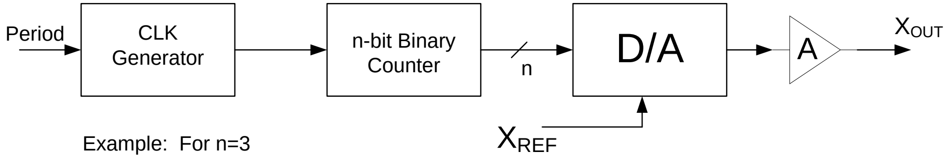
Irrespective of which form is considered, the increment in the output for one Boolean bit change in the input is $\mathcal{X}_{LSB}$ and the total range is 1LSB less than $\mathcal{X}_{REF}$

Applications of DACs

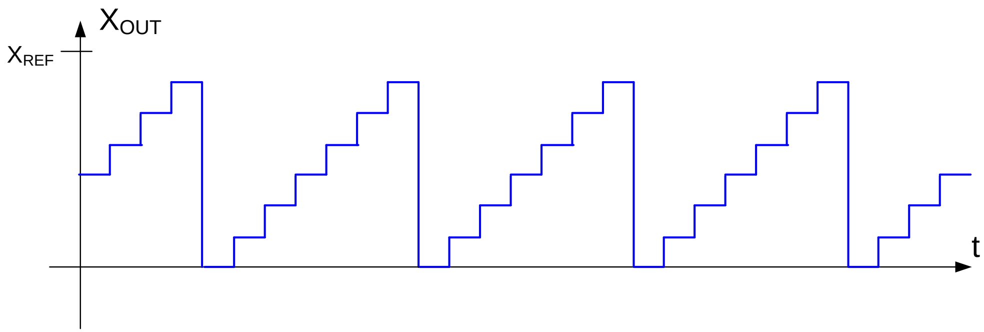
- Waveform Generation
- Voltage Generation
- Analog Trim or Calibration
- Industrial Control Systems
- Feedback Element in ADCs
- ….

Waveform Generation with DACs

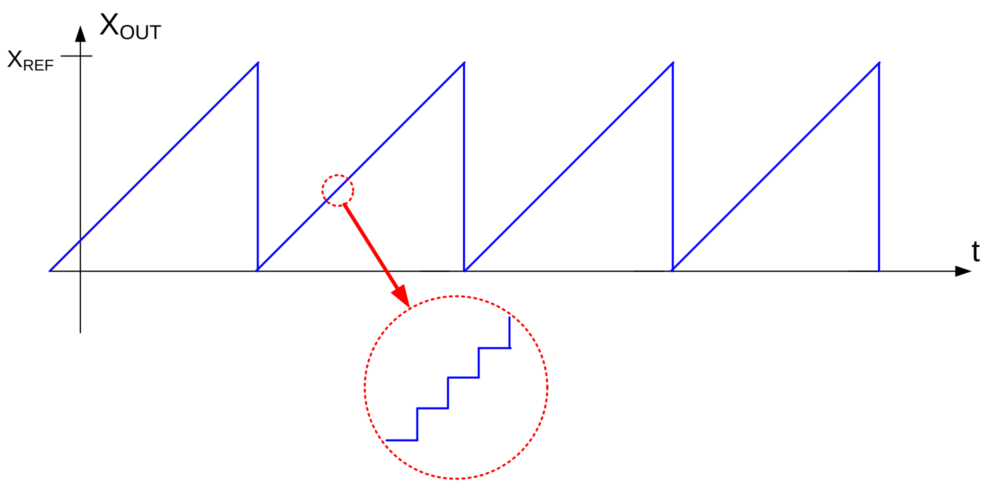
Ramp (Saw-tooth) Generator



Example: For n=3

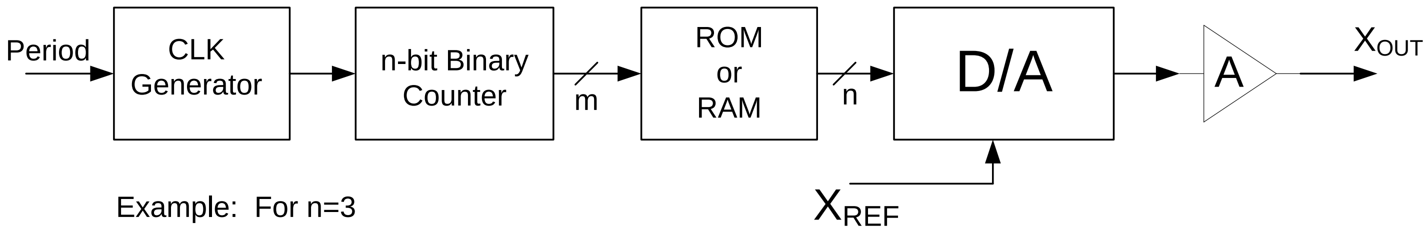


Example: For large n

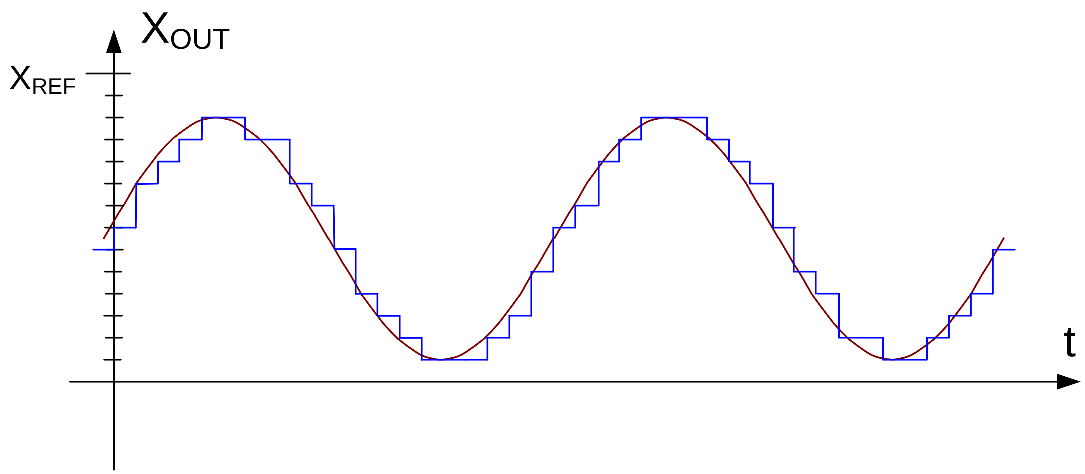


Waveform Generation with DACs

Sine Wave Generator



Example: For n=3

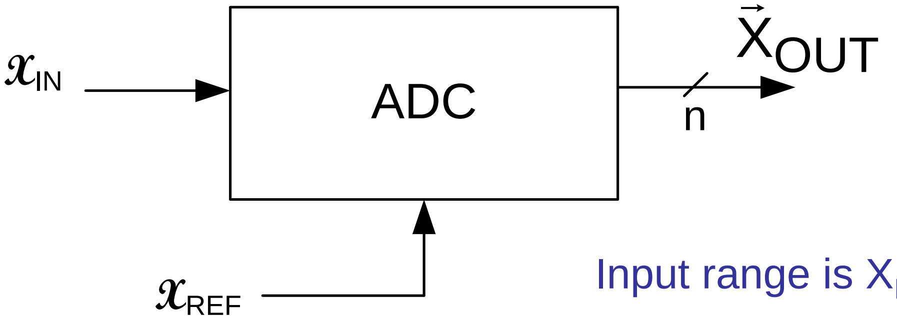


Distortion of the desired waveforms occurs due to both time and amplitude quantization

Often a filter precedes or follows the buffer amplifier to smooth the output waveform

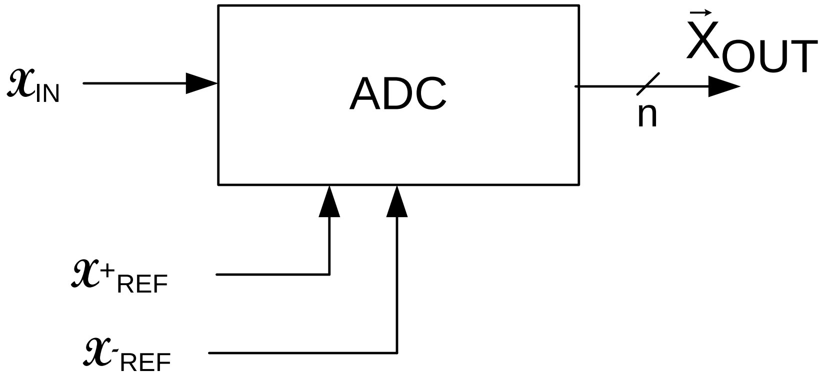
A/D Converters

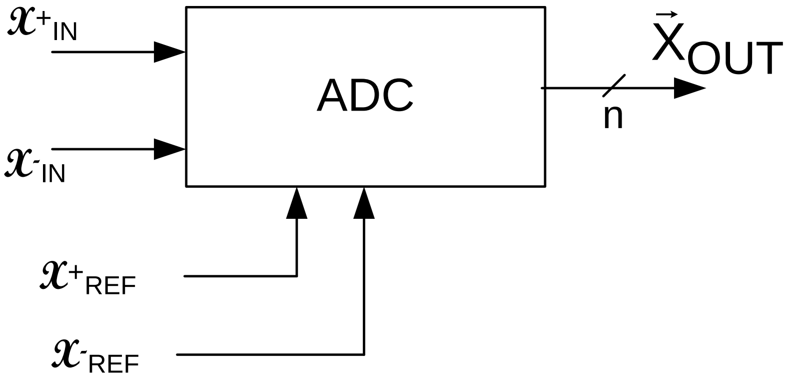
Basic structure:



Input range is X_{REF}

Basic structure with differential inputs/references:



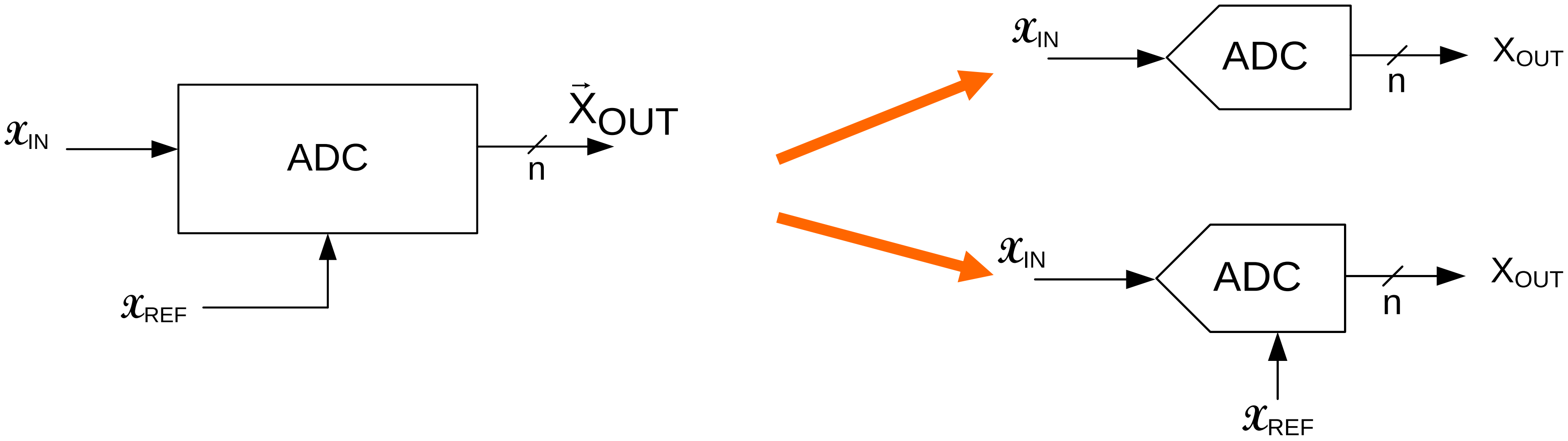


Input range is $X^+_{REF} - X^-_{REF}$

Typically Input range is $2(X^+_{REF} - X^-_{REF})$

A/D Converters

Notation:



Reference always exists even in not explicitly shown

A/D Converters

(assuming binary coding)

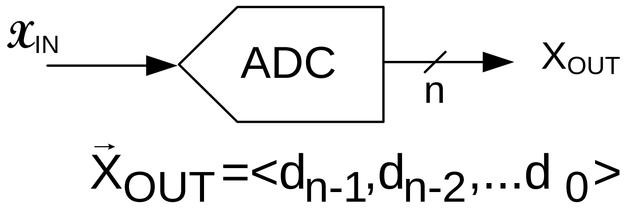
$$\vec{X}_{OUT} = <d_{n-1}, d_{n-2}, \ldots d_0>$$

d_0 is the Least Significant Bit (LSB)

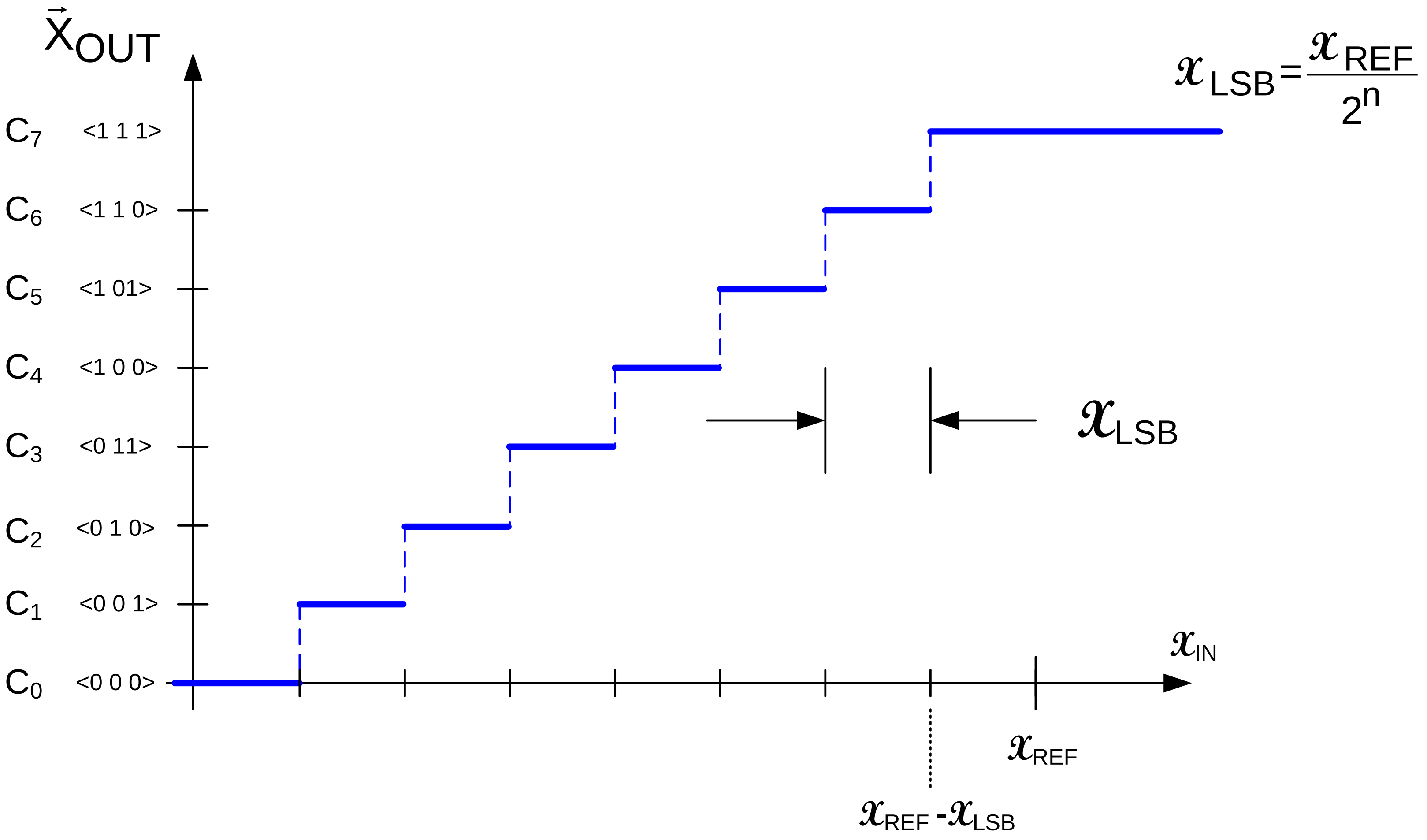
d_{n-1} is the Most Significant Bit (MSB)

An Ideal ADC is characterized at low frequencies by its static performance

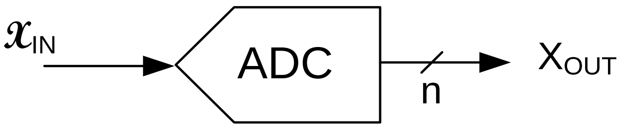
A/D Converters



An Ideal ADC transfer characteristic (3-bits) (Nyquist Rate)



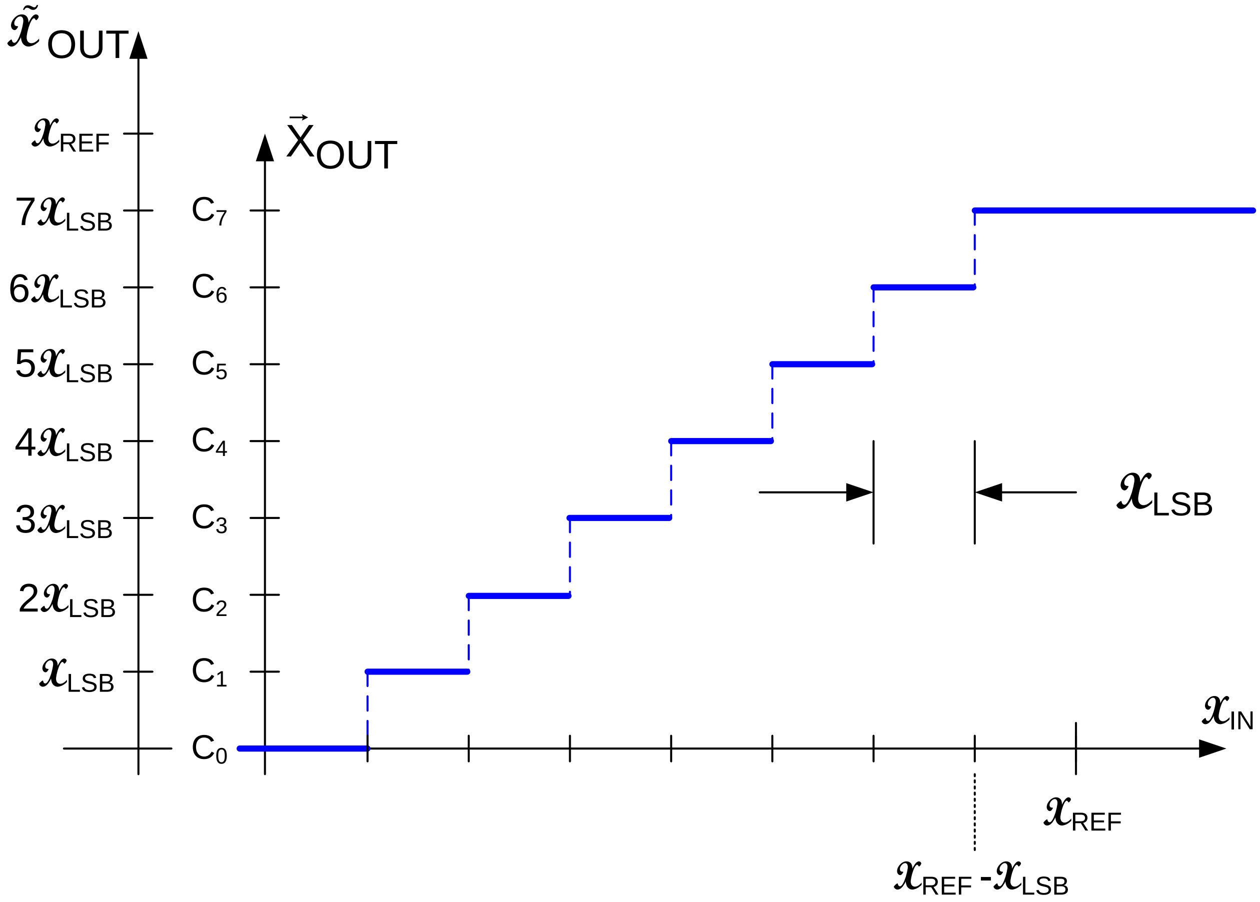
A/D Converters



$\vec{X}_{OUT} = <d_{n-1}, d_{n-2}, \ldots d_0>$

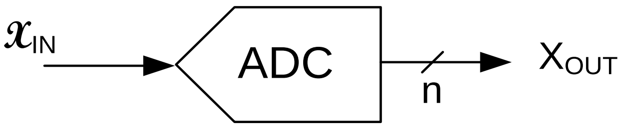
An Ideal ADC transfer characteristic (3-bits)

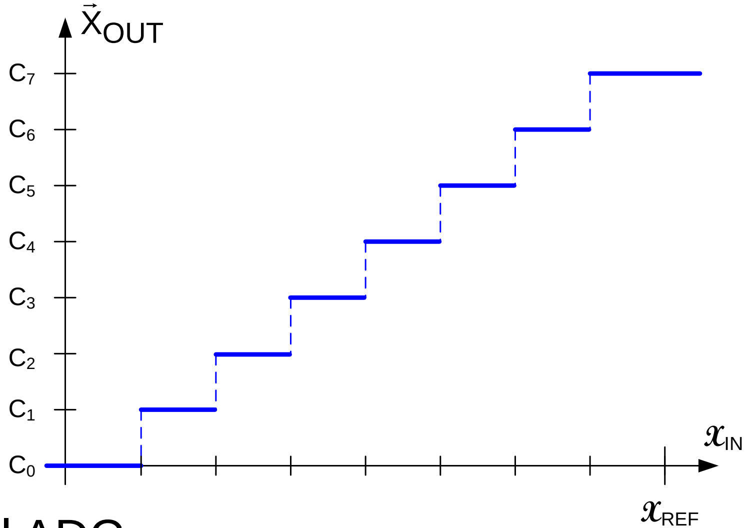
$$x_{LSB} = \frac{x_{REF}}{2^n}$$



The second vertical axis, labeled $\tilde{x}_{OUT}$ is the interpreted value of x_{IN}

A/D Converters





For this ideal ADC

$$\tilde{x}_{OUT} = x_{REF}\left(\frac{d_{n-1}}{2} + \frac{d_{n-2}}{4} + \frac{d_{n-3}}{8} + \ldots + \frac{d_1}{2^{n-1}} + \frac{d_0}{2^n}\right)$$

$$\tilde{x}_{OUT} - x_{IN} = \varepsilon$$

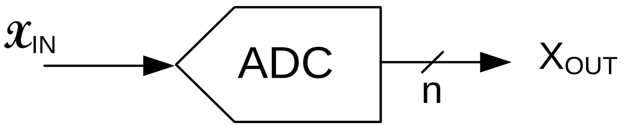
where ε is small (typically less than 1LSB)

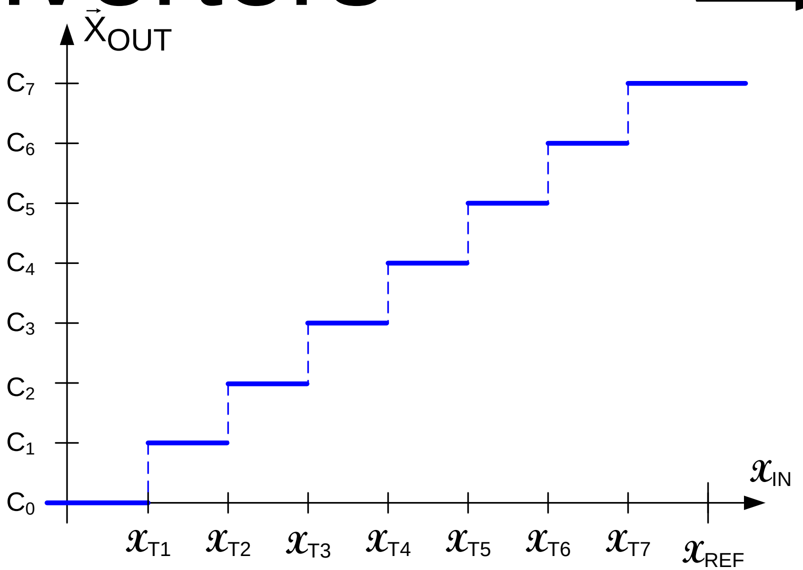
$$x_{IN} = x_{REF}\sum_{j=1}^{n}\frac{d_{n-j}}{2^j} - \varepsilon$$

- Number of bins gets very large for n large
- Spacing between break points is $x_{REF}/2^n$ and gets very small for n large

ε is the **quantization error** and is inherent in any ADC

A/D Converters





Transition Points

- Actual values of x_{IN} where transitions occur are termed transition points or break points
- For an ideal n-bit ADC, there are 2^n-1 transition points
- Ideally the transition points are all separated by 1 LSB -- $X_{LSB}=X_{REF}/2^n$
- Ideally the transition points are uniformly spaced
- In an actual ADC, the transition points will deviate a little from their ideal location

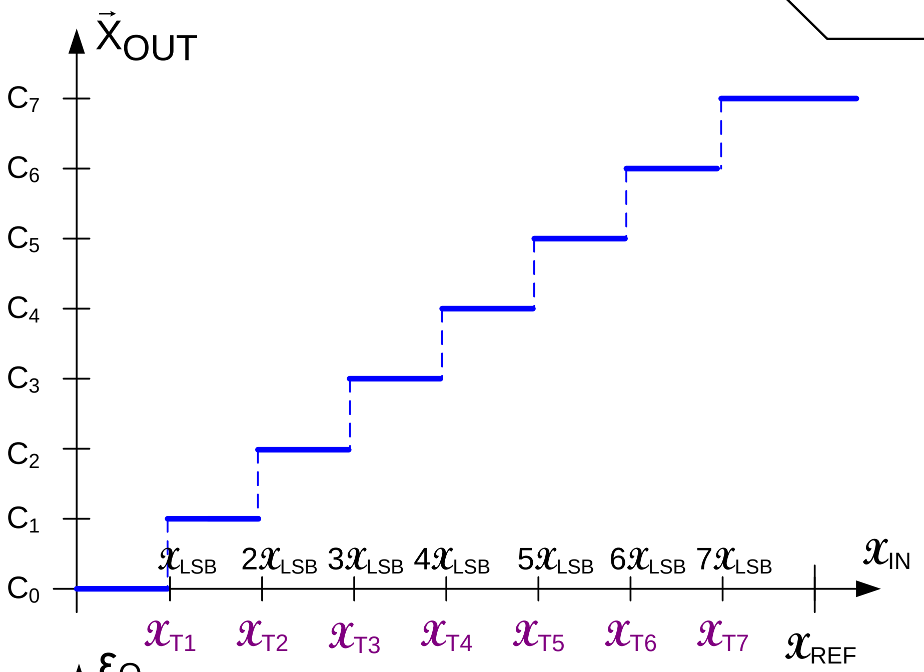
Labeling Convention: We will define the transition point X_{Tk} to be the break point where the transition in the code output to code C_k occurs. This seemingly obvious ordering of break points becomes ambiguous, though, when more than one break points cause a transition to code C_k which can occur in some nonideal ADCs

A/D Converters

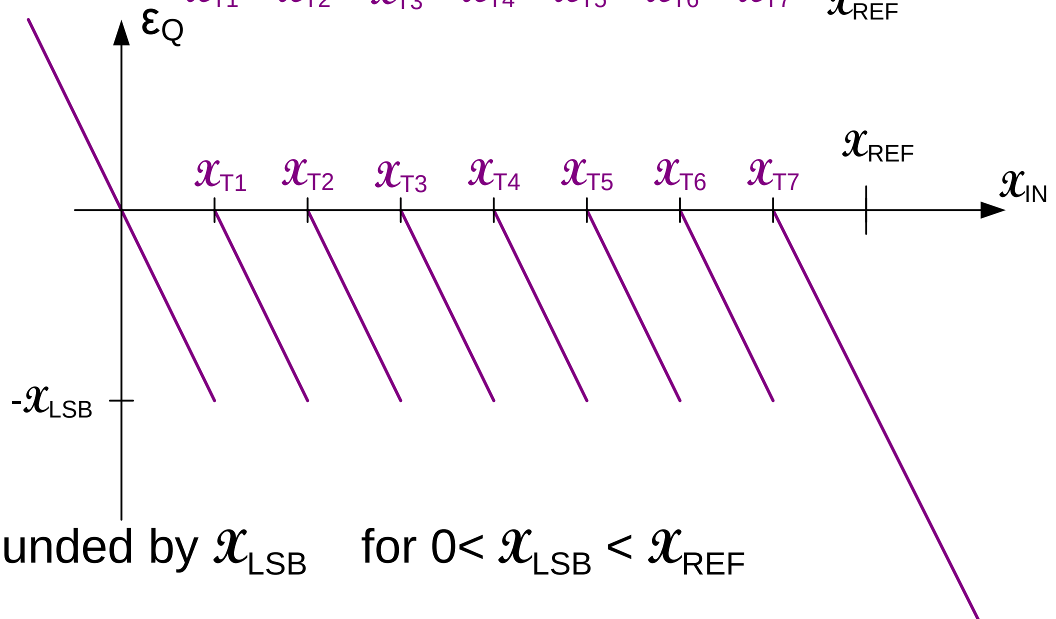
Quantization Errors

An ideal ADC

$x_{T1}=x_{LSB}$



$\varepsilon_Q = \tilde{x}_{OUT} - x_{IN}$



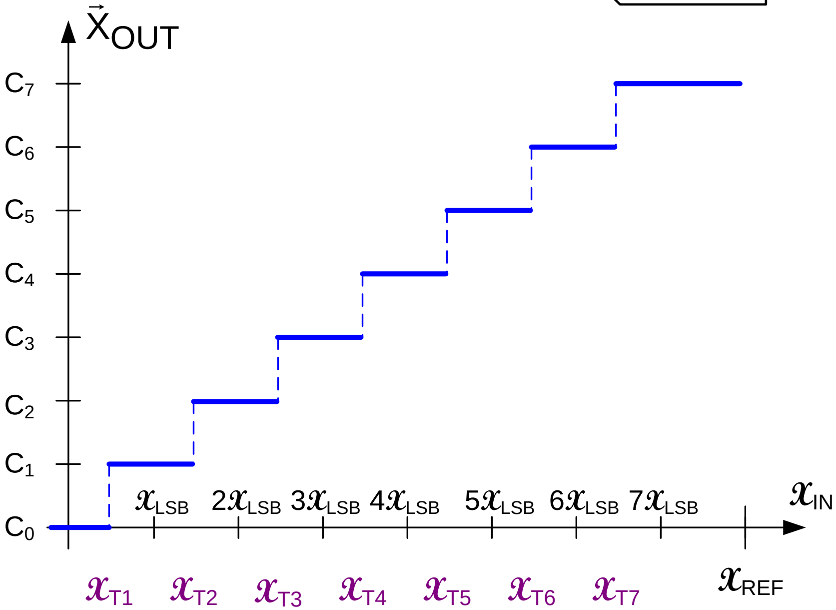
Magnitude of ε_Q bounded by x_{LSB} for $0< x_{LSB} < x_{REF}$

A/D Converters

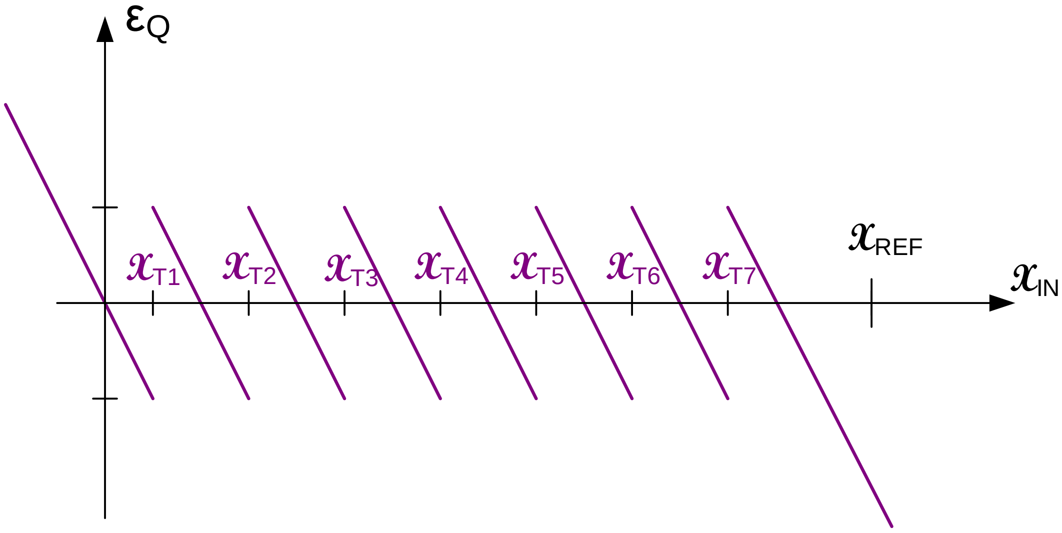
Quantization Errors

Another Ideal ADC

$x_{T1}=x_{LSB}/2$

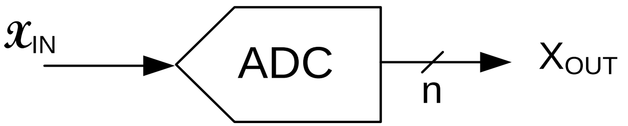


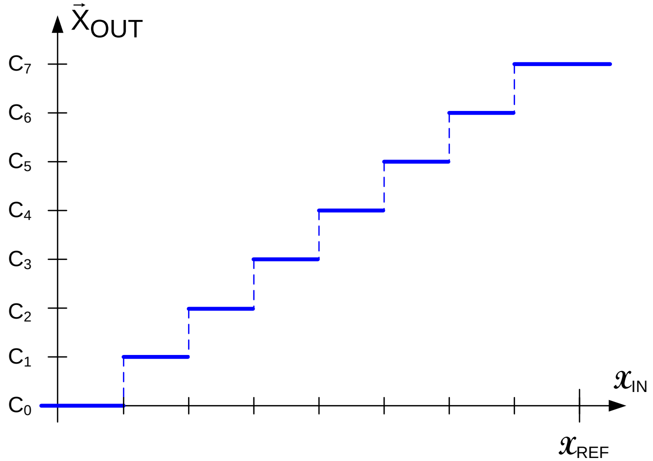
$\varepsilon_Q = \tilde{x}_{OUT} - x_{IN}$



Magnitude of ε_Q bounded by ½ x_{LSB}

A/D Converters





Quantization Errors

$$\varepsilon_Q = x_{REF}\left(\frac{d_{n-1}}{2}+\frac{d_{n-2}}{4}+\frac{d_{n-3}}{8}+\ldots+\frac{d_1}{2^{n-1}}+\frac{d_0}{2^n}\right) - x_{IN}$$

- The only way to reduce p-p quantization errors is to increase number of levels
- A lower bound on the quantization errors in $0 < x_{IN} < x_{REF}$ is $\pm\frac{1}{2}\, x_{LSB}$
- The static performance of an ADC is completely determined by the finite sequence of the transition points < x_{T1} , … x_{T1}>

A/D Converters

Many types:

- Successive Approximation Register (SAR)
- Pipelined
- Sigma-Delta
- Flash
- Single-slope
- Dual-slope

Wide ranges of performance:

- Speed
- Resolution
- Power
- Cost

Large number of vendors of catalog parts:

- Texas Instruments
- Analog Devices (Linear Technology)
- Maxim
- …

Embedded applications probably much larger:

- Many SoCs contain a large number of data converters of with varying performance

A/D Converters

What types are really used?

Consider catalog parts from one vendor – Analog Devices (Jan 2017)

Flash	2
SAR	233
Pipelined	242
Sigma-Delta	81
Total	559

What do ADCs cost?

A/D Converters

Maximize Filters | Sort by Newest | Choose Parameters | Reset Table | Download to Excel | Help

Part #	Hardware	ADC Resolution (bits)	ADC Output Sample Rate	ADC Channels	Device Architecture	US Price 1000 to 4999 ($ US)	INL in LSB (typ) (LSBs)	Vin Range (typ) (V p-p)	ADC SNR in dBFS (typ) (dBFS)	Power Dissipation (typ) (W)
	0 Values...	16 Values...	16.6 - 2.5G	13 Value...	7 Values S...	0.95 - 916.5	0.1 - 33.55	0.078 - 40	47 - 107.8	21u - 4.2
AD7492-5		12	1.25M	-	SAR	**	-	-	-	16.5m
AD7170		12	125	1	Sigma-Delta	$0.95	-	-	-	150µ
AD7478	-	8	1M	1	SAR	$0.96	-	5.25	-	17.5m
AD7478A	-	8	1.2M	1	SAR	$1.12	-	5.25	-	17.5m
AD7171		16	125	1	Sigma-Delta	$1.15	-	-	-	150µ
AD7999	-	8	140k	4	SAR	$1.35	-	5.5	-	4.7m
AD7468		8	320k	1	SAR	$1.35	-	3.6	-	570µ
AD7091		12	1M	1	SAR	$1.60	-	5.25	-	2.4m
AD7904		8	1M	4	SAR	$1.68	-	5.1	-	13.5m
AD7910		10	250k	1	SAR	$1.77	-	5.25	-	15m
AD7995		10	140k	4	SAR	$1.80	-	5.5	-	4.4m
AD7276		12	3M	1	SAR	$1.85	-	3.6	-	19.8m
AD7908	-	8	1M	8	SAR	$1.87	-	5.05	-	13.5m

What do ADCs cost?

A/D Converters

Maximize Filters | Sort by Newest | Choose Parameters | Reset Table | Download to Excel | Help

Part #	Hardware	ADC Resolution (bits)	ADC Output Sample Rate	ADC Channels	Device Architecture	US Price 1000 to 4999 ($ US)	INL in LSB (typ) (LSBs)	Vin Range (typ) (V p-p)	ADC SNR in dBFS (typ) (dBFS)	Power Dissipation (typ) (W)
	0 Values...	16 Values...	16.6 - 2.5G	13 Value...	7 Values S...	0.95 - 916.5	0.1 - 33.55	0.078 - 40	47 - 107.8	21u - 4.2
AD10465		14	65M	2	Pipelined	$916.53	-	4	-	3.5
ad9625-2600		12	-	1	Pipelined	$837.42	1	1.1	58.1	4
ad9625-2500		12	2.5G	1	Pipelined	$735.00	1	1.1	58.3	3.9
AD9691	-	14	1250M	2	Pipelined	$692.75	2.6	1.58	63.4	3.8
AD9680-1250		14	1.25G	2	Pipelined	$692.75	3	1.58	63.6	3.7
ad9625-2000		12	2G	1	Pipelined	$624.75	0.9	1.1	59.5	3.48
AD9680-1000		14	1G	2	Pipelined	$584.38	2.5	1.7	67.2	3.3
AD9694		14	500M	4	Pipelined	$488.75	1	-	67.1	1.66

Resolution?

3 bits to 24 bits (one at 32 bits)

4-Channel, 200 kSPS 12-Bit ADC with Sequencer in 16-Lead TSSOP

Data Sheet $2.58 in 1000's **AD7923**

FEATURES

Fast throughput rate: 200 kSPS
Specified for AV_{DD} of 2.7 V to 5.25 V
Low power
- **3.6 mW max at 200 kSPS with 3 V supply**
- **7.5 mW max at 200 kSPS with 5 V supply**

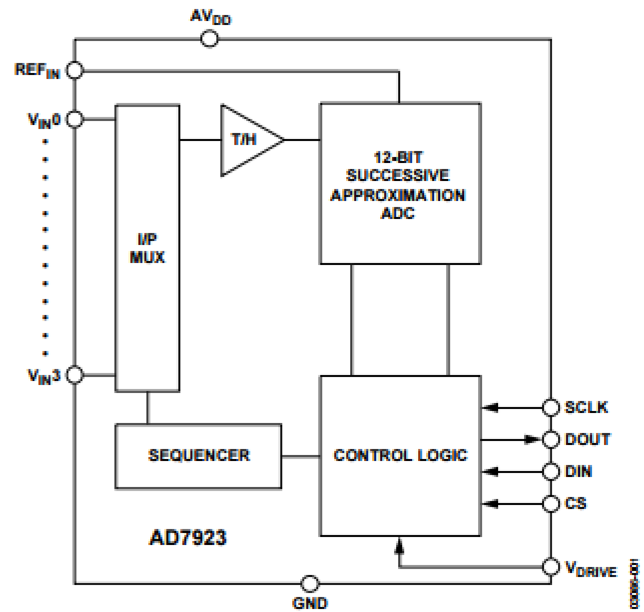
4 (single-ended) inputs with sequencer
Wide input bandwidth
- **70 dB Min SNR at 50 kHz input frequency**

Flexible power/serial clock speed management
No pipeline delays
High speed serial interface SPI®-/QSPI™-/MICROWIRE™-/DSP-compatible
Shutdown mode: 0.5 µA max
16-lead TSSOP package
Qualified for automotive applications

GENERAL DESCRIPTION

The AD7923 is a 12-bit, high speed, low power, 4-channel, suc-

FUNCTIONAL BLOCK DIAGRAM



SPECIFICATIONS

$AV_{DD} = V_{DRIVE}$ = 2.7 V to 5.25 V, REF_{IN} = 2.5 V, f_{SCLK} = 20 MHz, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	B Version[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 50 kHz sine wave, f_{SCLK} = 20 MHz
Signal-to-(Noise + Distortion) (SINAD)[2]	70	dB min	@ 5 V, −40°C to +85°C
	69	dB min	@ 5 V, 85°C to 125°C, typ 70 dB
	69	dB min	@ 3 V typ 70 dB, −40°C to +125°C
Signal-to-Noise (SNR)[2]	70	dB min	
Total Harmonic Distortion (THD)[2]	−77	dB max	@ 5 V typ, −84 dB
	−73	dB max	@ 3 V typ,−77 dB
Peak Harmonic or Spurious Noise	−78	dB max	@ 5 V typ, −86 dB
(SFDR)[2]	−76	dB max	@ 3 V typ, −80 dB
Intermodulation Distortion (IMD)[2]			f_A = 40.1 kHz, f_B = 41.5 kHz
Second Order Terms	−90	dB typ	
Third Order Terms	−90	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	50	ps typ	
Channel-to-Channel Isolation	−85	dB typ	f_{IN} = 400 kHz
Full Power Bandwidth	8.2	MHz typ	@ 3 dB
	1.6	MHz typ	@ 0.1 dB
DC ACCURACY[2]			
Resolution	12	Bits	
Integral Nonlinearity	±1	LSB max	
Differential Nonlinearity	−0.9/+1.5	LSB max	Guaranteed no missed codes to 12 bits
0 V to REF_{IN} Input Range			Straight binary output coding
Offset Error	±8	LSB max	Typ ±0.5 LSB
Offset Error Match	±0.5	LSB max	
Gain Error	±1.5	LSB max	
Gain Error Match	±0.5	LSB max	
0 V to 2 × REF_{IN} Input Range			−REF_{IN} to +REF_{IN} biased about REF_{IN} with twos complement output coding
Positive Gain Error	±1.5	LSB max	
Positive Gain Error Match	±0.5	LSB max	
Zero-Code Error	±8	LSB max	Typ ±0.8 LSB
Zero-Code Error Match	±0.5	LSB max	
Negative Gain Error	±1	LSB max	
Negative Gain Error Match	±0.5	LSB max	
ANALOG INPUT			
Input Voltage Range	0 to REF_{IN}	V	Range bit set to 1
	0 to 2 × REF_{IN}	V	Range bit set to 0, AV_{DD} = 4.75 V to 5.25 V
DC Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
REFERENCE INPUT			
REF_{IN} Input Voltage	2.5	V	±1% specified performance
DC Leakage Current	±1	µA max	
REF_{IN} Input Impedance	36	kΩ typ	f_{SAMPLE} = 200 kSPS
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7 × V_{DRIVE}	V min	
Input Low Voltage, V_{INL}	0.3 × V_{DRIVE}	V max	
Input Current, I_{IN}	±1	µA max	Typ 10 nA, V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[3]	10	pF max	

16-Bit, 200 MSPS/250 MSPS Analog-to-Digital Converter

Data Sheet | $120 in 1000's | **AD9467**

FEATURES

- 75.5 dBFS SNR to 210 MHz at 250 MSPS
- 90 dBFS SFDR to 300 MHz at 250 MSPS
- SFDR at 170 MHz at 250 MSPS
  - 92 dBFS at −1 dBFS
  - 100 dBFS at −2 dBFS
- 60 fs rms jitter
- Excellent linearity at 250 MSPS
  - DNL = ±0.5 LSB typical
  - INL = ±3.5 LSB typical
- 2 V p-p to 2.5 V p-p (default) differential full-scale input (programmable)
- Integrated input buffer
- External reference support option
- Clock duty cycle stabilizer
- Output clock available
- Serial port control
  - Built-in selectable digital test pattern generation
  - Selectable output data format
- LVDS outputs (ANSI-644 compatible)
- 1.8 V and 3.3 V supply operation

APPLICATIONS

- Multicarrier, multimode cellular receivers
- Antenna array positioning
- Power amplifier linearization
- Broadband wireless
- Radar
- Infrared imaging
- Communications instrumentation

FUNCTIONAL BLOCK DIAGRAM

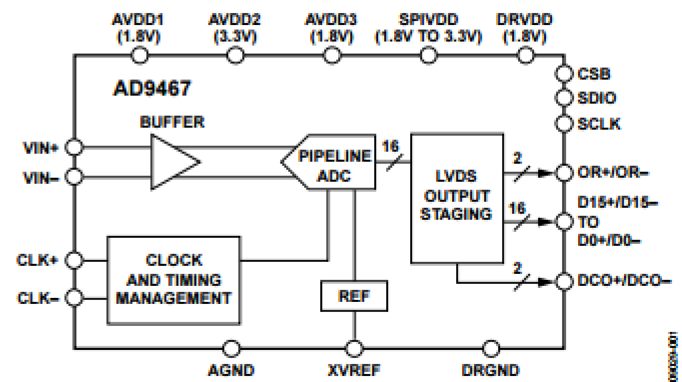


Figure 1.

A data clock output (DCO) for capturing data on the output is provided for signaling a new output bit.

The internal power-down feature supported via the SPI typically consumes less than 5 mW when disabled.

Optional features allow users to implement various selectable operating conditions, including input range, data format select, and output data test patterns.

The AD9467 is available in a Pb-free, 72-lead, LFCSP specified over the −40°C to +85°C industrial temperature range.

SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = −1.0 dBFS, DCS on, default SPI settings, unless otherwise noted.

Table 1.

Parameter[1]	Temp	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	−200	0	+200	LSB
Gain Error	Full	−3.9	−0.1	+2.6	%FSR
Differential Nonlinearity (DNL)[2]	Full	−0.9	±0.5	+1.5	LSB
Integral Nonlinearity (INL)[2]	Full	−12	±3.5	+12	LSB
TEMPERATURE DRIFT					
Offset Error	Full		±0.023		%FSR/°C
Gain Error	Full		±0.036		%FSR/°C
ANALOG INPUTS					
Differential Input Voltage Range (Internal VREF = 1 V to 1.25 V)	Full	2	2.5	2.5	V p-p
Common-Mode Voltage	25°C		2.15		V
Differential Input Resistance	25°C		530		Ω
Differential Input Capacitance	25°C		3.5		pF
Full Power Bandwidth	25°C		900		MHz
XVREF INPUT					
Input Voltage	Full	1		1.25	V
Input Capacitance	Full		3		pF
POWER SUPPLY					
AVDD1	Full	1.75	1.8	1.85	V
AVDD2	Full	3.0	3.3	3.6	V
AVDD3	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
I_{AVDD1}	Full		567	620	mA
I_{AVDD2}	Full		55	61	mA
I_{AVDD3}	Full		31	35	mA
I_{DRVDD}	Full		40	43	mA
Total Power Dissipation (Including Output Drivers)	Full		1.33	1.5	W
Power-Down Dissipation	Full		4.4	90	mW

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.

AC SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = −1.0 dBFS, DCS on, default SPI settings, unless otherwise noted.

Table 2.

Parameter[1]	Temp	Min	Typ	Max	Unit
ANALOG INPUT FULL SCALE		2.5	2/2.5		V p-p
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 5 MHz	25°C		74.7/76.4		dBFS
f_{IN} = 97 MHz	25°C		74.5/76.1		dBFS
f_{IN} = 140 MHz	25°C		74.4/76.0		dBFS
f_{IN} = 170 MHz	25°C	73.7	74.3/75.8		dBFS
	Full	71.5			dBFS
f_{IN} = 210 MHz	25°C		74.0/75.5		dBFS
f_{IN} = 300 MHz	25°C		73.3/74.6		dBFS
SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)					
f_{IN} = 5 MHz	25°C		74.6/76.3		dBFS
f_{IN} = 97 MHz	25°C		74.4/76.0		dBFS
f_{IN} = 140 MHz	25°C		74.4/76.0		dBFS
f_{IN} = 170 MHz	25°C	72.4	74.2/75.8		dBFS
	Full	71.0			dBFS
f_{IN} = 210 MHz	25°C		73.9/75.4		dBFS
f_{IN} = 300 MHz	25°C		73.1/74.4		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 5 MHz	25°C		12.1/12.4		Bits
f_{IN} = 97 MHz	25°C		12.1/12.3		Bits
f_{IN} = 140 MHz	25°C		12.1/12.3		Bits
f_{IN} = 170 MHz	25°C		12.0/12.3		Bits
	Full	11.5			Bits
f_{IN} = 210 MHz	25°C		12.0/12.2		Bits
f_{IN} = 300 MHz	25°C		11.9/12.1		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR) (INCLUDING SECOND AND THIRD HARMONIC DISTORTION)					
f_{IN} = 5 MHz	25°C		98/97		dBFS
f_{IN} = 97 MHz	25°C		95/93		dBFS
f_{IN} = 140 MHz	25°C		94/95		dBFS
f_{IN} = 170 MHz	25°C	82	93/92		dBFS
	Full	82			dBFS
f_{IN} = 210 MHz	25°C		93/92		dBFS
f_{IN} = 300 MHz	25°C		93/90		dBFS
SFDR (INCLUDING SECOND AND THIRD HARMONIC DISTORTION)					
f_{IN} = 5 MHz at −2 dB Full Scale	25°C		100/100		dBFS
f_{IN} = 97 MHz at −2 dB Full Scale	25°C		97/97		dBFS
f_{IN} = 140 MHz at−2 dB Full Scale	25°C		100/95		dBFS
f_{IN} = 170 MHz at −2 dB Full Scale	25°C		100/100		dBFS
f_{IN} = 210 MHz at −2 dB Full Scale	25°C		93/93		dBFS
f_{IN} = 300 MHz at −2 dB Full Scale	25°C		90/90		dBFS
WORST OTHER (EXCLUDING SECOND AND THIRD HARMONIC DISTORTION)					
f_{IN} = 5 MHz	25°C		98/97		dBFS
f_{IN} = 97 MHz	25°C		97/93		dBFS
f_{IN} = 140 MHz	25°C		97/95		dBFS
f_{IN} = 170 MHz	25°C	88	97/93		dBFS
	Full	82			dBFS
f_{IN} = 210 MHz	25°C		97/95		dBFS
f_{IN} = 300 MHz	25°C		97/95		dBFS

SWITCHING SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = −1.0 dBFS, DCS on, default SPI settings, unless otherwise noted.

Table 4.

Parameter[1]	Temp	Min	Typ	Max	Unit
CLOCK[2]					
Clock Rate	Full	50		250	MSPS
Clock Pulse Width High (t_{CH})	Full		2		ns
Clock Pulse Width Low (t_{CL})	Full		2		ns
OUTPUT PARAMETERS[2, 3]					
Propagation Delay (t_{PD})	25°C		3		ns
Rise Time (t_R) (20% to 80%)	25°C		200		ps
Fall Time (t_F) (20% to 80%)	25°C		200		ps
DCO Propagation Delay (t_{CPD})	25°C		3		ns
DCO to Data Delay (t_{SKEW})	Full	−200		+200	ps
Wake-Up Time (Power-Down)	Full		100		ms
Pipeline Latency	Full		16		Clock cycles
APERTURE					
Aperture Delay (t_A)	25°C		1.2		ns
Aperture Uncertainty (Jitter)	25°C		60		fs rms
Out-of-Range Recovery Time	25°C		1		Clock cycles

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] Can be adjusted via the SPI interface.
[3] Measurements were made using a part soldered to FR-4 material.

Performance Characterization of Data Converters

- A large number of parameters are used to characterize a data converter
- Performance parameters of interest depend strongly on the application
- Very small number of parameters of interest in many/most applications
- “Catalog” data converters are generally intended to satisfy a wide range of applications and thus have much more stringent requirements placd on their performance
- Custom application-specific data converter will generally perform much better than a “catalog” part in the same

Performance Characterization of Data Converters

- Static characteristics
  - Resolution
  - Least Significant Bit (LSB)
  - Offset and Gain Errors
  - Absolute Accuracy
  - Relative Accuracy
  - Integral Nonlinearity (INL)
  - Differential Nonlinearity (DNL)
  - Monotonicity (DAC)
  - Missing Codes (ADC)
  - Quantization Noise
  - Low-f Spurious Free Dynamic Range (SFDR)
  - Low-f Total Harmonic Distortion (THD)
  - Effective Number of Bits (ENOB)
  - Power Dissipation

Performance Characterization of Data Converters

- Dynamic characteristics
  - Conversion Time or Conversion Rate (ADC)
  - Settling time or Clock Rate (DAC)
  - Sampling Time Uncertainty (aperture uncertainty or aperture jitter)
  - Dynamic Range
  - Spurious Free Dynamic Range (SFDR)
  - Total Harmonic Distortion (THD)
  - Signal to Noise Ratio (SNR)
  - Signal to Noise and Distortion Ratio (SNDR)
  - Sparkle Characteristics
  - Effective Number of Bits (ENOB)

Dynamic characteristics

- Degradation of dynamic performance parameters often due to nonideal effects in time-domain performance
- Dynamic characteristics of high resolution data converters often challenging to measure, to simulate, to understand source of contributions, and to minimize

Example: An n-bit ADC would often require SFDR at the 6n+6 bit level or better. Thus, considering a 14-bit ADC, the SFDR would be expected to be at the -90dB level or better.
If the input to the ADC is a 1V p-p sinusoidal waveform, the second harmonic term would need to be at the $10^{(-90dB/20dB)} = 32\mu V$ level. A 32uV level is about 1part in 30,000. Signals at this level are difficult to accurately simulate in the presence of a 1V level signal. For example, convergence parameters in simulators and sample (strobe) points used in data acquisition adversely affect simulation results and observing the time domain waveforms that contribute to nonlinearity at this level and relationships between these waveforms and the sources of nonlinearity is often difficult to visualize. Simulation errors that are at the 20dB level or worse can occur if the simulation environment is not correctly established.

Characterization of Data Converter Performance

- Almost all ADC architectures will work perfectly if nonideal effects are ignored !!
- Most data converter design effort involves managing nonideal properties of components
- “Devil is often in the detail” when designing an ADC

Critical to know how to accurately characterize an ADC

What may appear to be minor differences in performance are often differentiators in both the marketplace and in the profit potential of a part

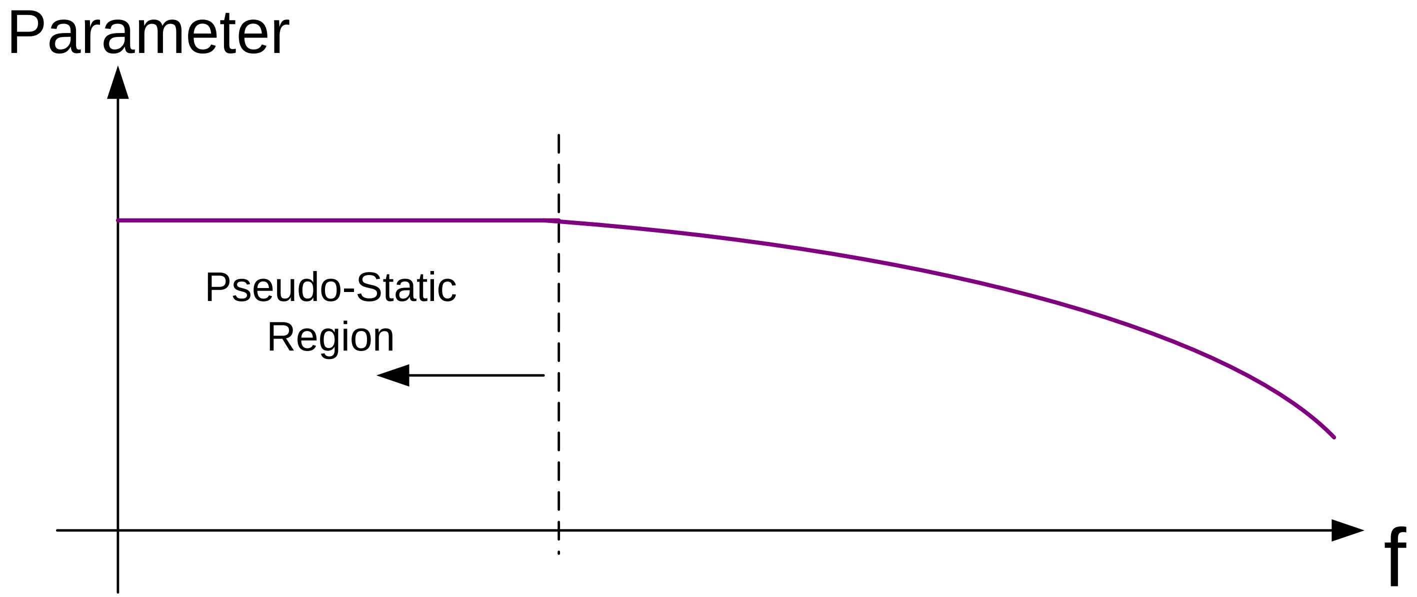
Performance Characterization of Data Converters

What is meant by "low frequency" ?

Operation at frequencies so low that further decreases in frequency cause no further changes in a parameter of interest

Low frequency operation is often termed Pseudo-static operation

Low-frequency or Pseudo-Static Performance



Performance Characterization

Resolution

- Number of distinct analog levels in an ADC
- Number of digital output codes in A/D
- In most cases this is a power of 2
- If a converter can resolve 2^n levels, then we term it an n-bit converter
  - 2^n analog outputs for an n-bit DAC
  - 2^n-1 transition points for an n-bit ADC
- Resolution is often determined by architecture and thus not measured
- Effective resolution can be defined and measured
  - If N levels can be resolved for an DAC then

$$n_{EQ} = \frac{\log N}{\log 2}$$

  - If N-1 transition points in an ADC, then

$$n_{EQ} = \frac{\log N}{\log 2}$$

Performance Characterization

Least Significant Bit

Assume $N = 2^n$

Generally Defined by Manufacturer to be

$$x_{LSB} = x_{REF}/N$$

Effective Value of LSB can be Measured

For DAC: x_{LSB} is equal to the maximum increment in the output for a single bit change in the Boolean input

For ADC: x_{LSB} is equal to the maximum distance between two adjacent transition points

Performance Characterization of Data Converters

- Static characteristics
  - Resolution
  - Least Significant Bit (LSB)
  - Offset and Gain Errors
  - Absolute Accuracy
  - Relative Accuracy
  - Integral Nonlinearity (INL)
  - Differential Nonlinearity (DNL)
  - Monotonicity (DAC)
  - Missing Codes (ADC)
  - Quantization Noise
  - Low-f Spurious Free Dynamic Range (SFDR)
  - Low-f Total Harmonic Distortion (THD)
  - Effective Number of Bits (ENOB)
  - Power Dissipation

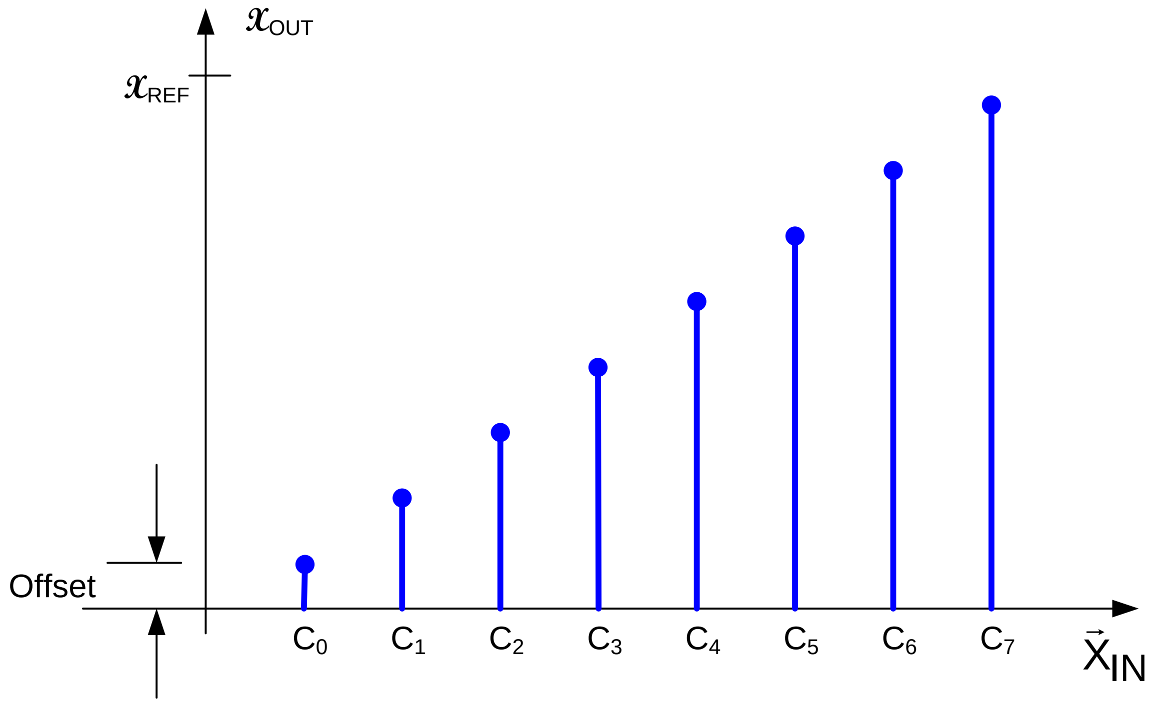
Performance Characterization

Offset

For DAC with ideal code 0 output of 0V the offset is

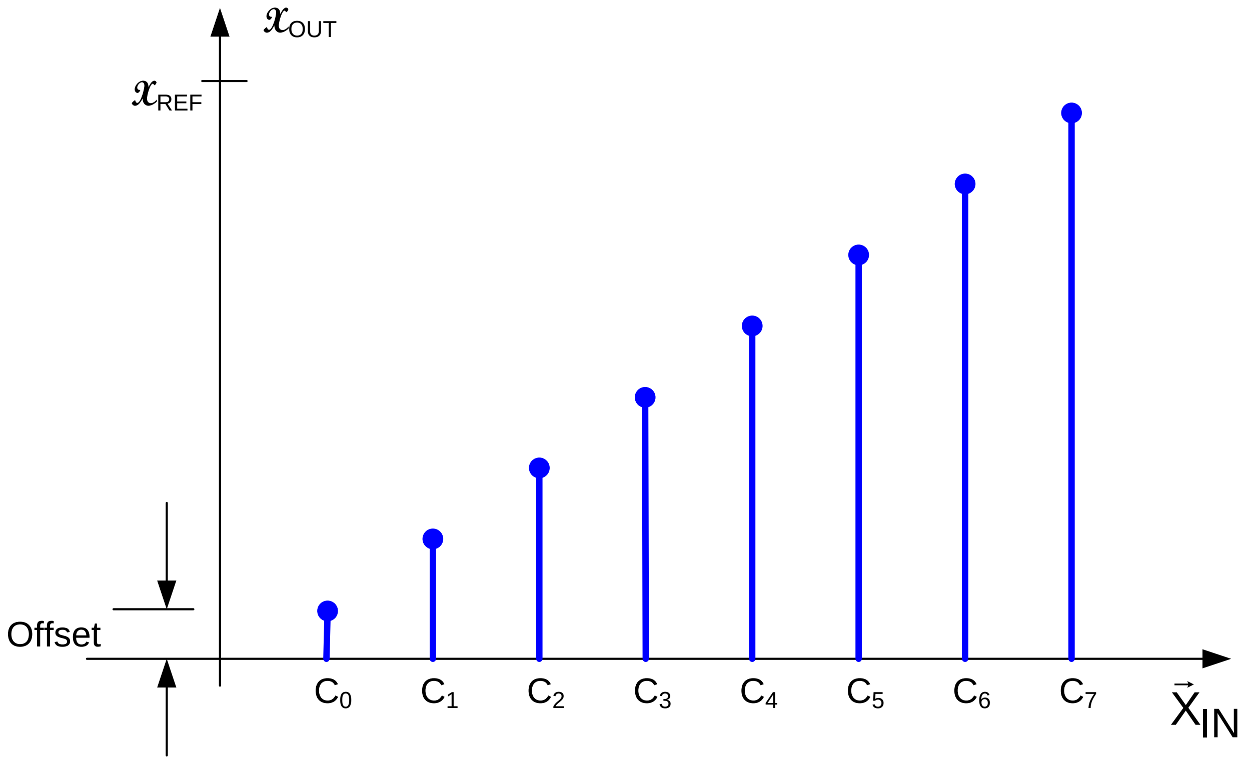
$x_{OUT}(<0,\ldots,0>)$ - absolute

$$\frac{x_{OUT}(\langle 0,\ldots,0\rangle)}{x_{LSB}}$$ - in LSB



Performance Characterization

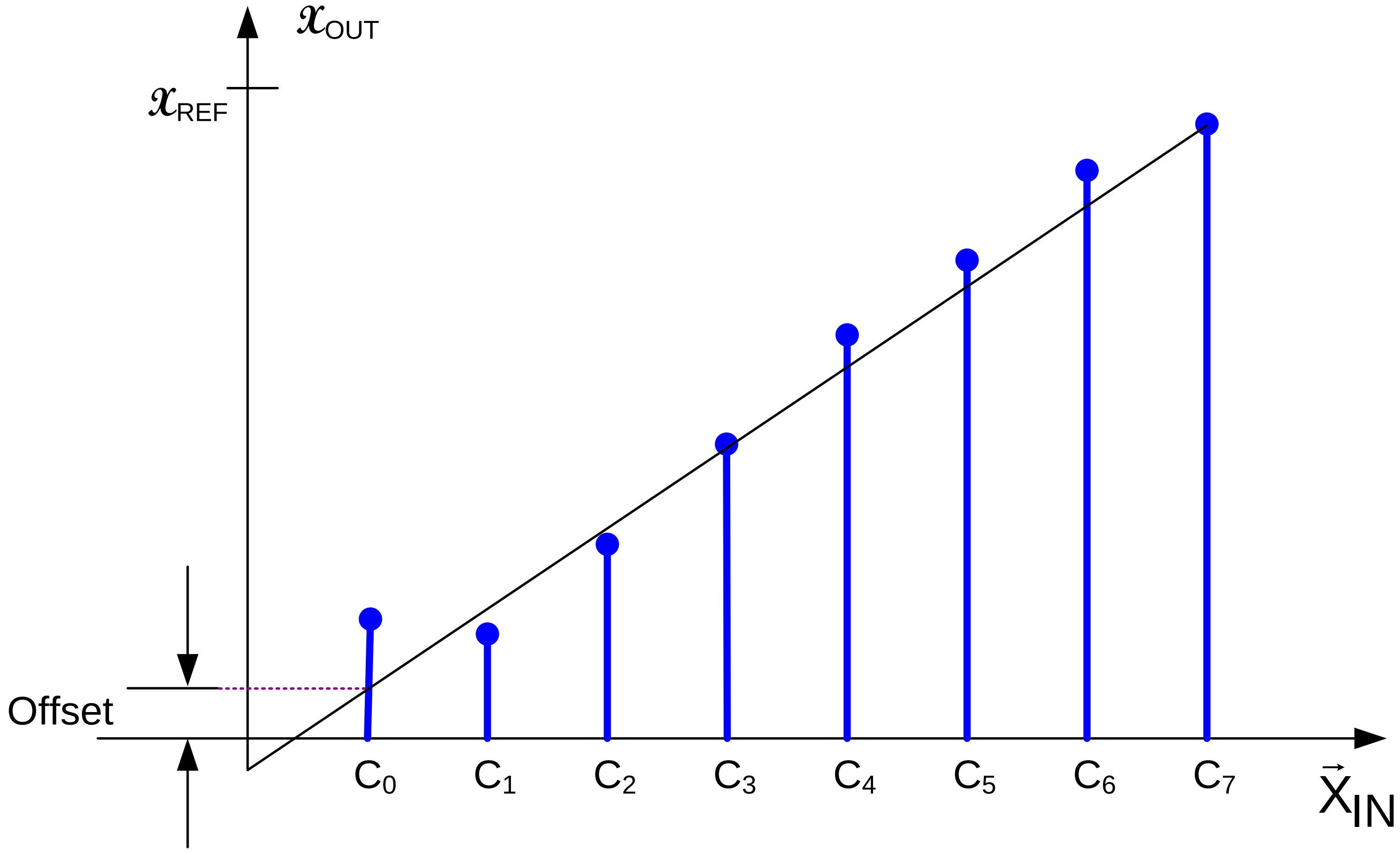
Offset (for DAC)



- Offset strongly (totally) dependent upon performance at a single point
- Probably more useful to define relative to a fit of the data

Performance Characterization

Offset (for DAC)



Offset relative to fit of data

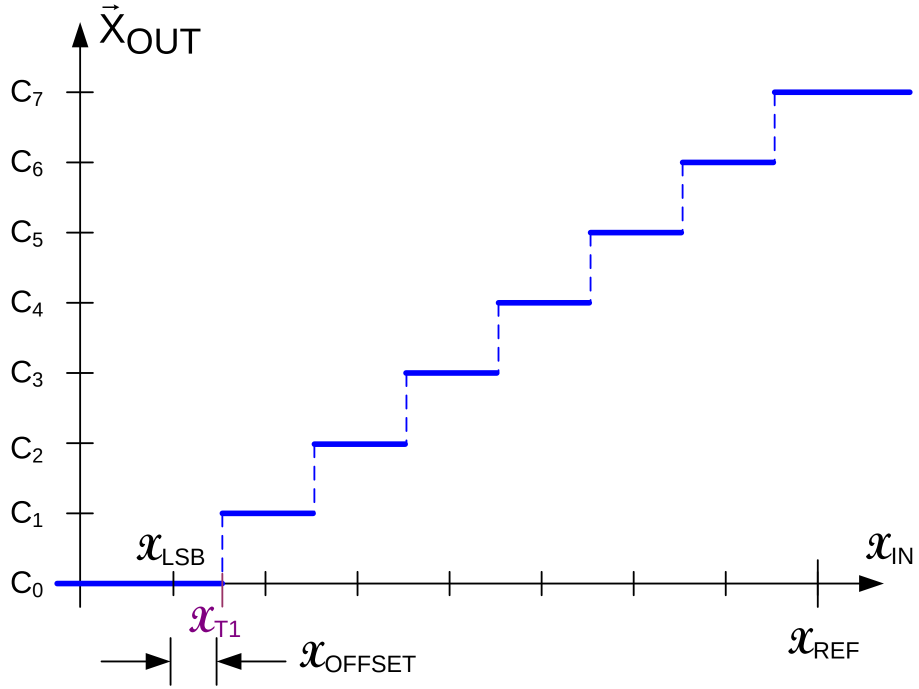
Performance Characterization

Offset

For ADC with ideal transition point at 1 LSB, the offset is

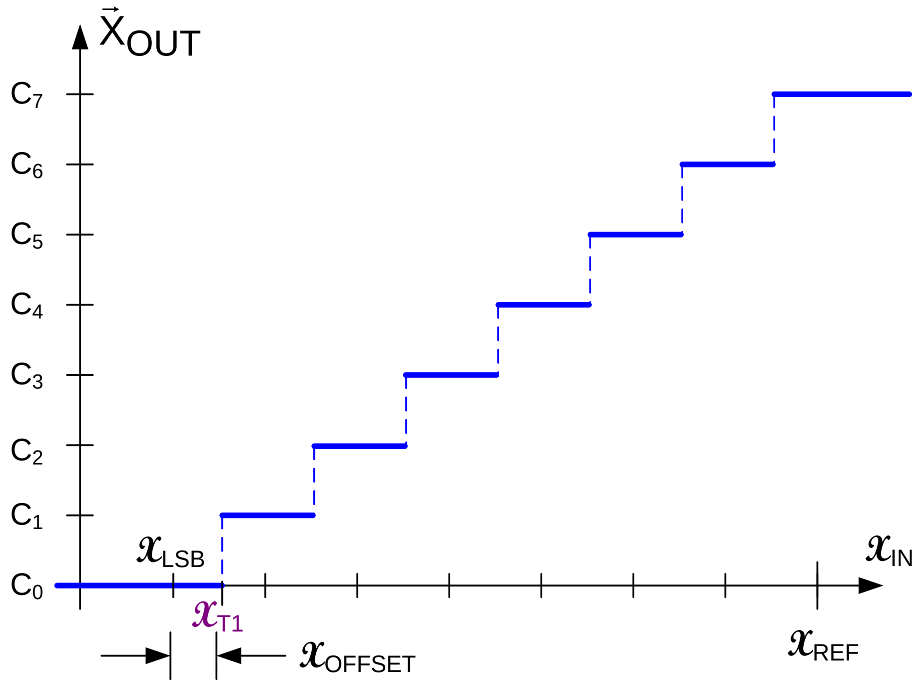
$x_{T1} - x_{LSB}$ - absolute

$\frac{x_{T1} - x_{LSB}}{x_{LSB}}$ - in LSB



Offset

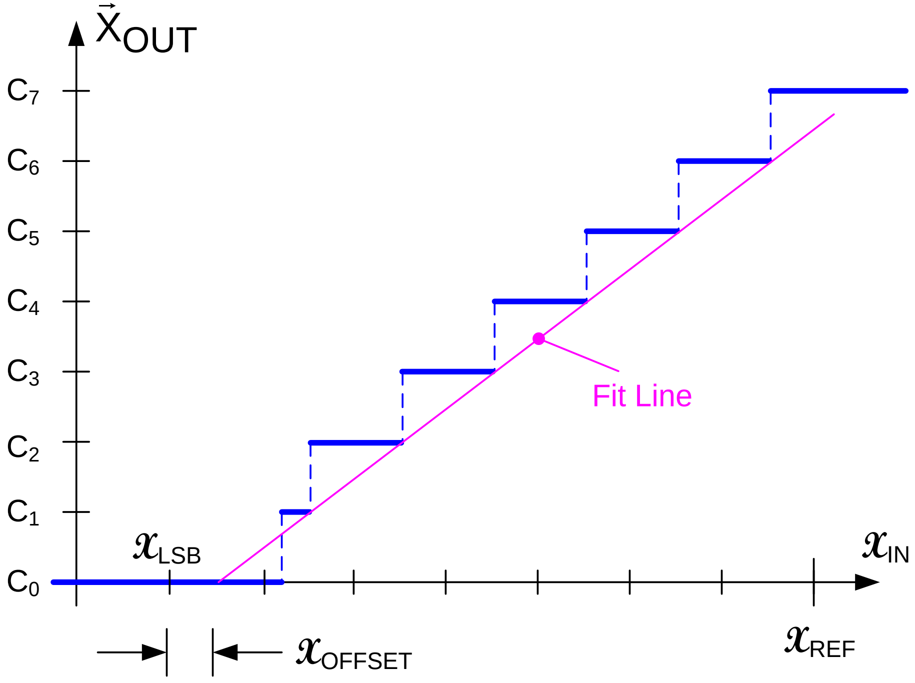
For ADC the offset is



- Offset strongly (totally) dependent upon performance at a single point
- Probably more useful to define relative to a fit of the data

Offset

For ADC the offset is

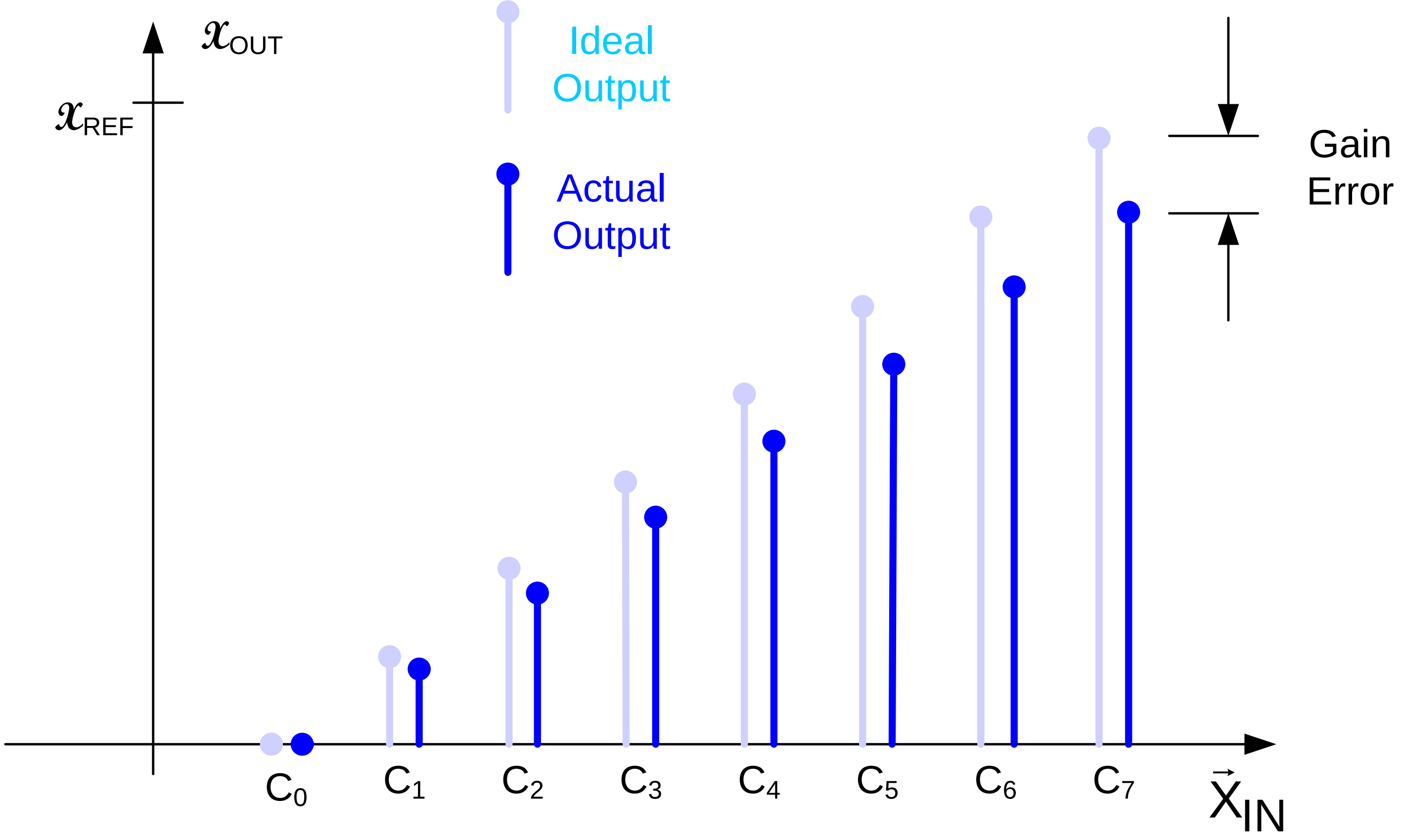


Offset relative to fit of data

Performance Characterization

Gain and Gain Error

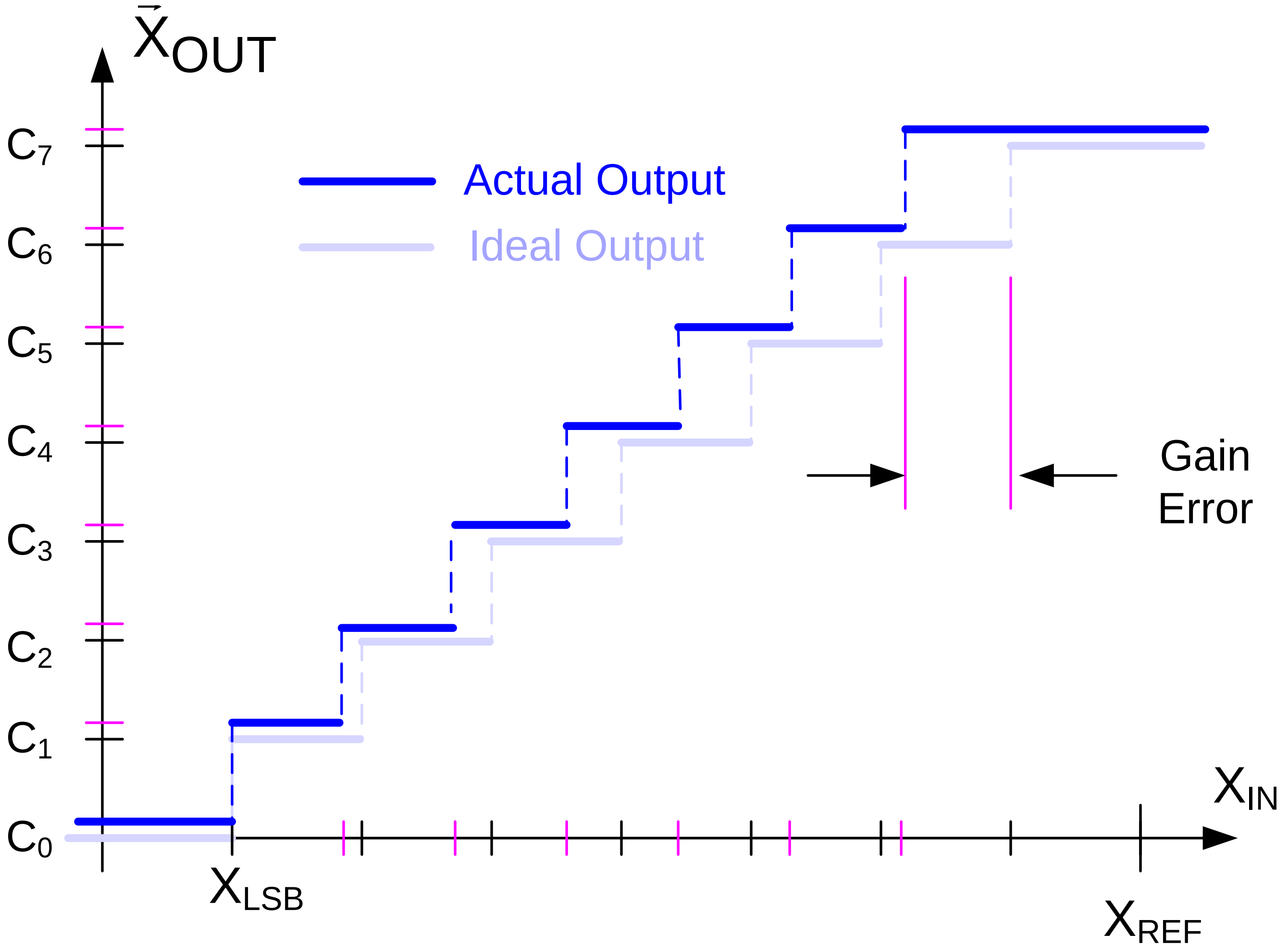
For DAC



Performance Characterization

Gain and Gain Error

For ADC



Performance Characterization

Gain and Offset Errors

- Fit line would give better indicator of error in gain but less practical to obtain in test
- Gain and Offset errors of little concern in many applications
- Performance of systems using data converters is often nearly independent of gain and offset errors
- Can be trimmed in field if gain or offset errors exist and are of concern

Performance Characterization of Data Converters

- Static characteristics
  - Resolution
  - Least Significant Bit (LSB)
  - Offset and Gain Errors
  - Absolute Accuracy
  - Relative Accuracy
  - Integral Nonlinearity (INL)
  - Differential Nonlinearity (DNL)
  - Monotonicity (DAC)
  - Missing Codes (ADC)
  - Quantization Noise
  - Low-f Spurious Free Dynamic Range (SFDR)
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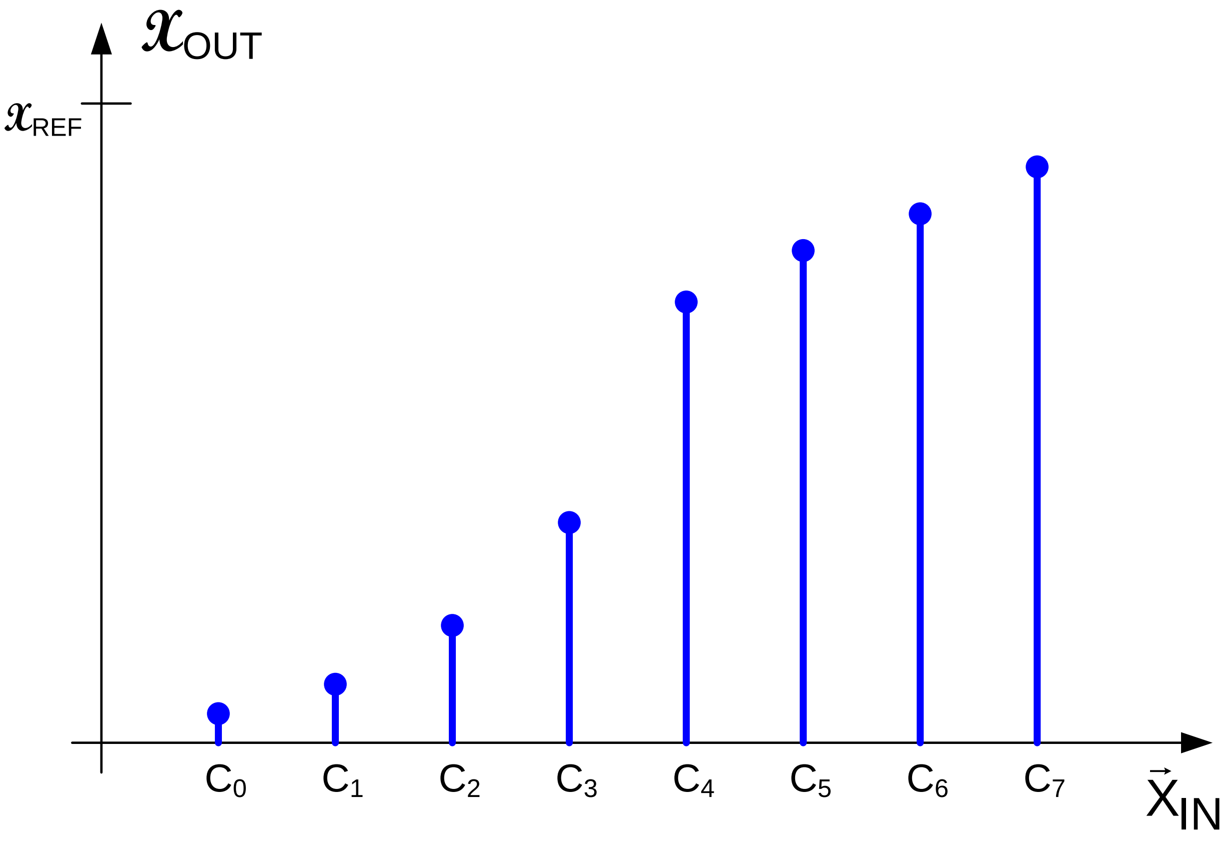
  - Effective Number of Bits (ENOB)
  - Power Dissipation

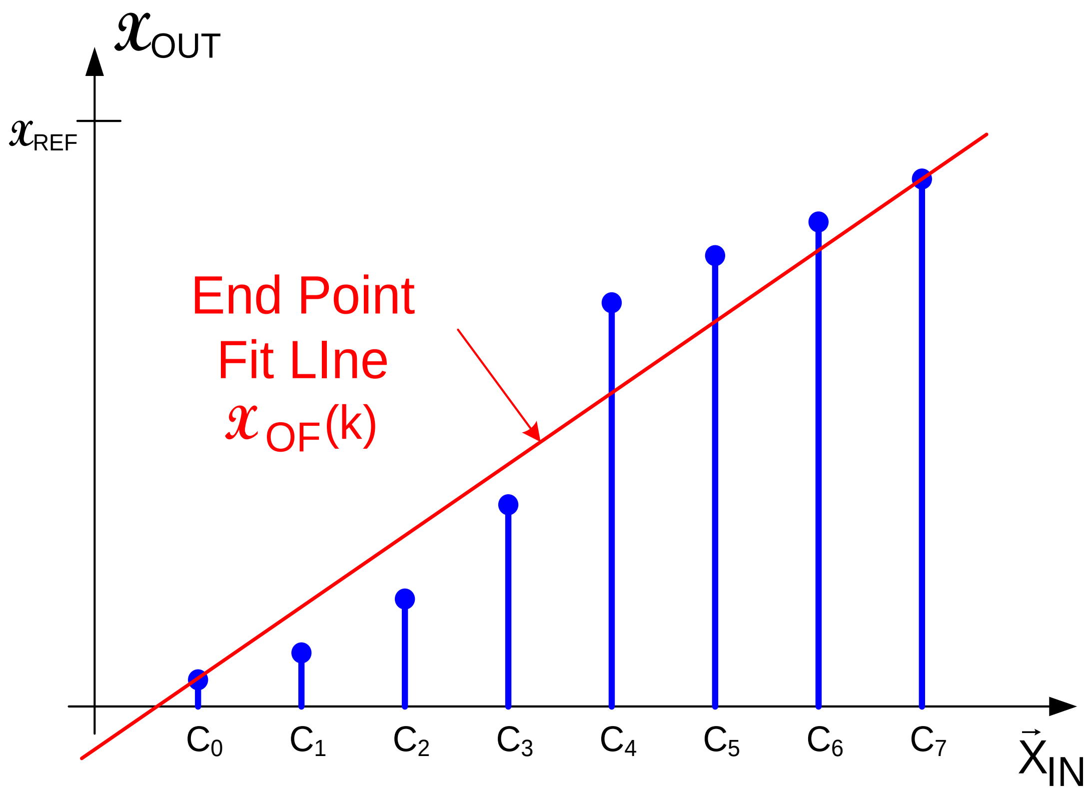
Integral Nonlinearity (DAC)

Nonideal DAC



Integral Nonlinearity (DAC)

Nonideal DAC

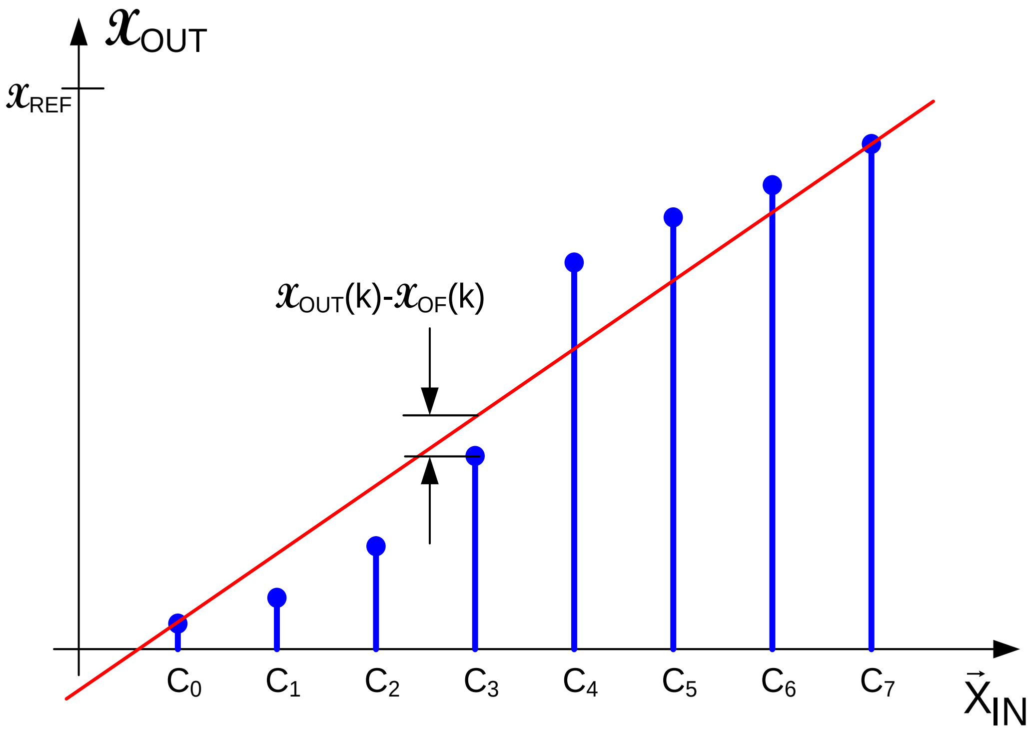


$$x_{OF}(k) = mk + x_{OUT}(0)$$

$$m = \frac{x_{OUT}(N-1) - x_{OUT}(0)}{N-1}$$

Integral Nonlinearity (DAC)

Nonideal DAC

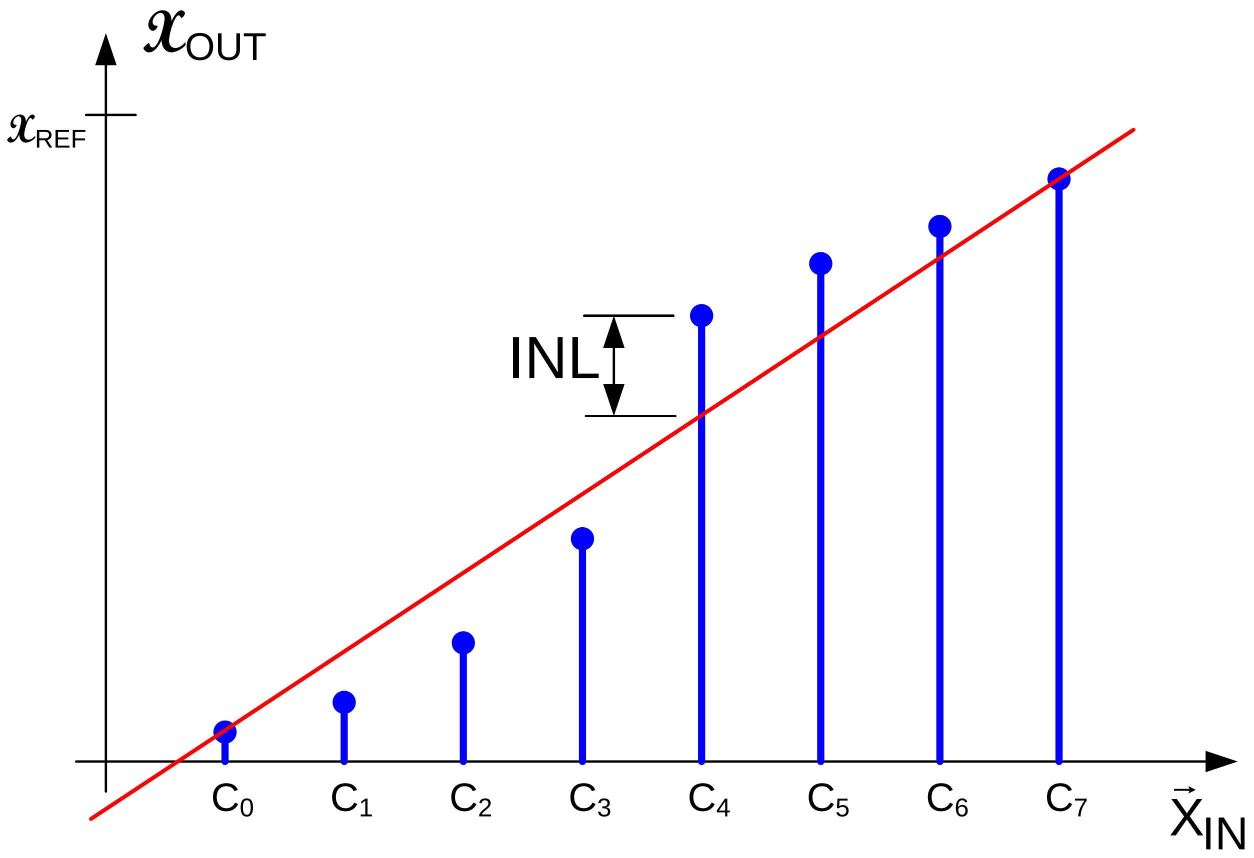


$$INL_k = \mathcal{X}_{OUT}(k) - \mathcal{X}_{OF}(k)$$

$$INL = \max_{0 \le k \le N-1} \left\{ \left| INL_k \right| \right\}$$

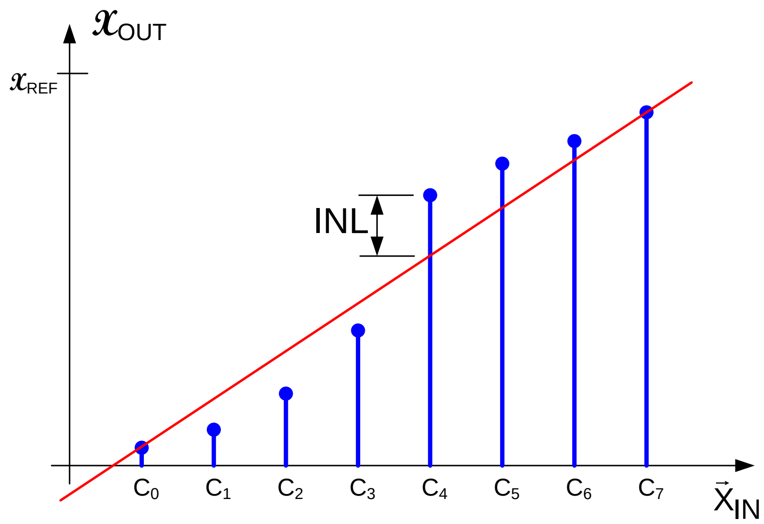
Integral Nonlinearity (DAC)

Nonideal DAC



Integral Nonlinearity (DAC)

Nonideal DAC



INL often expressed in LSB

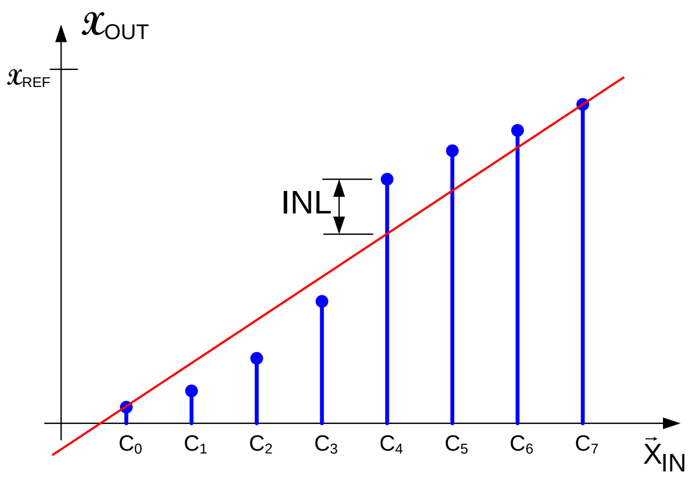
$$INL_k = \frac{x_{OUT}(k) - x_{OF}(k)}{x_{LSB}}$$

$$INL = \max_{0 \le k \le N-1} \{|INL_k|\}$$

- INL is often the most important parameter of a DAC
- INL_0 and INL_{N-1} are 0 (by definition)
- There are N-2 elements in the set of INL_k that are of concern
- INL is almost always nominally 0 (i.e. designers try to make it 0)
- INL is a random variable at the design stage
- INL_k is a random variable for $0<k<N-1$
- INL_k and INL_{k+j} are almost always correlated for all k,j (not incl 0, N-1)
- Fit Line is a random variable
- INL is the N-2 order statistic of a set of N-2 correlated random variables
- **INL is a parameter that is attempting to characterize the linearity of a DAC !**

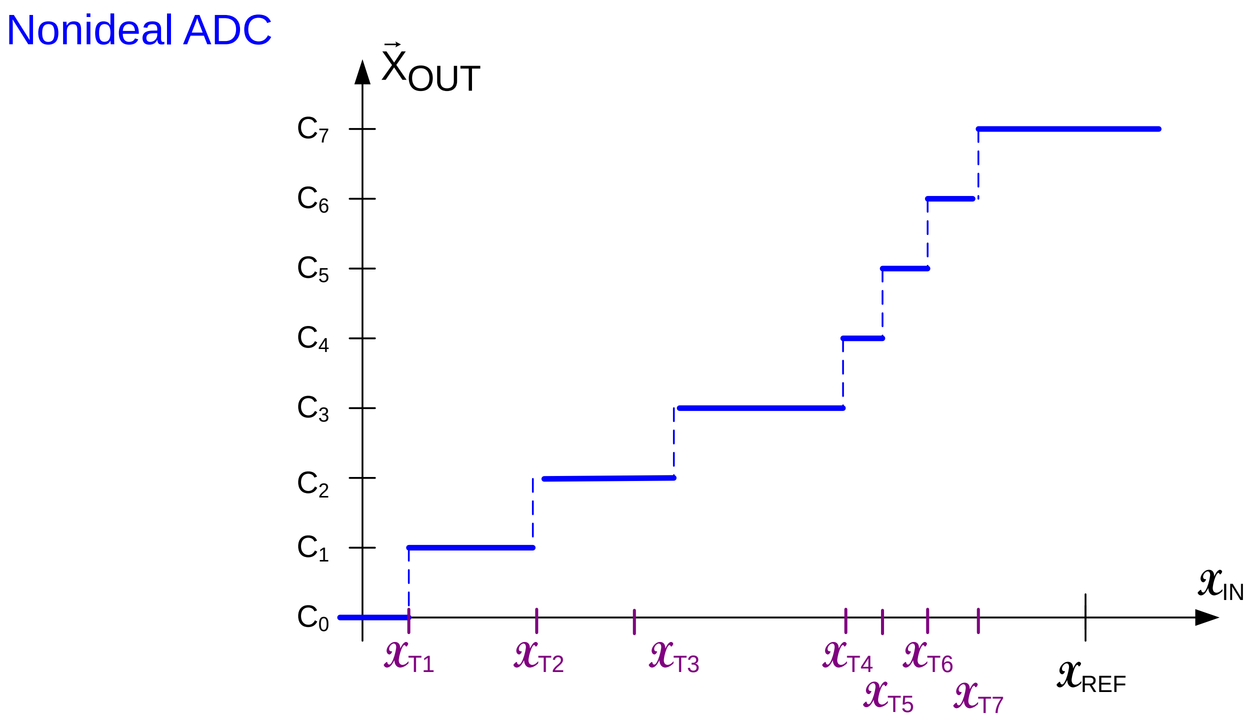
Integral Nonlinearity (DAC)

Nonideal DAC



- At design stage, INL characterized by standard deviation of the random variable
- Closed-form expressions for INL almost never exist because PDF of order statistics of correlated random variables is extremely complicated
- Simulation of INL very time consuming if n is very large (large sample size required to establish reasonable level of confidence)
  - Model parameters become random variables
  - Process parameters affect multiple model parameters causing model parameter correlation
  - Simulation times can become very large
- INL can be readily measured in laboratory but often dominates test costs because of number of measurements needed when n is large
- Expected value of INL_k at k=(N-1)/2 is largest for many architectures
- Major effort in DAC design is in obtaining acceptable yield !
- Yield often strongly dependent upon matching of random variables!

Integral Nonlinearity (ADC)



x_{Tk} is the transition input to code C_k

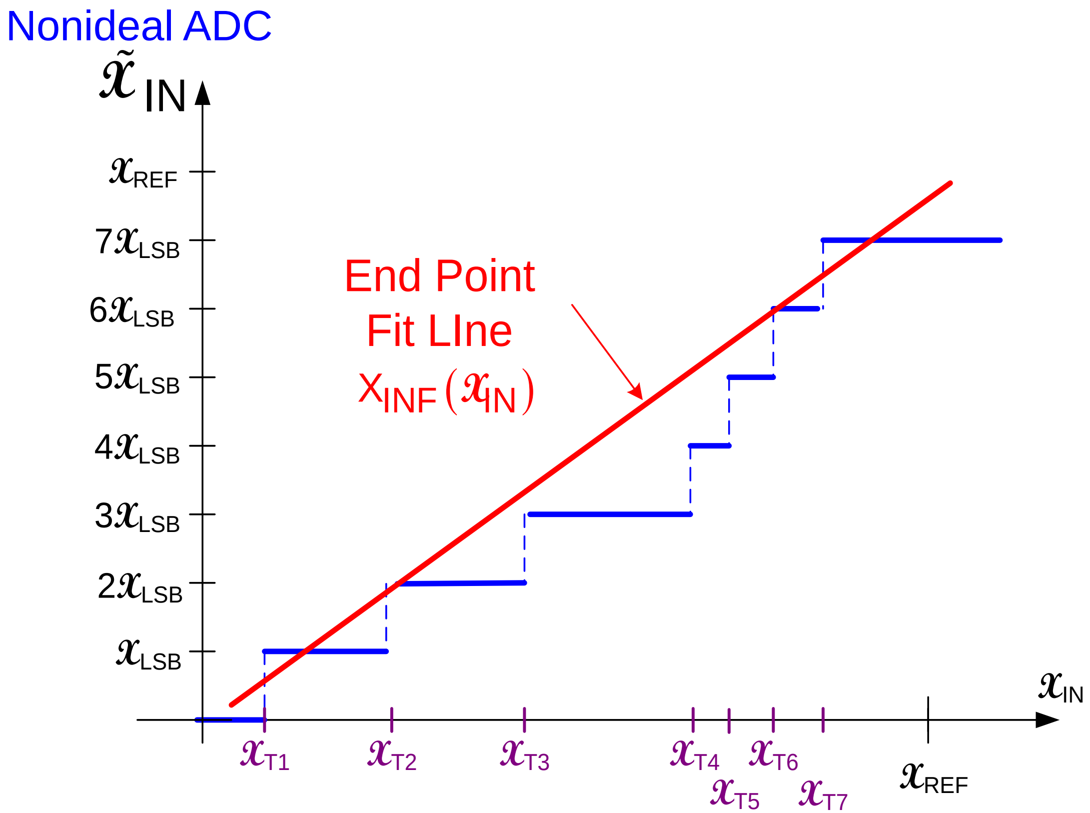
Transition points are not uniformly spaced !

More than one definition for INL exists !

Will give two definitions here (second almost always used)

Note: is some cases the sequence $< x_{Tk} >$ may not be monotone

Integral Nonlinearity (ADC)



Consider end-point fit line with interpreted output axis

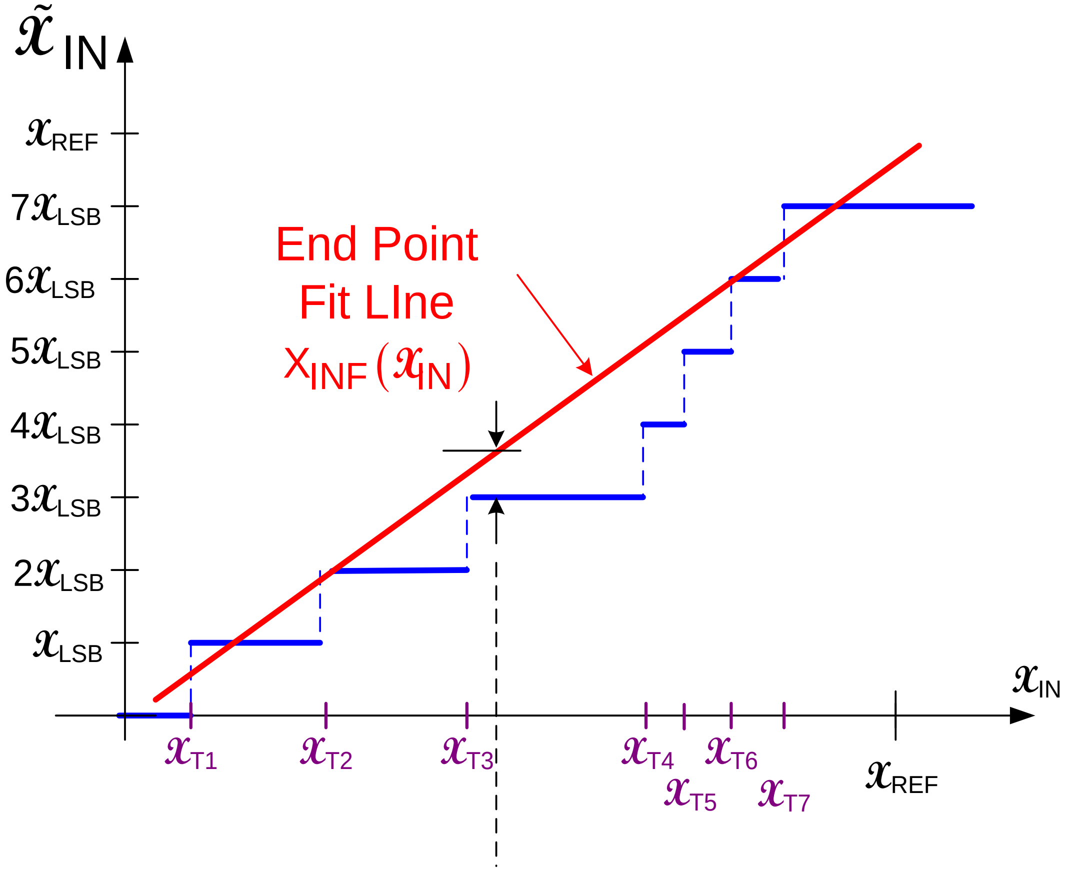
$$X_{INF}(x_{IN}) = m x_{IN} + \left(\frac{x_{LSB}}{2} - m x_{T1}\right)$$

$$m = \frac{(N-2)\,x_{LSB}}{x_{T7} - x_{T1}}$$

Integral Nonlinearity (ADC)

Nonideal ADC

Continuous-input based INL definition



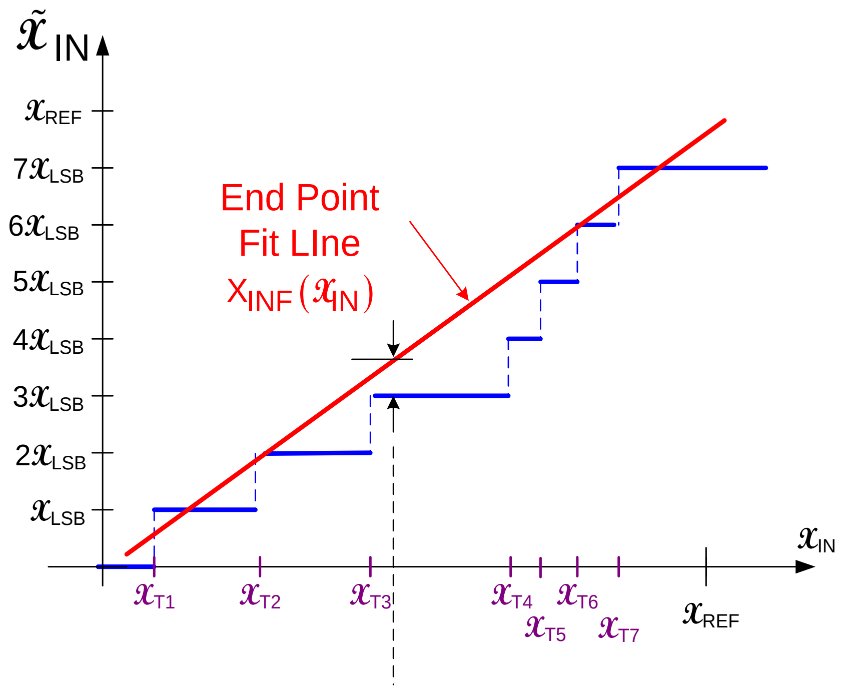
$$INL(x_{IN}) = \tilde{x}_{IN}(x_{IN}) - X_{INF}(x_{IN})$$

$$INL = \max_{0 \le x_{IN} \le x_{REF}} \left\{ \left| INL(x_{IN}) \right| \right\}$$

Integral Nonlinearity (ADC)

Nonideal ADC

Continuous-input based INL definition



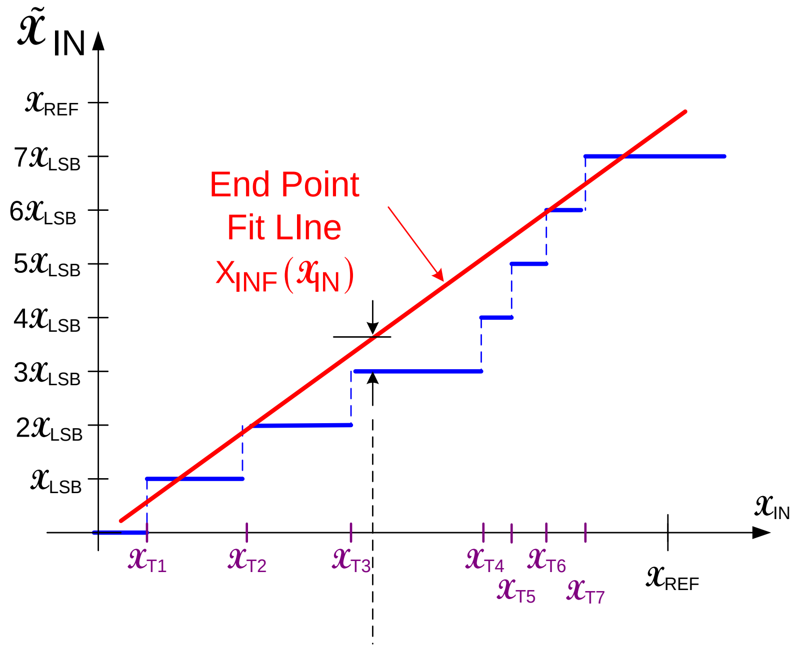
Often expressed in LSB

$$INL(x_{IN}) = \frac{\tilde{x}_{IN}(x_{IN}) - X_{INF}(x_{IN})}{x_{LSB}}$$

$$INL = \max_{0 \le x_{IN} \le x_{REF}} \left\{ \left| INL(x_{IN}) \right| \right\}$$

Integral Nonlinearity (ADC)

Nonideal ADC



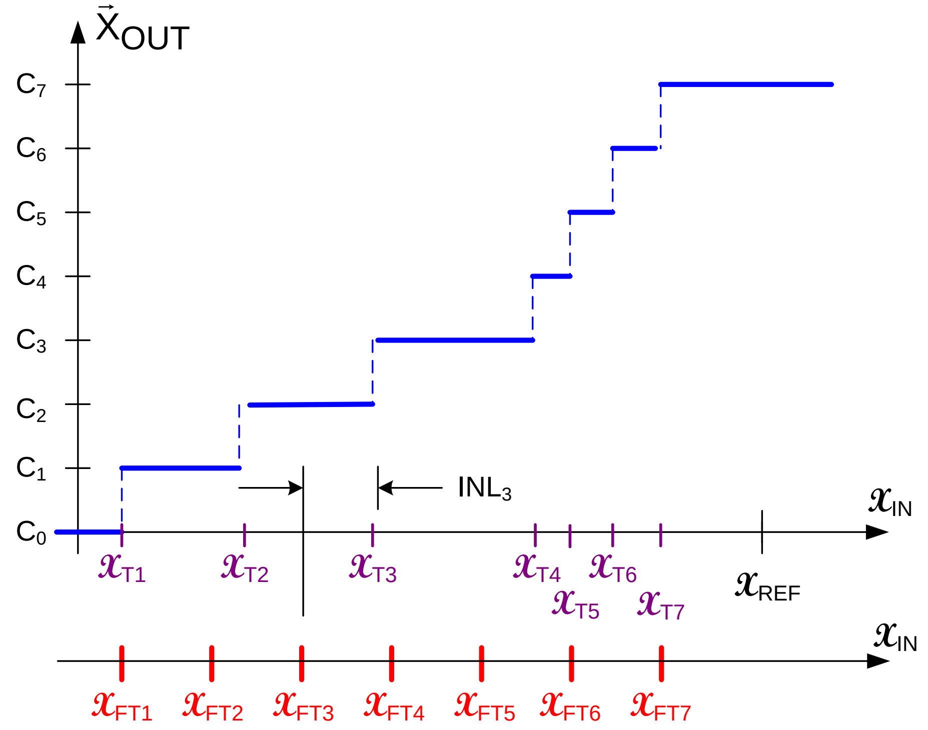
With this definition of INL, the INL of an ideal ADC is $x_{LSB}/2$ (for $x_{T1}=x_{LSB}$)

This is effective at characterizing the overall nonlinearity of the ADC but does not vanish when the ADC is ideal and the effects of the breakpoints is not explicit

Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition (assuming N-3 internal transitions)



Place N-3 uniformly spaced points between X_{T1} and $X_{T(N-1)}$ designated x_{FTk}

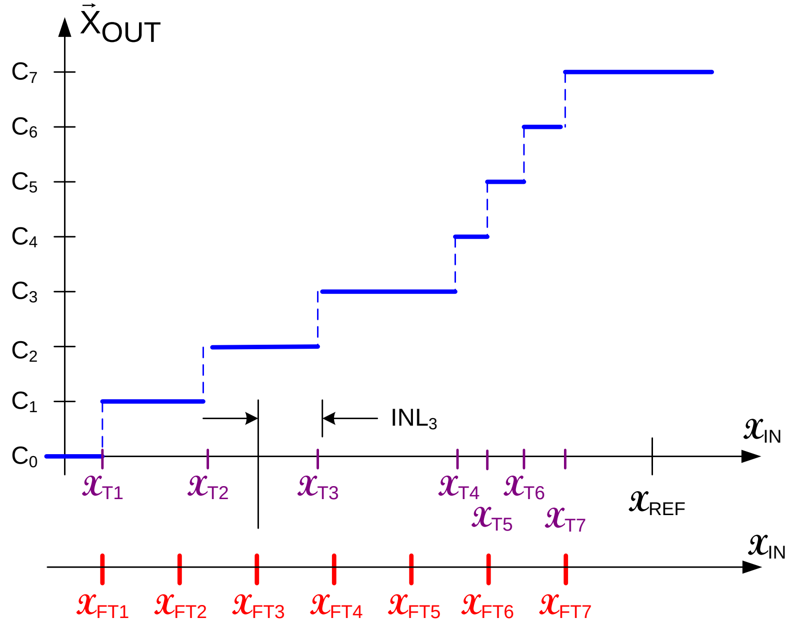
$$INL_k = x_{Tk} - x_{FTk} \qquad 1 \le k \le N-2$$

$$INL = \max_{2 \le k \le N-2} \{|INL_k|\}$$

Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition (assuming N-3 internal transitions)



Often expressed in LSB

$$INL_k = \frac{x_{Tk} - x_{FTk}}{x_{LSB}} \qquad 1 \le k \le N-2$$

$$INL = \max_{2 \le k \le N-2} \{|INL_k|\}$$

For an ideal ADC, INL is ideally 0

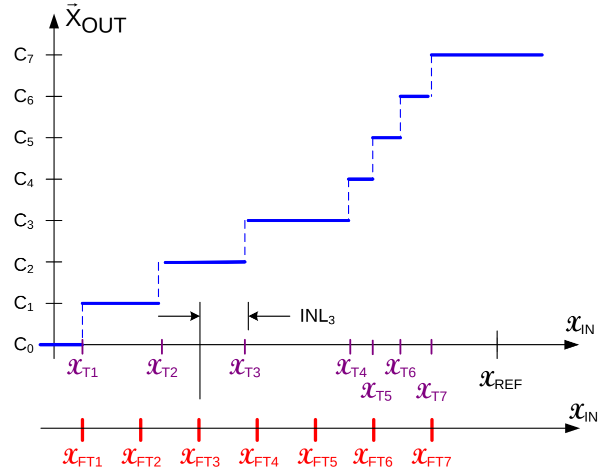
Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition (assuming N-3 internal transitions)

$$INL_k = \frac{x_{Tk} - x_{FTk}}{x_{LSB}} \qquad 1 \le k \le N-2$$

$$INL = \max_{2 \le k \le N-2} \{|INL_k|\}$$



- INL is often the most important parameter of an ADC
- INL_1 and INL_{N-1} are 0 (by definition)
- There are N-3 elements in the set of INL_k that are of concern
- INL is a random variable at the design stage
- INL_k is a random variable for 0<k<N-1
- INL_k and INL_{k+j} are correlated for all k,j (not incl 0, N-1) for most architectures
- Fit Line (for cont INL) and uniformly spaced break pts (breakpoint INL) are random variables
- INL is the N-3 order statistic of a set of N-3 correlated random variables (breakpoint INL)
- **INL is a parameter that is attempting to characterize the linearity of an ADC !**

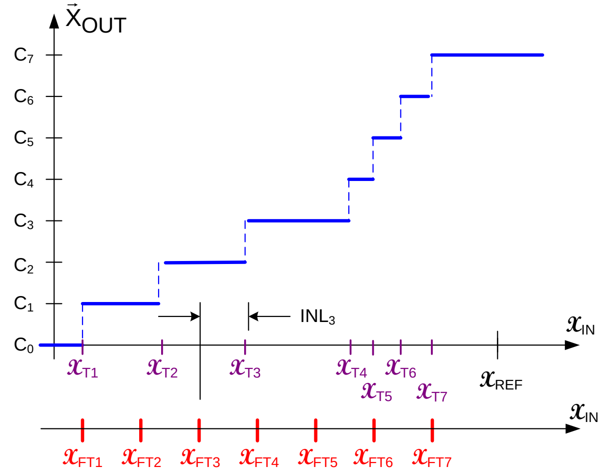
Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition (assuming N-3 internal transitions)

$$INL_k = \frac{x_{Tk} - x_{FTI}}{x_{LSB}} \qquad 1 \le k \le N-2$$

$$INL = \max_{2 \le k \le N-2} \{|INL_k|\}$$



What if there are less than N-3 internal transitions?

- Assume N-k internal transitions where k>3
- Data converter may still perform quite well !
- Insert N-k uniformly spaced values and use previous definition
- Unusual issues can crop up when testing data converters and it is important to have well-defined algorithms for handling these situations

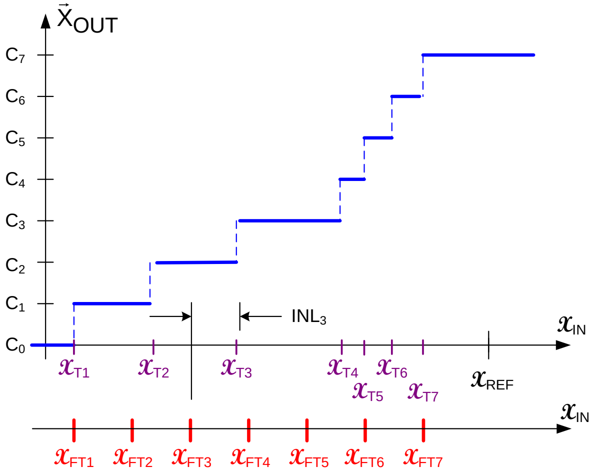
Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition

$$INL_k = \frac{x_{Tk} - x_{FTk}}{x_{LSB}} \qquad 1 \le k \le N-2$$

$$INL = \max_{2 \le k \le N-2} \{ |INL_k| \}$$



- At design stage, INL characterized by standard deviation of many random variables
- Closed-form expressions for INL almost never exist because PDF of order statistics of correlated random variables is extremely complicated
- Simulation of INL very time consuming if n is very large (large sample size required to establish reasonable level of confidence)
  - -Model parameters become random variables
  - -Process parameters affect multiple model parameters causing model parameter correlation
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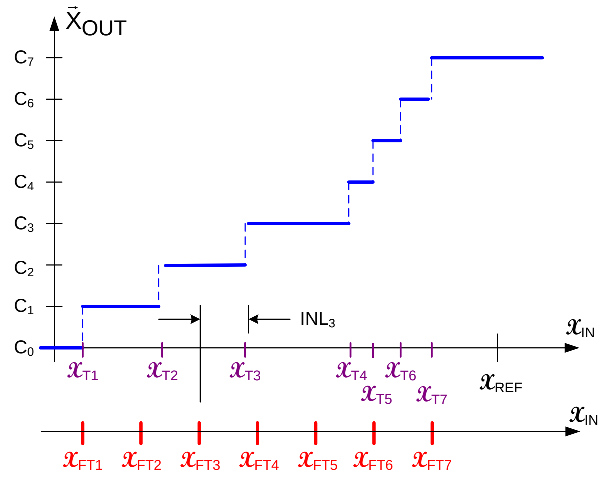
Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition

$$\text{INL}_k = \frac{x_{Tk} - x_{FTk}}{x_{LSB}} \qquad 1 \le k \le N\text{-}2$$

$$\text{INL} = \max_{2 \le k \le N-2} \left\{ \left| \text{INL}_k \right| \right\}$$



- INL can be readily measured in laboratory but often dominates test costs because of number of measurements needed when n is large
- Expected value of INL_k at k=(N-1)/2 is largest for many architectures
- INL of $\frac{x_{LSB}}{2}$ often considered acceptable (this is the ideal value of the continuous-input INL)

- Major effort in ADC design is in obtaining an INL acceptable yield !
- Yield often strongly dependent upon matching of random variables !

Stay Safe and Stay Healthy !

End of Lecture 1